



“It’s the Economy,..”

**A Qualitative And Quantitative
Look At Circuit Design**

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Introduction

- Chip complexity increases
- Number of design parameters increases
- Satisfying delay constraints is a challenge
- Area is a major constraint
- Power consumption has become a major constraint
- .. and the future doesn't look any simpler

A Design Flow

- Microprocessors are divided into many ‘blocks’
- Most blocks use gates from standard cell libraries
 - Each gate comes in many different sizes
- There are 100s of different blocks
- Blocks may have many 1000s of gates
- Blocks are designed by compiler or by ‘hand’

Circuit Design Questions

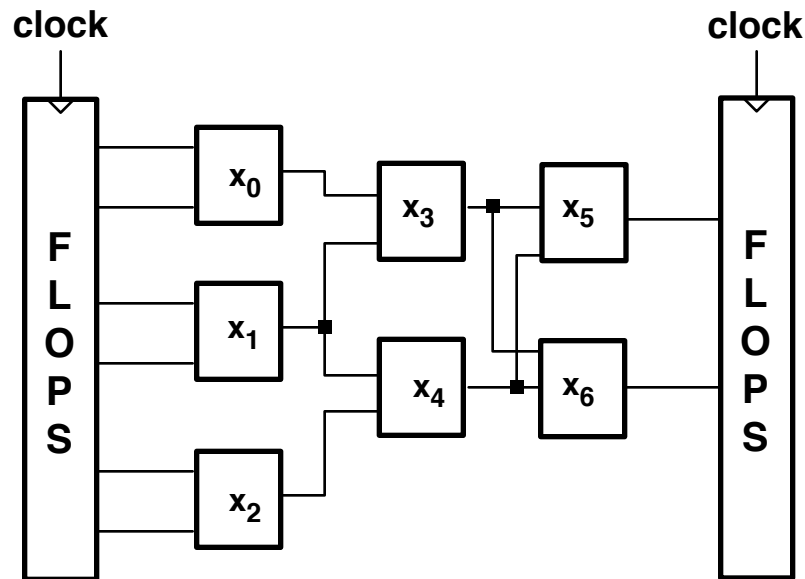
- What circuit implementation do I choose?
- Leave it to compiler?
- What gate sizes do I choose?
 - > low, normal, or high threshold gates?
- How do I satisfy the delay constraints?
 - > area constraints? power constraints?
- How do I optimize for delay?
 - > area? power?
- Can it be done (before tape-out date)?

Main Goals of Circuit Optimization

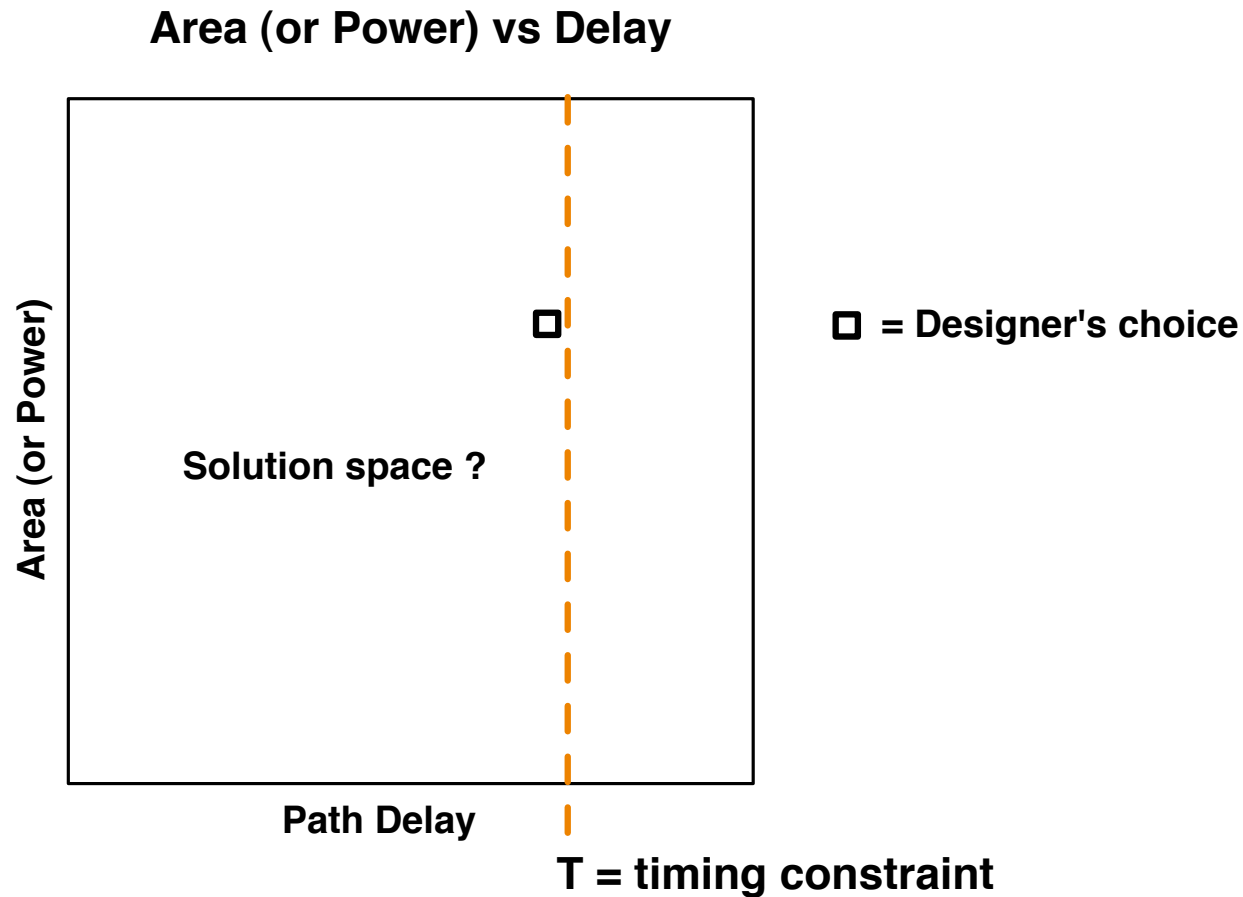
- Optimize circuit under constraints
 - > Main initial parameter: size of gate
 - > Optimization objectives: delay, area, and energy
 - > Constraints: delay, area, energy, ..
- Show trade offs between delay, area, and energy
- Compare different circuits independent of technology
- Simplify task of designer

Example

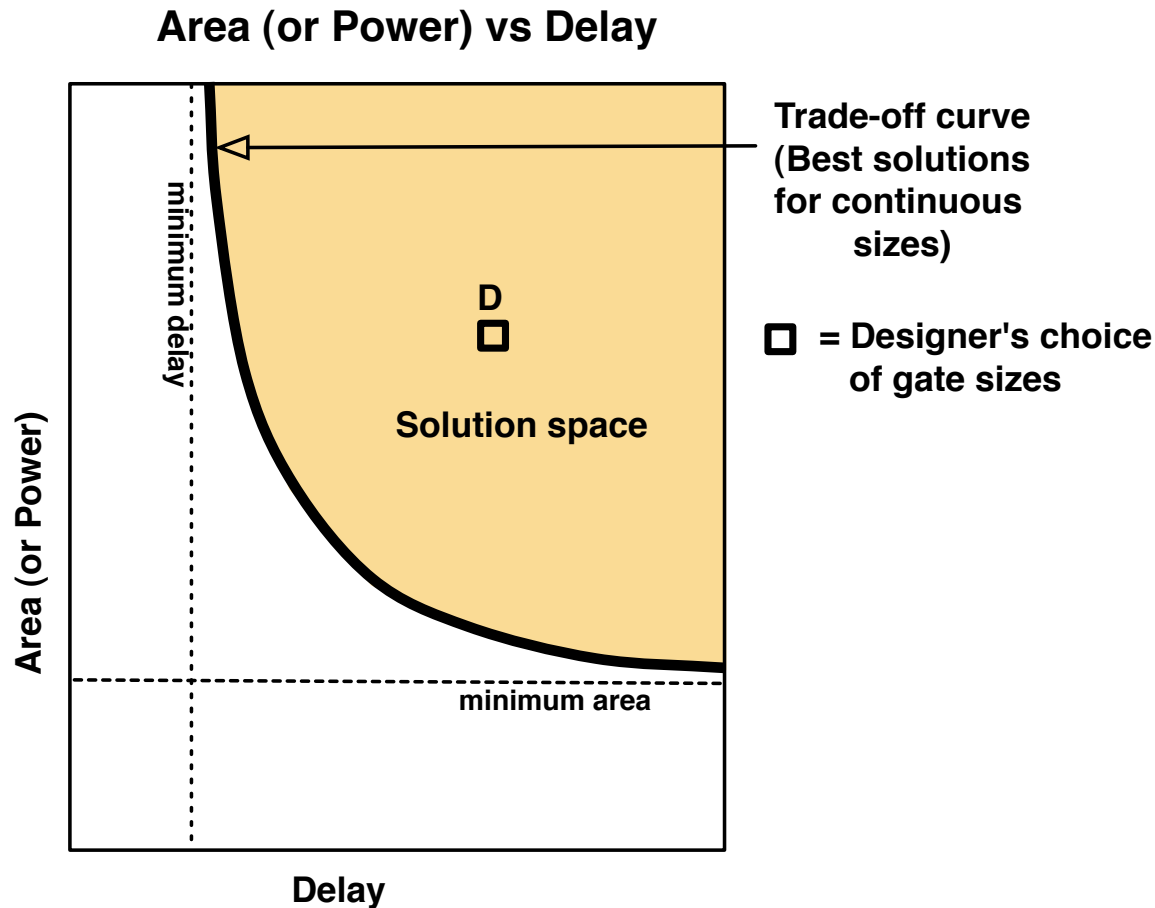
- General circuit design problem: find sizes \underline{x}
- Minimize $\text{Area}(\underline{x})$ or $\text{Power}(\underline{x})$
 - > subject to constraint $\text{Delay}(\underline{x}) < T$



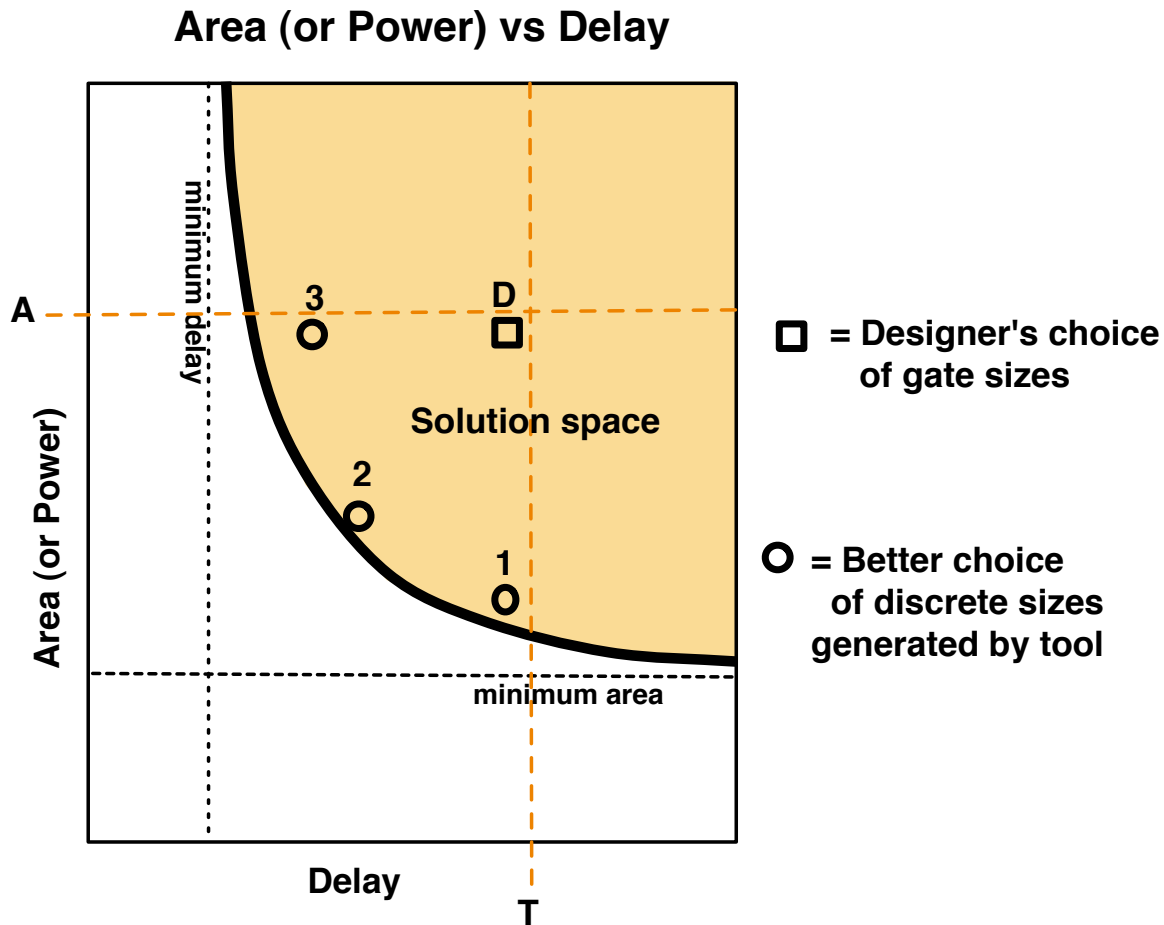
A Solution



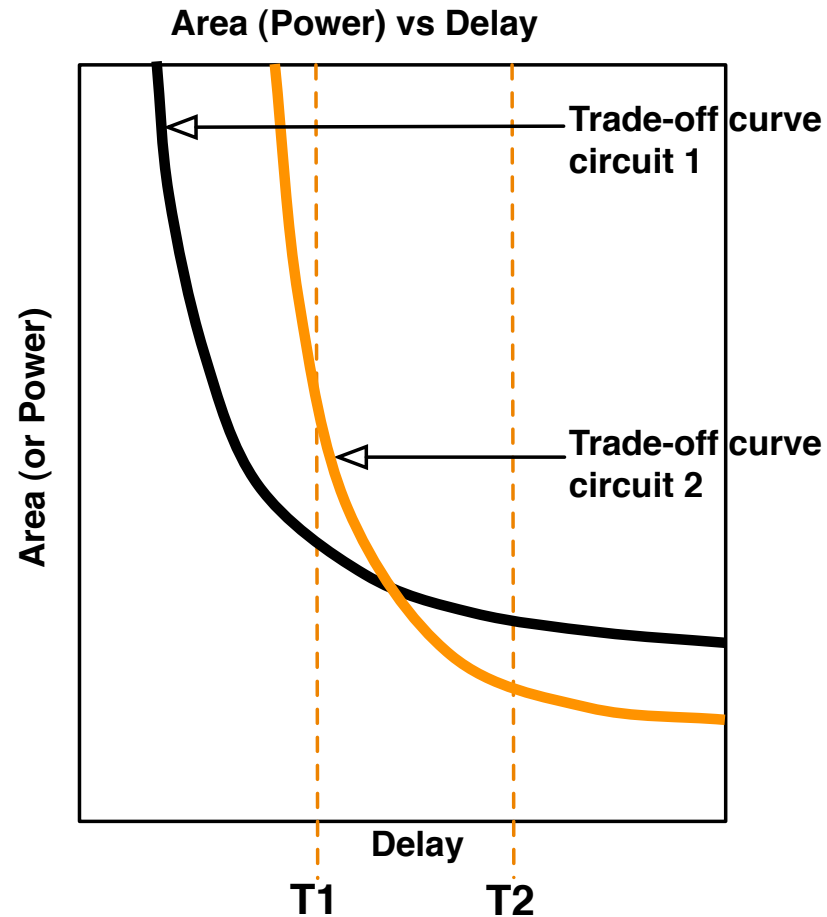
A Solution Space



Optimize Under Constraints

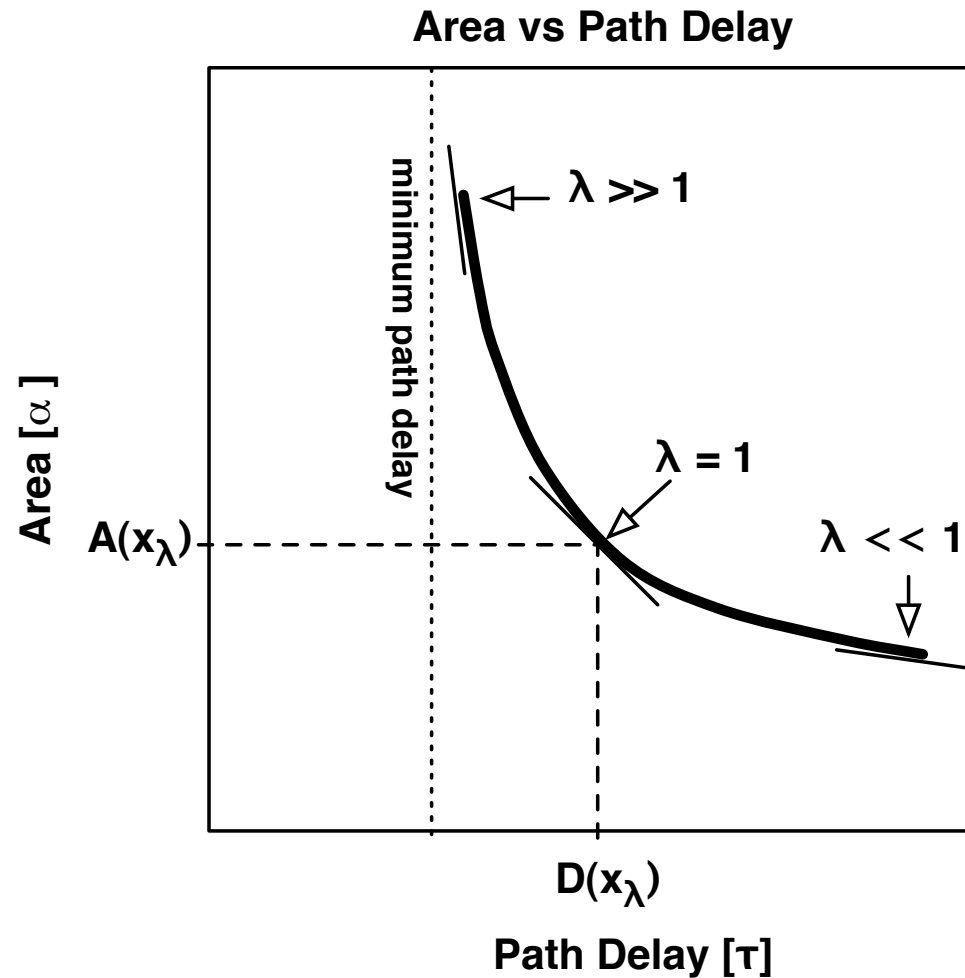


Comparing Circuits



Typical Trade-Off Curve

- Defines costs in terms of trade offs
- -1 unit in delay can be traded for $+\lambda$ units in area



Properties of Trade-Off Curves

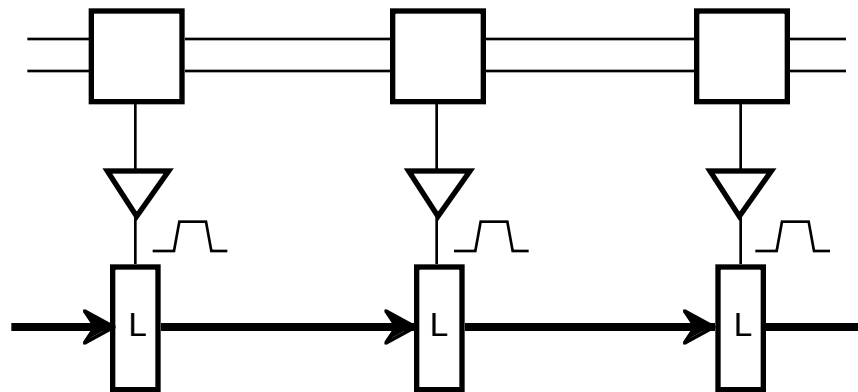
- Trade-off curves offer qualitative and quantitative analysis of a circuit
- Minimal path delay (area, or power) often comes at high cost. (Trade-off cost is high.)

Convex Optimization

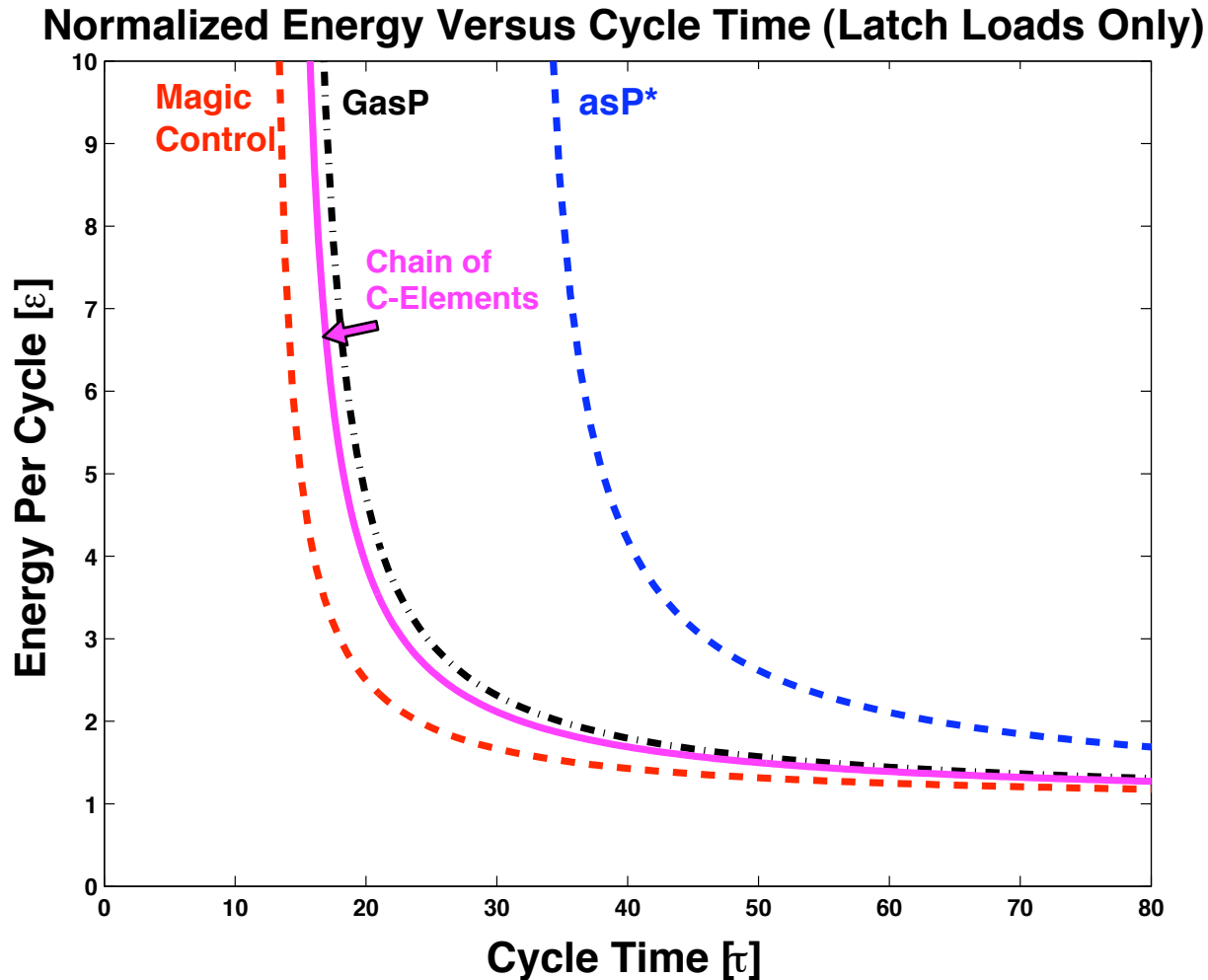
- Generating trade-off curve relies on techniques from convex optimization
- Delay, Area, and Power are convex functions of gate sizes
- New techniques from convex optimization make algorithms scalable

Comparing Circuits

- Asynchronous control of ripple FIFO
- Function: if predecessor is full and successor empty, then move item
- Compare different implementations, assuming all gates have equal delay

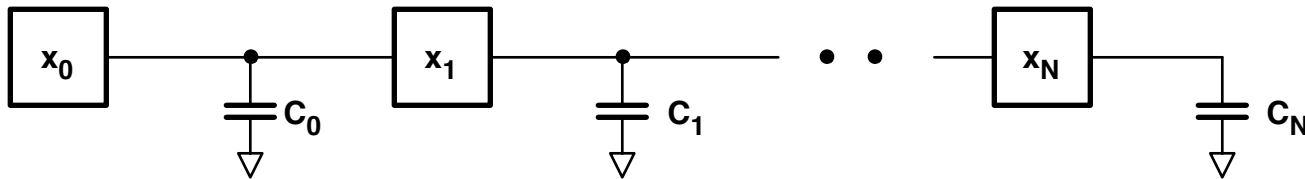


Trade Off Curves



The Single-Path Problem

- A path with delay $D(\underline{x})$ and area $A(\underline{x})$
- Path spends energy $E(\underline{x})$ per activation



- Minimize $A(\underline{x})$, subject to $D(\underline{x}) < D_0$
- Minimize $E(\underline{x})$, subject to $D(\underline{x}) < D_0$
- CAD tool LEO solves this simpler problem

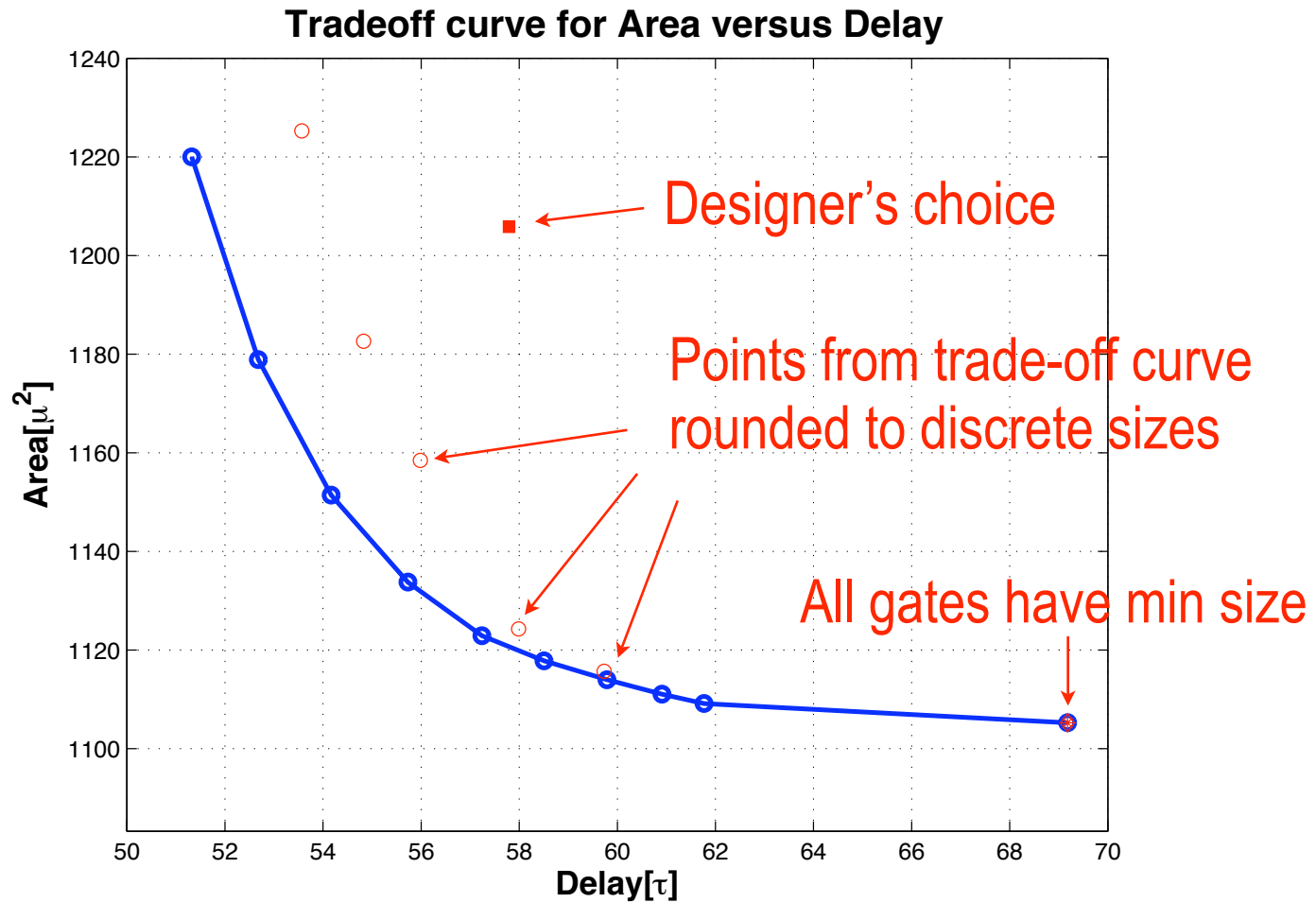
Some Results With LEO

	Min path delay		Designer guess		LEO	
	delay[ps]	area[α]	delay[ps]	area[α]	delay[ps]	area[α]
path 1	89ps	851	102ps	216	107ps	186
path 2	177ps	670	259ps	170	262ps	126
path 3	171ps	923	230ps	269	221ps	192
path 4	97ps	1485	110ps	165	113ps	128

An Example 19-Bit Adder

- Used in ROCK, provided by Ilyas Elkin
- Has approx. 200 gates
- Input drive strength 8x
- Output loads 32x
- Best algorithm (LSGS) generates trade off curve in a few sec's using Matlab
- Algorithm LSGS from Siddharth Joshi and Stephen Boyd (Stanford)

Trade-Off Curve



“It’s the Economy, Stupid”

- Our model is similar to input-output model of an economy
- Moving charges in circuit = moving capital goods in economy
 - > “Gate” = economic sector
 - > “Capacitance” = demand for capital goods
 - > “Drive strength” = supply of capital goods per time unit
 - > “Energy” = total cost of capital goods
- Wassily Leontief (1906 -1999)
- A chip is like an economy



Thank you

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