A Novel MCM Package Enabling Proximity Communication I-O

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Abstract

A novel packaging approach is described that is based on micro-machined features integrated into CMOS chips. Our solution combines two key self-alignment mechanisms for the first time: solder reflow self-alignment and a novel micro-ball and pyramidal pit for passive self-alignment. We report on the demonstration of a MCM package with large footprint semiconductor CMOS chips interconnected by Proximity Communication (PxC), characterization of their high accuracy assembly process, and metrology of the resulting chip misalignment. Our goal is to develop a scalable, lead-free packaging approach by which large NxN PxC-enabled chip arrays are assembled with high precision on organic substrates in a cost effective manner while using industry standard parts and tooling.

Introduction

The world of microelectronics has been enjoying a steady improvement in component performance mainly substantiated by "Moore's Law". Semiconductor processing technology, backed by economical arguments, has continued to arm designers with progressively smaller and denser transistors and on-chip interconnects. As a result, the integrated circuit chips have evolved at continuously fast pace, their complexity and functionality have been dramatically increased leading way to ever-more intricate architectures and systems.

There are, however, growing concerns that such electronic transistor size scaling may prove more challenging to sustain. There are both economic and technological reasons behind it. The latest edition of ITRS [1] lists that manufacturing solutions are not yet available for several key process technologies required to advance memory or CPU fabrication beyond the 28 nm node. With sufficient economic interest these roadblocks are to be timely addressed provided that new exotic materials are pioneered and novel tooling is invented to fabricate further miniaturized transistors that increasingly behave as quantum devices. Additionally, it is becoming nearly cost prohibitive to launch the next generation IC fabrication facility. It is estimated the price tag to build a new most advanced high volume manufacturing factory would exceed $5 billion [2] which amounts to almost 2% of the worldwide semiconductor chip annual revenue. This high expense may slow down the construction of such factories, fabs, and, consequently, the release of the next generation ICs produced by them.

To continue along the performance trends outlined by "Moore's Law" it is, therefore, imperative to not only rely on semiconductor fabrication advances but also put further emphasis on chip packaging technologies. With growing die sizes, I/O counts, and power densities, significant complexities arise in connecting chips to their first-level packages. Along with ongoing developments in 3D integration and multi-chip modules (MCMs) this presents an opportunity for novel I/O technologies that can improve performance despite severe dimensional constraints.

Proximity Communication (PxC) signaling [3] is a type of capacitively coupled-data communication that allows architects to aggregate multiple chips into MCMs to perform as one large piece of Silicon. Further, PxC enables the heterogeneous integration of chip technologies having different process nodes and functionality, such as DRAM, flash memory and processor chips. High-performance multi-chip packages integrating PxC can potentially alleviate I/O bottlenecks in applications requiring higher-bandwidth, lower-power, and lower-latency.

1. Proximity Communication packaging constraints

PxC interconnected channels are formed in the top-most metal layer of interconnected VLSI chips. The chips need accurate face-to-face positioning

(Fig.1) and separation of only a few microns, such that overlapping transceiver circuits communicate with neighbors through capacitive PxC pads. Packaging chips in this way presents several unique and unsolved challenges. For one, the multi-chip package must position and maintain several chips into precise 3D, global alignment reliably.

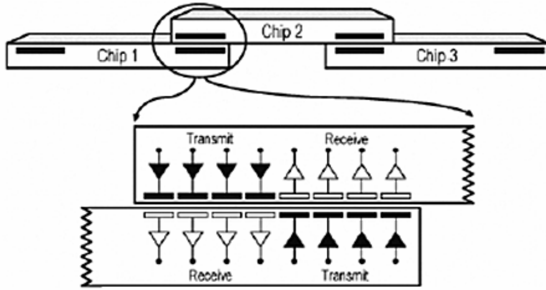

Figure 1. Capacitive proximity communication (PxC) between three face-to-face chips [4].

As opposed to solder bumps or wire bonds, capacitively coupled interconnection is established wirelessly and without the specific need for permanent chip-to-chip attachment. Therefore, such an interconnect facilitates MCM package diagnostics and rework, if necessary, as non-functional die may be separated from functional ones, *i.e.* identifying known good die (KGD), which is key to enhancing assembly yield.

Experimental measurements indicate that for any particular choice of pad size on PxC provisioned chips, an X-, Y-, and Z- chip-to-chip alignment of less than 1/3 of a pad pitch, or 8 μm for 24 μm pads in our case, must be established in order to couple a transmitter strongly to its matching receiver and keep the signal above the noise level and avoid cross-talk. This type of chip-to-chip alignment accuracy could be achieved and maintained with a low volume state-of-the-art flip chip bonder if three chips are all aligned and permanently attached to each other prior to soldering to the package substrate.

In an earlier MCM PxC package demonstration described in [5] three such permanently glued chips formed silicon subassemblies nearly 40 mm long which would not readily conform to the non-planar organic substrate during the C4 array reflow which correspondingly deteriorates the next level interconnect yield. State of the art flip chip bonding equipment was employed in their approach as chip alignment, attach and assembly to a substrate have to comply with micron scale alignment tolerances as specified above. The high accuracy and tight tolerance alignment demanded by proximity communication are not attainable with conventional pick-and-place tooling, which adversely affects assembly throughput. Also, due to a large CTE mismatch between the glued sizeable multi-chip silicon subassembly and the organic substrate the reflowed 180 μm pitch C4 solder ball connections were prone to bridging.

Such MCM packages with permanently attached to each other chips carry a high potential for reliability failure due to large thermo-mechanical stresses developed during assembly or operation. The stresses can cause fracture of the glued chips or delamination of the thin intrachip bond line that determines the vertical chip separation. The latter may cause degradation of the PxC signal integrity if the separation exceeds the 8 μm margin. The assembly tolerances and built-in stresses can become ultimately unmanageable when large scale two-dimensional PxC chip arrays are envisioned. This necessitates novel packaging solutions that can retain the chips in alignment, provide adequate power to all chips in the array, and dissipate heat from such a tightly packed module.

2. PxC MCM packaging approach

2.1 Package description

In order to accurately position PxC interfaced VLSI chips and reliably package them into a large area high performance 2D array we developed a glue-free packaging approach based on two self-alignment mechanisms: the first relies on self-orientation of the island dies by solder reflow, the second relies on the micro-ball and pit self-steering of the bridge chip into a designed location. Our PxC package demonstration is a MCM prototype with two large area *"island"* (15.1x12.2 mm^2) chips that are to be PxC interconnected with each other through a third, *"bridge"*, chip forming a linear 1x3 array. Figure 2 schematically depicts the parts involved in the described 1x3 array demonstration along with the two designated PxC areas to overlap.

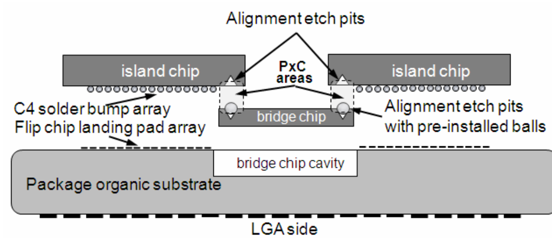

Figure 2. Cross-sectional schematic view of the components comprising PxC package.

All chips have been fabricated in 0.18µm CMOS carrying 144 capacitive PxC channels designed to operate at 1.8 Gb/s per channel thereby providing an unprecedented bandwidth density of 430 Gb/s/mm^2 [4].

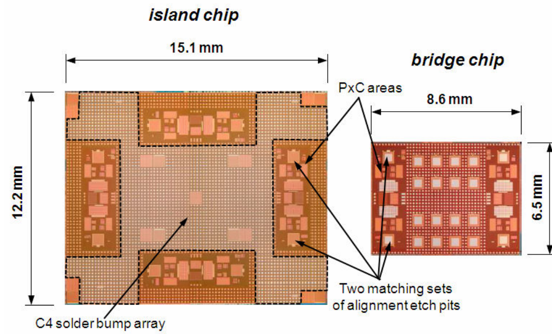

Figure 3. Top view of packaged VLSI chips, island and bridge, with their respective dimensions and layout.

The layout and dimensions of the island and bridge chips are shown in Fig. 3 along with dedicated areas for PxC channels and alignment etch pits. The island chip was designed to be PxC accessed or *bridged* from four different sides. There are a total of four PxC areas on the island chip corresponding to each of its edges and two opposing PxC areas on the bridge chip which allows for a matrix of interconnected island chips to be configured. Only one island chip edge PxC area is utilized in this demonstration. The PxC area also contains position detection circuitry, which electronically measures the alignment between the bridge chip and the two island chips. Each of these island chips is populated with 2512 C4 solder balls of 100 µm diameter arrayed on a 180x180 µm^2 pitch (inside the dashed highlighted area).

As indicated both island and bridge chips are provisioned to accommodate dedicated alignment features. These are etch pits fabricated in a post-CMOS manufacturing environment. Their CMOS compatible processing details and achievable micromachined feature accuracy could be found in [6]. Owing to the tight tolerances of the photolithographic patterning and high etch anisotropy these micromachined pits in silicon are precisely formed in PxC overlapping regions of island and bridge chips. There are two matching sets of pits per PxC interconnected interface. To enable etch pits self-steering functionality they are populated with sapphire micro-balls with sphericity and diameter tolerances less than a micron. Figures 4 shows an example of the etch pit and micro-ball integration into a commercial CMOS IC. The pits and micro-spheres are appropriately sized for aligned packaging to minimize chip-to-chip vertical separation as well as lateral walk-off [6-8]. The etch pits with 200µm X 200µm top opening and 100 µm depth were paired with 176 µm diameter sapphire balls to ensure accurate alignment without vertical separation between the facing chips.

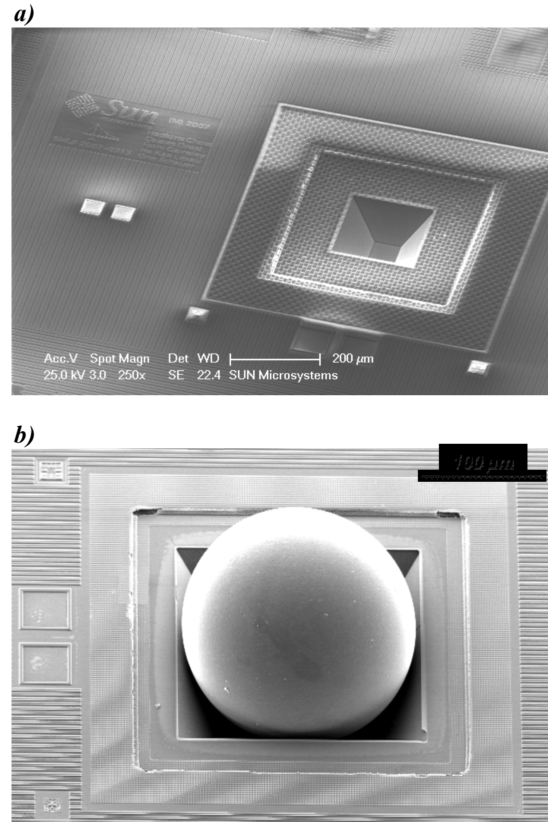

Figure 4. Highly accurate and reproducible etch pit alignment features integrated into CMOS back-end: (a) fragment of the VLSI chip with fully micromachined etch pit, (b) etch pit housing a high precision sapphire micro-ball.

A large MCM organic substrate (45mm x 45mm x 1.34mm) was designed to carry sites for two island flip chip bonds, with 2512 C4 pads each on a 180x180 µm^2 pitch, separated by a 8.8x6.7mm^2 cavity sized to house an appropriately thinned bridge chip (Fig.5). The opposite socket side is a LGA on 1 mm pitch. The substrate is built using 5-2-5 organic laminate process with copper traces. The core and each build-up layer are 800 µm and 30 µm thick, respectively. The cavity is created by patterning the top 5 build-up layers to yield a cavity depth of 250 µm from the flip chip pads to the Cu surface on the bottom of the cavity. Figure 5 (top) displays the chip attach side of the package substrate with the respective sites for two island

chips and a cavity for a bridge chip. Twenty three wirebond pads that are used to power up the bridge chip are also identified in the Figure.

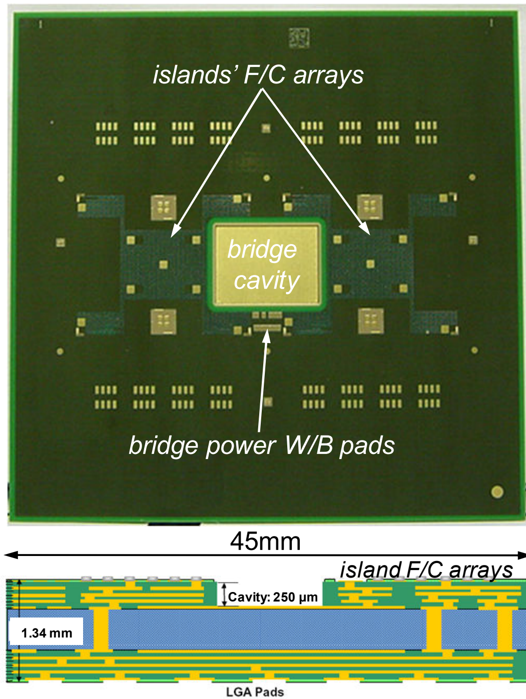

Figure 5. Top and cross-sectional view of the organic substrate with a cavity for MCM PxC package.

The substrates were characterized for global and local flatness as well as lateral positions of most of the 5024 flip chip landing pads. The substrate warpage averaged less than 30 µm across the two landing pad array sites with the central cavity residing below the island's flip chip arrays. We intend to conventionally solder attach both island chips simultaneously to the organic substrate in a single reflow step. As discussed previously, due to the large overall three PxC chip footprint relative to the substrate it is prudent to keep chips physically unconstrained by one another. As both island chips are reflow bonded to the substrate at elevated temperature, the solder surface tension will pull chips to the positions of their respective flip chip landing pad arrays on the organic substrate. As such, the final position and orientation of the island chips relative to each other are governed in large part by the position and orientation of the flip chip landing pad arrays on the organic substrate. By design the island chips have to be spaced from each other such that the distance between their edge PxC areas is exactly equal to the span between PxC areas on the bridge chip (Fig. 2). As the assembly relies on solder self-alignment it is important to establish whether the organic substrates and their flip chip solder landing pad arrays are fabricated with sufficient precision to ensure that island chips are appropriately spaced.

We have custom built a dedicated metrology system that combines a high magnification microscope with sub-micron accuracy motion stage and computer controlled pattern recognition capability. This system was programmed to recognize individual landing pads and identify their X- and Y- locations. Each substrate's flip chip arrays positions have been accordingly mapped out and statistically compared to their respective designed CAD values.

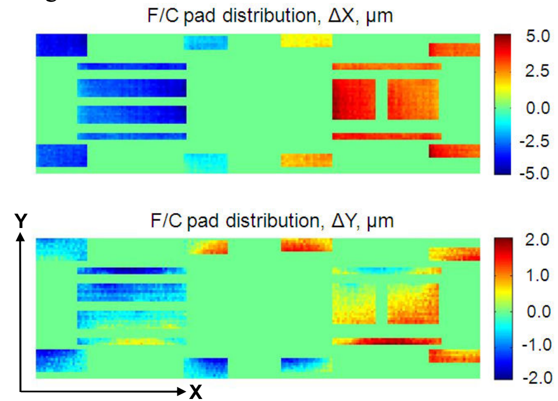

Figure 6. A typical color map of the MCM PxC organic substrate representing each flip chip pad location with respect to the designed CAD value in X- and Y- direction.

As a result we deduced the separation of the centroid of one island chip landing pad array to the centroid of the other island chip landing pad array. The deviation of this measured distance from the designed target, or registration error, was averaged over several tens of characterized substrates from different lots and amounted to 4 µm with less than 2 µm of standard deviation in X- direction, including the measurement error. Such registration error in Y- direction did not exceed 1 µm. Two flip chip bonded island chips are expected to be laterally solder self-aligned to comparable accuracy even if their initial placement is limited to pick-and-place tooling accuracy of +/-25 µm (~1/3 pad size), which is commonly met by the packaging industry.

Figure 6 displays the colored maps of the island chip landing pad arrays from one the inspected substrates. To give a better perspective, the overall center to center distance between left and right island flip chip landing pad arrays is 18.12 mm by design. The measured 4 µm walk-off on the manufactured substrate constitutes only ~0.02% error which is far below the typical

specified tolerances warranted by an organic substrate vendor. No special efforts were made to minimize registration errors or substrate warpage. It is concluded therefore that typical organic substrates are manufactured with sufficient accuracy to allow PxC MCM packaging. Ceramic substrates of identical layout and size as the described organic substrates were also characterized. Their dimensional accuracy or registration error as well as warpage across the top surface were found to exceed the tight specifications imposed by PxC MCM packaging requirements.

2.2 PxC package assembly

The package assembly begins with wafer level bridge chip thinning down to 150 µm from the original thickness of 725 µm in order to fit it into the substrate's cavity. Each of the bridge chip's four etch pits, with a 200 µm by 200 µm top opening and 100 µm depth, is populated with 176 µm diameter sapphire micro-balls. Three or even two micro-balls might be sufficient to properly orient and align bridge chip with respect to its PxC mating islands later in the process. The exact relationship of the number of micro-balls and the degree of ultimate repeatable alignment will be explored in future experiments. Installing and securing the micro-balls in the chip's etch pits is a wafer level compatible procedure with tooling similar to a solder bump transfer process. Once populated, the bridge chip is placed into the substrate cavity face up (Fig. 7a).

In the next step, two pitted and bumped (100 µm diameter Sn60/Pb40 bumps have been wafer processed after etch pits were completed) island chips are flipped, aligned and positioned onto their fluxed respective flip chip landing pad arrays (Fig. 7b, c).

At this point, the bridge chip with its protruding micro-balls resides in the cavity with over 50 µm of clearance not interfering with island chips' surfaces and their freedom to move. The island chip positioning was carried out by a flip chip bonder with a rated placement accuracy of +/- 5 µm. This could also be achieved with a lower grade high throughput pick-and-place tool (+/-25 µm tolerance) as the ultimate island alignment is provided by solder self-alignment and governed by substrate's smaller registration errors. The package is then exposed to a modified solder reflow profile.

As emphasized previously we rely on the remarkable feature of the solder flip chip interconnect to self-align. The driving force for self-alignment is surface tension that minimizes molten solder surface area for a given volume. The surface tension is balanced by the internal pressure of the solder.

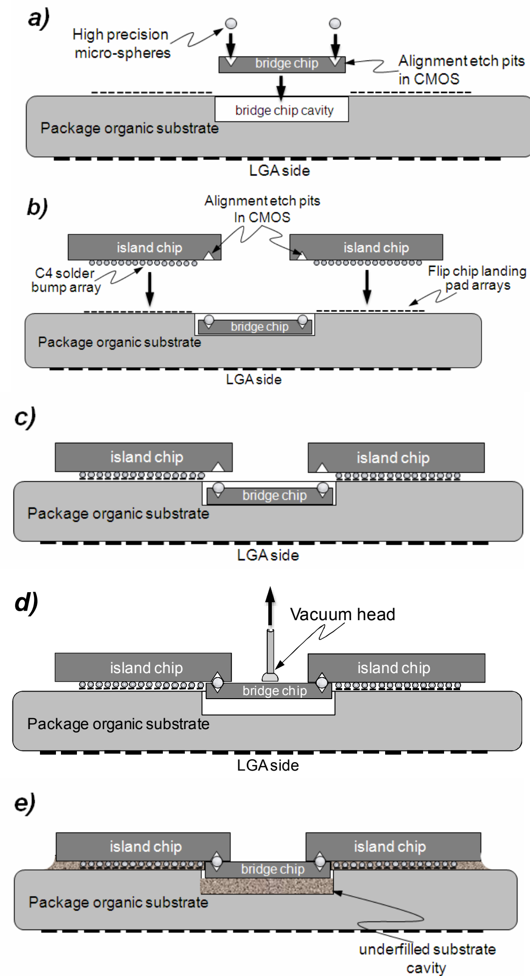

Figure 7. PxC MCM package assembly flow.

Any distortion from the minimal surface area spherical shape would create a restoring force that again is approximately proportional to the additional created surface area which diminishes rapidly as alignment is restored. Solder self-align accuracies down to 0.1 µm has been demonstrated [9]. We have extended reflow profile at the wetting stage from standard 90 seconds to several minutes to allow additional time for the island chips to move into their aligned positions preset by the substrate.

After solder reflow, the cooled down package is placed back onto a pick-and-place tool with a vacuum head. The bridge chip is picked up by the vacuum head in its cavity and lifted up to the level of the island chips. The bridge chip has to be initially coarsely aligned to either island chip within half the ball diameter, or about ~85 µm; then the

bridge's micro-balls capture the opposing island's etch pits and center the micro-ball into the opposing pit potentially bringing the bridge into micrometer-scale alignment (Fig. 5d) [6-8]. In fact the substrate's cavity could be specified to be oversized laterally by half the micro-ball diameter in all directions relative to the bridge chip. With such an appropriately sized cavity the bridge chip would be immediately coarsely aligned once placed into it. In this scenario, no additional active alignment is necessary as the bridge would be auto-steered by the micro-ball and etch pit as it is lifted all the way up till the hard stop provided by the attached island chips or when the substrate is consequently elevated by the bridge chip. In our case, the cavity was made too large for coarse alignment to work right away so little active alignment guided by provisioned visual alignment marks while zeroing or minimizing the separation between the facing chips was necessary. After final accurate bridge to island alignment was established with micro-balls and pits the bridge was temporarily tacked to the island with an instant adhesive in order to lock it in place for further remaining steps.

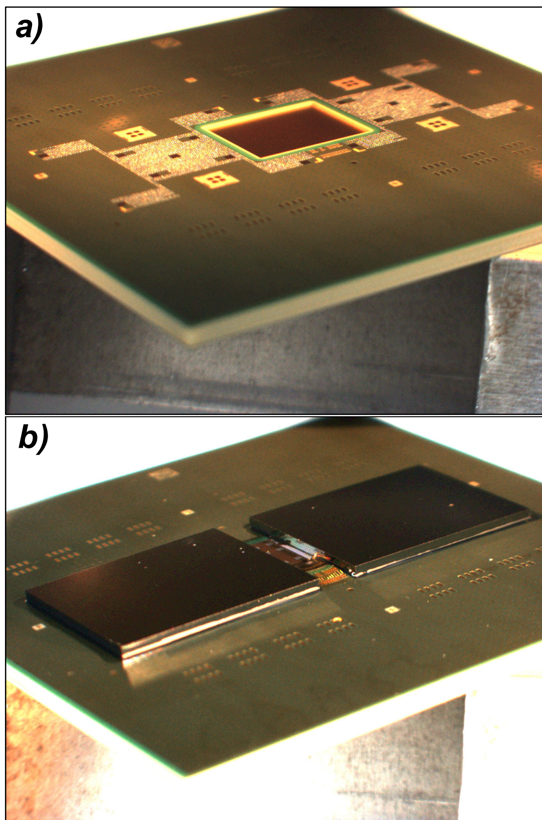

Figure 8. PxC MCM organic substrate (a) before and (b) after the package assembly.

The island chips and the cavity under the suspended bridge chip were then underfilled. After the underfill step, the bridge chip is reliably secured in the properly aligned position with established PxC interfaces (Fig. 7e). Wirebonding from the substrate to the bridge was conducted to provide the bridge chip with power, which finalized the packaging.

Figure 8 shows PxC MCM package before and after chip alignment and completed assembly. There is a close-up of the PxC areas between aligned packaged chips in Figure 9.

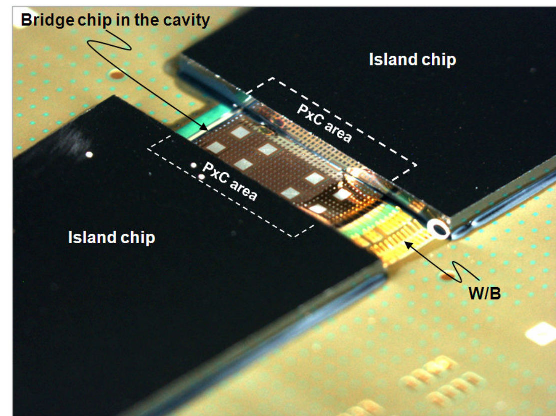

Figure 9. A central fragment of the package displaying respective PxC areas.

3. PxC MCM package metrology

The alignment of the chips in the assembled packages has been characterized with optical and electrical tests. Each chip, islands and bridge, was provisioned with sets of reference features fabricated in the CMOS stack-up. These features are designed to be clearly viewed either through the front side or the back side of the chip. The latter could be attempted with an infrared (IR) capable camera. The relative position of these reference features could be quantified and directly indicate how well the bridge and island chips are aligned with respect to each other.

Figure 10 displays the reference features inspected at four different bridge and island overlapping points. In these images, the camera is focused onto the bridge reference (the lighter frame) while the darker references (cross and four corner blocks), are situated on the island chips. The chip separation could be inferred by moving the camera focus on one chip's reference or another and noting the relative height change in associated objective lens movement. This, however, is not a very accurate approach due to uncertainty in the

working range and diffraction of the IR optics caused by IR light propagating through multiple layers of metal and dielectrics in the CMOS stack up. So while lateral misalignment of one chip with respect to another could be inferred with ~1.5μm accuracy, it could only be concluded with visual means whether or not the vertical chip separation is under 10 μm. This is sufficient to establish whether this reported packaging technique is applicable for PxC applications.

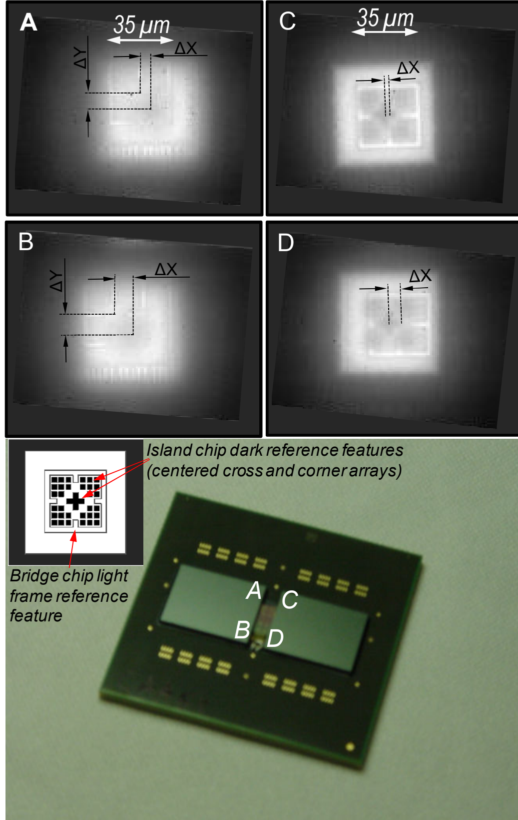

Figure 10. Images of the reference features captured in the infrared range displaying relative island and bridge relative misalignment, ΔX and ΔY, at corresponding A, B, C and D points of their PxC overlap. The IR camera is focused onto the lighter frame of the bridge chip's reference mark; the island chip's darker reference mark appears blurry if chips are not in immediate contact and there is a certain several micron separation, ΔZ, between them. The inset image shows a schematic of the superimposed reference features of aligned bridge and island chips.

The bridge chip powered up and received JTAG commands through wirebonds with the substrate. As mentioned earlier, the PxC area of our VLSI chips also carries position detection circuitry, based on Vernier scale capacitive elements, which electronically measure the alignment between the bridge chip and the two island chips.

Table 1. Summary of the packaged bridge and islands positional alignment.

	ΔX, μm	ΔY, μm	ΔZ, μm
IR optical measurements			
A, B	7.9	7.1	<10
C, D	3.8	4.0	<10
Electrical measurements			
A, B	6	5	<5
C, D	DNM*	DNM*	DNM*

* did not measure.

Table 1 contains a statistical average of chip to chip, bridge to island, relative positioning averaged over several PxC MCM packages built with the described assembly technique as measured by both the electrical and optical means. All of the measured packages have been misaligned remarkably by less than 8 μm in X- and Y-direction with vertical separation not exceeding 10 μm or less which is to be verified by direct package cross-sectioning. It clearly indicates the packages meet the strict PxC alignment specifications of high-fidelity signaling with low bit-error rates [10].

Conclusions

Capacitively coupled communication enables high-bandwidth, low-power, and low-latency chip-to-chip I/O capabilities in high performance multi-chip modules. We reported on an assembly technique that addresses the demanding specifications imposed on packaging by PxC requirements. We showed chips in the PxC MCM packages could be aligned within 8 μm in three degrees of freedom allowing high fidelity signaling.

The described packaging approach is a glue-free assembly that does not constrain the chips mechanically but maintains their mutual state of specified alignment. This enables PxC communication and allows them all to seamlessly function as a single large piece of silicon. Such packaging could be extended to aggregate multiple proximity communicating chips that function as one oversized chip with an overall area far larger than the current reticle-limited maximum area single chip in the modern semiconductor foundry.

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