Grating-coupler based low-loss optical interlayer coupling

Jin Yao, Xuezhe Zheng, Guoliang Li, Ivan Shubin, Hiren Thacker, Ying Luo, Kannan Raj, John E. Cunningham, and Ashok V. Krishnamoorthy
Oracle Labs, Oracle, San Diego CA 92121

Abstract: Optical interlayer couplers with 2.8dB insertion loss and 48nm bandwidth were designed and demonstrated in a commercial 130nm SOI CMOS process. 10Gb/s transmission through an interlayer-coupled link showed a power penalty of <0.1dB.

1. Introduction

Silicon photonics has emerged as a promising enabling solution to interconnects within future large scale computing systems owing to its advantages of high density, large bandwidth, and low communication latency. Various network architectures have been proposed [1-3] for photonically interconnected many-core systems. One of the challenges to implement these relatively complex networks using just one photonic layer is waveguide crossings. Although special structures can be used to alleviate the loss and crosstalk penalty[1,2], the scaling of these interconnect networks will still be significantly limited by the waveguide crossings due to the accumulated loss and crosstalk in the WDM links. Another approach, therefore, is to use waveguides in two separate layers and use inter-layer couplers to eliminate waveguide crossings completely [3]. In this approach, dual-layer couplers route the optical signal the same way as the electrical signal: optical signals propagate in waveguides without crossing each other. The inter-layer couplers connect optical waveguides in different layers akin to vias for electrical routing. Thus a large-scale point-to-point optical interconnect network can be realized [4].

Therefore chip-to-chip, inter-layer couplers with low loss, large bandwidth, small footprint and integration compatibility are highly desirable. Optical proximity couplers (OPxCs) for interlayer coupling have been reported previously using reflecting mirrors on silicon waveguides [5-7]. A pair of such tilted reflecting mirrors can be fabricated to form smooth <111> crystal plane and then coated with metal to change the direction of optical propagation to interconnect two chips. With WDM technology, this approach can achieve high data transmission density, large bandwidth and facet-to-facet loss as low as 2.7 dB [7]. However, so far the demonstrated reflecting mirrors were fabricated either by anisotropic hydroxide etching on ~10 μm-thick silicon active layer; or with epitaxially grown 3-dimensional tapers to ~10μm to construct the OPxC structures. Since many Si photonic devices (modulators, mux/demux, etc) need to be fabricated with thinner waveguides (200-500 nm) in order to achieve small footprint and low power consumption, it is desirable to develop OPxC devices compatible with these small waveguides.

Grating couplers (GCs) have been demonstrated to couple light between the optical fiber and the SOI chip [8]. In this paper, we report on the design and fabrication of GCs to enable the optical interlayer coupling in a commercial 130nm SOI CMOS platform. Compared to the optical proximity coupling approach based on the reflecting mirrors, the developed interlayer grating coupler avoids the need for millimeter long 3-dimensional waveguide tapers and a thick silicon active layer. It is a fully CMOS compatible device with substantially reduced footprint. Compared to previous proof-of-concept demonstration using GCs with pigtailed fibers in [9], we have designed and improved both the loss performance from 4dB to 2.8dB and the alignment tolerance substantially by optimizing the GC structure for a larger mode size.

2. Design and experimental results

The concept of the grating coupler based OPxC is illustrated in Figure 1. To achieve coupling of optical signals between two layers, two chips with grating couplers are placed face-to-face and in close proximity. When the grating couplers from each chip are appropriately aligned, light from the waveguide on one chip can be coupled onto the waveguide on the other chip.

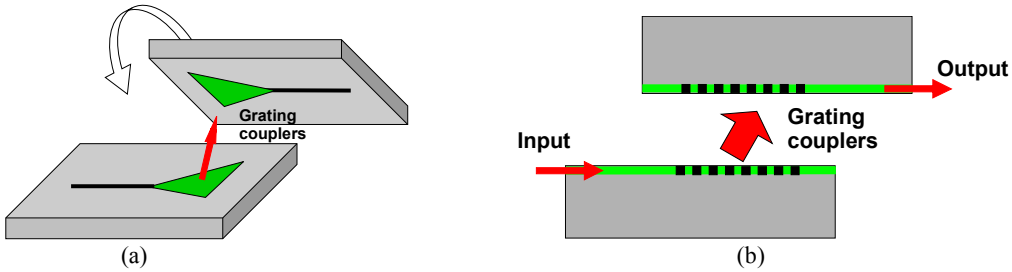

Figure 1. GC-based interlayer coupling structure: (a) Two SOI chips are placed face to face, interconnected by the optical coupling between the two grating couplers. (b) Corresponding cross-sectional view.

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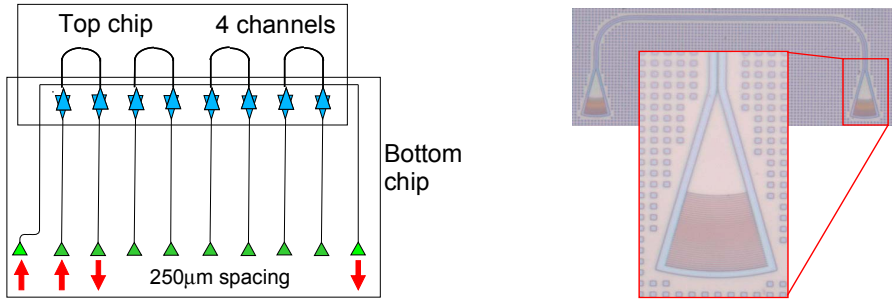
The GC structures were designed and optimized using 2-D FDTD modeling. Each GC has a triangular shape about 25 μm wide and 40 μm long, as shown in Figure 2. The grating period is apodized to form better mode matching along the optical propagation direction. The first period at the waveguide end starts at 586 nm, and has a trench of 120 nm. The grating couplers with the connecting waveguides were fabricated on SOI wafers using the Luxtera optoelectronic process integrated in Freescale's HIP7 130nm SOI CMOS technology [10].

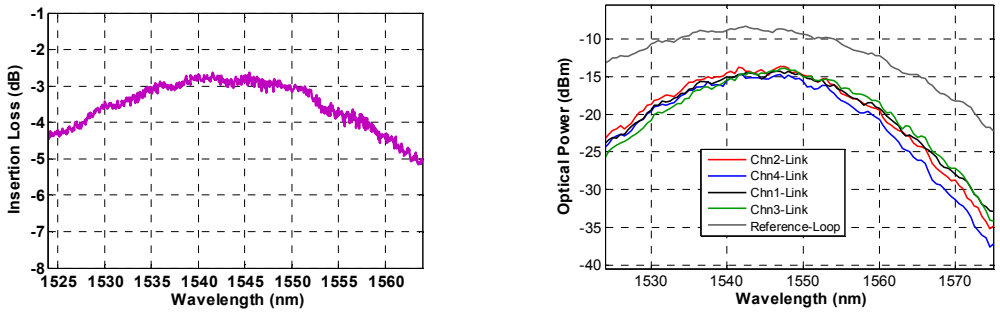
To facilitate chip-to-chip interlayer coupler testing, Figure. 2 shows that each of the OPxC grating coupler on the bottom chip was connected to a waveguide and terminated with a grating coupler to couple to a standard single mode fiber. The grating couplers on the top chip were connected as loops. With all the grating couplers spaced at 250 μm, 8 grating couplers on the top chip were paired to form a 4-channel interlayer coupler array. The first and last grating coupler on the bottom chip for the fiber interface were designed to form a reference loop for the fiber array alignment. By aligning the fiber array to these two edge grating couplers using six-axis alignment stages, we obtained alignment between the other input/output fibers and their corresponding interlayer couper channels. Using on-chip alignment markers for coarse initial positioning, the two chips were then aligned by injecting light to the input of the interlayer channel, and maximizing the output light received from the corresponding output channel.



(a) (b)

Figure 2. Testing structures and loops for interlayer grating couplers.(a)Top and bottom chips with aligned structures. (b)A fabricated grating coupler loop in the top chip and optical micrograph of the GC.

Total optical loss from the input fiber to the output fiber was measured, which included two interlayer coupling losses and two coupling losses from the grating couplers to the fibers. In order to calibrate out the loss attributed to other parts of the link, the loss of the reference loop was measured and subtracted as it contained two input/output losses from the grating coupler to the fiber and the waveguide loss. The waveguide loss difference between the reference loop and the channel loop due to the length difference was less than 0.1 dB. Figure. 3(a) shows a measured optical transmission spectrum of the OPxC hop after calibration. The minimum loss is 2.8 dB around 1543nm wavelength, with a 3 dB optical bandwidth of 48 nm. The measured 4-channel spectra with the reference are shown in Figure. 3(b), demonstrating good loss uniformity across all 4 channels.



(a) (b)

Figure 3. (a) Interlayer coupling spectrum of the measured OPxC loss (b)Measured 4-channel spectra with the reference loop.

In order to verify the performance impact on high speed data transmission, we have further tested the two-chip OPxC link for data transmission at 10 Gbps data rate using a set of off-the-shelf optical transmitter (Tx) and receiver (Rx). Figure 4 shows the receiver sensitivity plots for both the transmitter/receiver in a back-to-back configuration and through the two-hop OPxC configuration. The power penalty at the receiver after the OPxC hops was measured to be less than 0.1 dB at a BER of 10^{-9}. This indicates that the OPxC hop causes negligible signal distortion and confirms the high fidelity of the photonic link.

Alignment tolerances of the grating coupler were also measured with results shown in Fig. 5. The X-direction

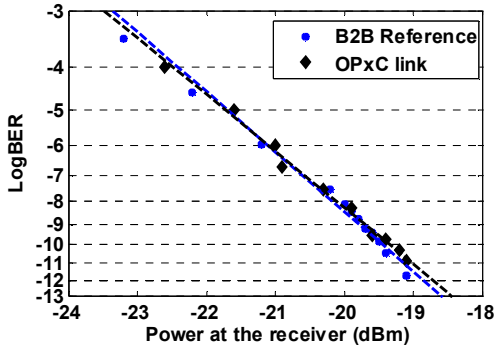
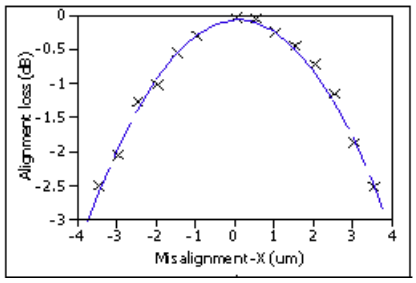
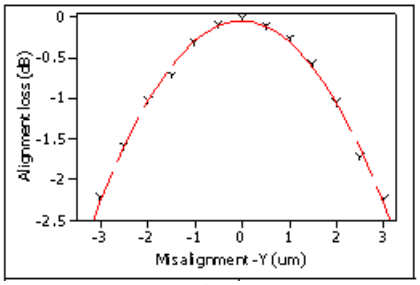


Figure 4. Power penalty measurements for high speed transmission of the OPxC link with two interlayer hops.

tolerance (along the waveguide direction) is shown in Fig. 5(a); and the Y-direction tolerance (perpendicular to the waveguide direction) is shown in Fig. 5(b). As seen from the results, a 2-μm misalignment accuracy causes around 1 dB excess loss in both X- and Y- directions. This tolerance is better than the results in [9], attributed to the optimized GC design with larger mode size compared to the GCs in [9]. Using FDTD simulation, we further found that a significant part of the optical loss is from scattering to the substrate. We believe the loss performance of the GC interlayer couplers can be further improved by implementing a mirror structure at the backside of the couplers.



(a)



(b)

Figure 5. Measured alignment tolerances of the grating coupler based OPxC. (a) X-direction tolerance (along the waveguide direction), and (b) Y-direction tolerances (perpendicular to the waveguide direction).

3. Conclusion

We have designed and demonstrated optical interlayer coupling using grating couplers, for high performance silicon photonic interconnects. The grating couplers and the connecting waveguides were fabricated on a SOI wafer using a commercial 130nm CMOS process. Chip-to-chip interlayer coupling in four OPxC channels were tested with 2.8 dB coupling loss and 48 nm 3dB bandwidth with good uniformity. Less than 0.1 dB power penalty for 10Gbps data transmission demonstrated that the photonic link using GC-based OPxCs has low signal impairment. This interlayer coupling has the potential to be used in high density WDM interconnects for intra/inter-chip applications. Low cost and dense integration can be achieved leveraging existing CMOS fabrication infrastructures. This work is supported in part by DARPA under Agreements HR0011-08-09-0001 and W911NF-07-1-0529. The views expressed are those of the authors and do not reflect the official policy or position of the Department of Defense or the U.S. Government. Approved for Public Release, Distribution Unlimited.

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