Non-Volatile Memory and Java

A series of short articles about the impact of non-volatile memory (NVM) on the Java platform.

Part 1: Introducing NVM

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Non-volatile RAM (NVRAM) has arrived into the computing mainstream. This development is likely to be highly disruptive: it will change the economics of the memory hierarchy by providing a new, intermediate level between DRAM and flash, but fully exploiting the new technology will require widespread changes in how we architect and write software. Despite this, there is surprisingly little awareness on the part of programmers (and their management) of the technology and its likely impact, and relatively little activity in academia (compared to the magnitude of the paradigm shift) in developing techniques and tools which programmers will need to respond to the change.

In this series I will discuss the possible impact of NVRAM on the Java ecosystem. Java is the most widely used programming language: there are millions of Java developers and billions of lines of Java code in daily use.

I'll start by describing the coming Intel hardware and its software interface. Next I'll go into the consequences of this combination on software, entailing both opportunities and challenges. After that I'll get into the specifics of how Java may be impacted, the choices facing the platform in addressing the technology and how those choices have been resolved in proposals to date. Finally, I'll describe some ideas I've been pursuing at Oracle Labs and explain the rationale behind those choices.

I'll try to keep this accessible to typical Java programmers (and their managers) by explaining concepts and terms as necessary.

Introduction

For as long as most people can remember, computers have lost the content of main memory when power is removed.[1] However, that is about to change. Intel has just released Non-Volatile DIMMs (NV-DIMM), under the brand *Optane DC Persistent Memory*. The underlying circuit technology is known by the brand *3D XPoint*. SSDs using 3D XPoint chips have been shipping since mid-2017, and now computers are available with these devices attached as NVRAM. Many other companies are also working towards similar goals and we can expect there to be a variety of competing

[1] Before semiconductor memory there was ferrite core storage, which was also non-volatile, although I don't know if anyone exploited this property, or, if so, how.

technologies and products appearing in the coming years. However, Intel's entry into the field has given it new legitimacy and importance.

What we know about Intel's hardware[2]

Many details about the technology developed by Intel and Micron (Intel's technology partner[3]) are yet to emerge. As of this writing, the details below are based mostly on Intel statements; I have not yet obtained access to a working system.

In addition to byte-addressability and non-volatility:

1. *Memory density* is significantly higher than DRAM. Initial Persistent Memory Module (PMM) sizes are 128, 256 and 512GB[4] using 128Gb dies[5]; in comparison, the largest DRAM DIMM is currently 256GB using 16Gb dies[6].
2. *Cost/bit* is expected to be significantly lower than DRAM, although (initially, at least) significantly higher than flash (I haven't seen any street prices yet).
3. *Read and write latencies* will be higher than DRAM, but within an order of magnitude and hence much lower (by several orders of magnitude) than flash. I haven't seen any figures from Intel, but a new study from UCSD[7] confirms thIs: they measure random read latency at around 300ns (compared to around 80ns for DRAM) and sequential read latency of around 170ns. Write latencies are closer: 94ns for Optance vs 86ns for DRAM (more on this later).
4. *Read bandwidth* peaks at about one-third that of DRAM, while write bandwidth is about a sixth that of DRAM.
5. *Endurance* is expected to be much higher than flash, although how close to DRAM we don't yet know — Intel has not released any official endurance figures.

Early marketing claimed Optane would have 1000 times the speed (which I take to mean reciprocal media latency) and endurance of flash[8], at 8–10x DRAM density[9]. Because of the higher latency (and perhaps lesser endurance) than DRAM, systems using Optane will still contain DRAM. New systems capable of supporting NVRAM have also been released.[10]

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[2] All information in this document was gleaned from public sources.

[3] For now; https://www.theregister.co.uk/2018/07/18/3d_xpoint_issues_and_micron_intel_split/

[4] https://www.realworldtech.com/intels-3dxp-dimms/

[5] https://www.anandtech.com/show/12828/intel-launches-optane-dimms-up-to-512gb-apache-pass-is-here

[6] https://www.samsung.com/semiconductor/dram/module/

[7] https://arxiv.org/abs/1903.05714

[8] https://newsroom.intel.com/editorials/3d-xpoint-memory-storage/

[9] https://www.intelsalestraining.com/infographics/memory/3DXPointc.pdf

[10] https://www.theregister.co.uk/2019/01/15/supermicro_server_cascade_lake_optane/

In Intel's new Cascade Lake architecture each CPU socket has up to 6 PMMs attached via two memory controllers, for a maximum capacity of 6TB per socket. Each PMM contains an internal indirection table which is used to map CPU physical addresses to internal addresses; this allows wear leveling and bad block management to be done internally to each module.[11] A module or module partition can be configured in one of two modes: in *Memory* mode the DRAM attached to the same controller acts as a cache, while in *AppDirect* mode the persistent memory is accessed by the CPU directly. Memory mode does not support persistence — there is no way to force writebacks — and so I will not consider this mode any further here.

To bring this technology to market requires a wide variety of developments involving many aspects of system architecture, as I shall describe in later parts, and which have taken many years to complete. It's not "just" a matter of inventing a non-volatile circuit technology and building pin-compatible DIMMs. This gives Intel an advantage, in that there aren't many industry players in control of all the necessary technologies. There's a downside too, however: Intel's NVDIMMs won't work in other manufacturer's systems; they won't even work in older Intel hardware. An enterprise customer wanting multiple sources of non-volatile memory technology before making mission-critical changes to its IT architecture will have to wait for competitors to catch up. To help minimize divergence, an industry consortium (SNIA — the Storage Networking Industry Association) has been authoring a roadmap under its Solid State Storage Initiative[12].

There are many other companies developing NVRAM technologies, so I am confident that multiple sources will emerge, eventually, although the timescale is difficult to predict. Some, e.g., Nantero, claim that their technology will be as fast as DRAM. If speed and endurance eventually match or improve upon DRAM, then it becomes conceivable to replace *all* DRAM with NVRAM, but this does not appear imminent. However, if DRAM is eventually replaced by NVM it would be nice if we could avoid having to go through two rounds of disruption in the way we build software, and plan for that eventuality.

In the next part I will discuss software issues in using NVRAM.

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[11] https://arxiv.org/abs/1903.05714, §2.1.1

[12] https://www.snia.org/forums/sssi