Two FIFO Ring Performance Experiments

Charles E. Molnar
Ian W. Jones
William S. Coates
Jon K. Lexau
Scott M. Fairbanks
Ivan E. Sutherland

20 May 1998

Sun Microsystems Inc.

Palo Alto, California.

Motivation

- Asynchronous vs. clocked, which is faster?
- Early discouraging results.
- Re-examine basic circuits.
- Gain experience with new asynchronous design techniques:
  - Control kiting.
  - Dual-rail complementary control signals.
  - asP* control protocol.
- Our experiments exhibit equivalent performance with greater functionality.

Introduction

- **Two asynchronous FIFO designs fabricated in 0.6 m CMOS:**

  a) asP* - uses a pulse-like control protocol and conventional data latches.

  b) Micropipeline - uses transition signaling protocol and special transition data latches that are about 50% larger.

- **Management of local delays required.**

- **Throughput:**

  - asP* = 1.1 Giga data items per second.

  - Micropipeline = 1.7 G data items per sec.

Goals

1) To design an asynchronous FIFO that performs as fast as a clocked shift register.

2) The “ultimate verification method”: build and test chips.

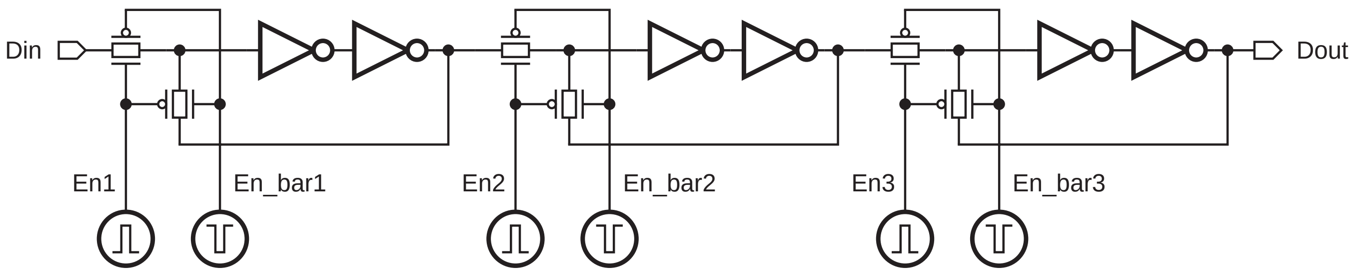
   a) Establish path to fabrication.

   b) Develop test procedures.

   c) Correlate simulation results with measured chip performance.

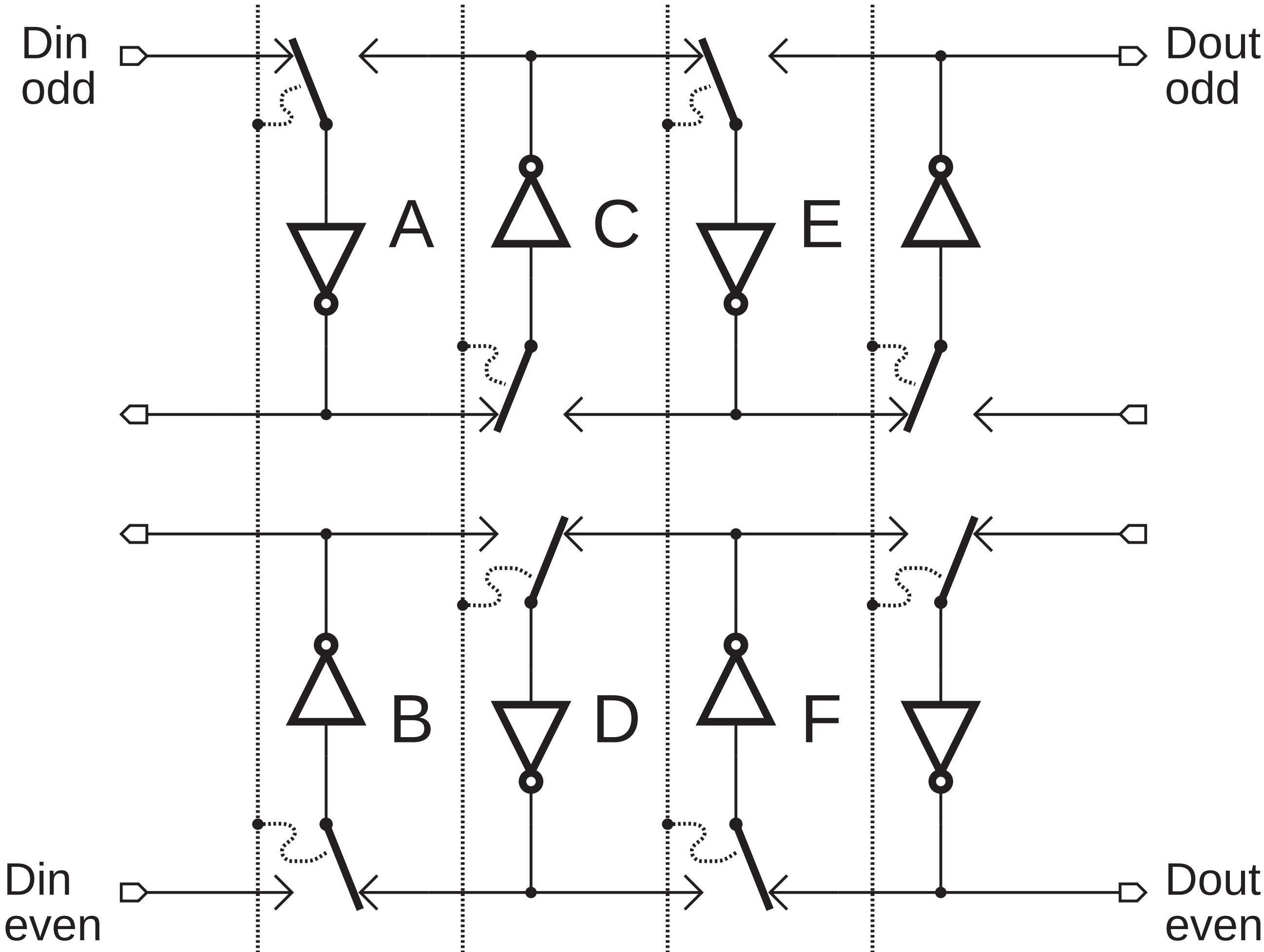
   d) Gain experience in managing local delays and the effects of process variation.

   e) Measure circuit robustness.

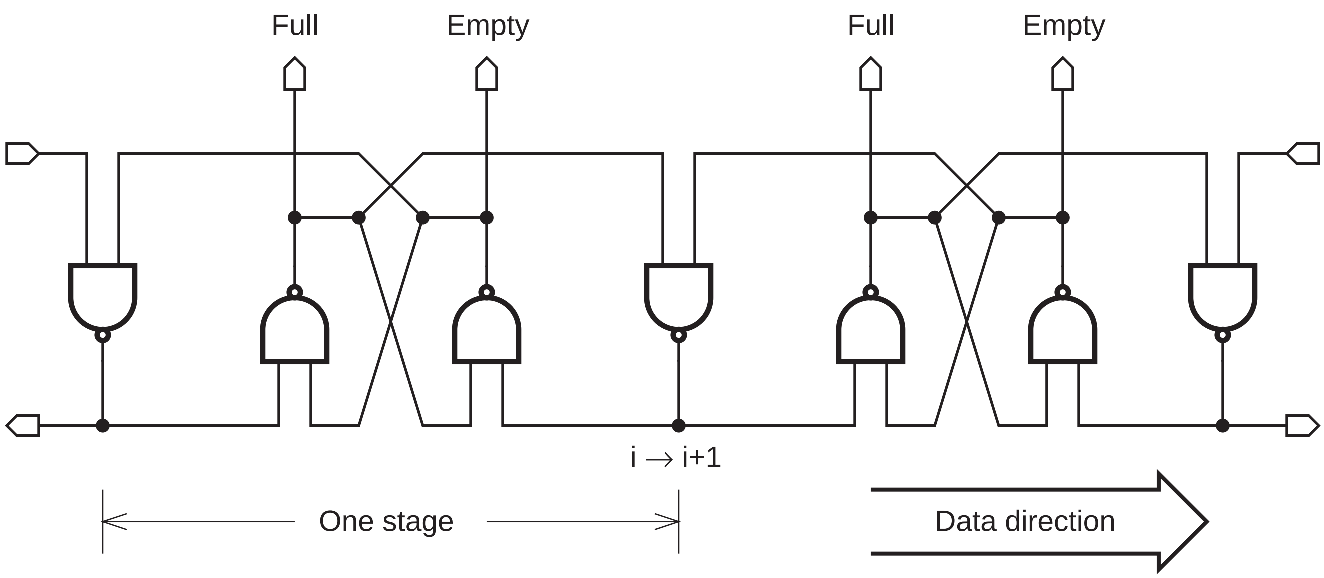


Data Latch Study - Magic Control

- **Choose latch circuit for the asP* design.**
- **Best with two complementary “clocks”, 180° out of phase, 800ps cycle time.**
- **Can asynchronous control produce such “clock” signals?**

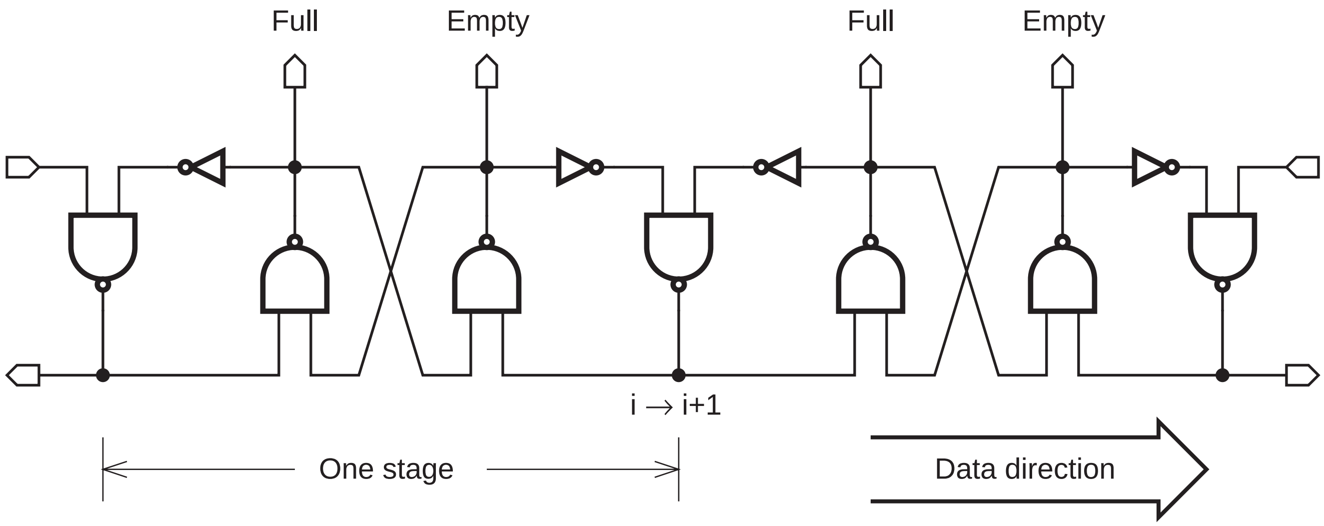


Micropipeline Transition Data Latches



First-cut asP* FIFO Control

- **Pulse used to “move” data from full to empty stage.**
- **Circuit is sensitive to timing variations.**
- **Circuit has undesirable stable state with both outputs HI.**

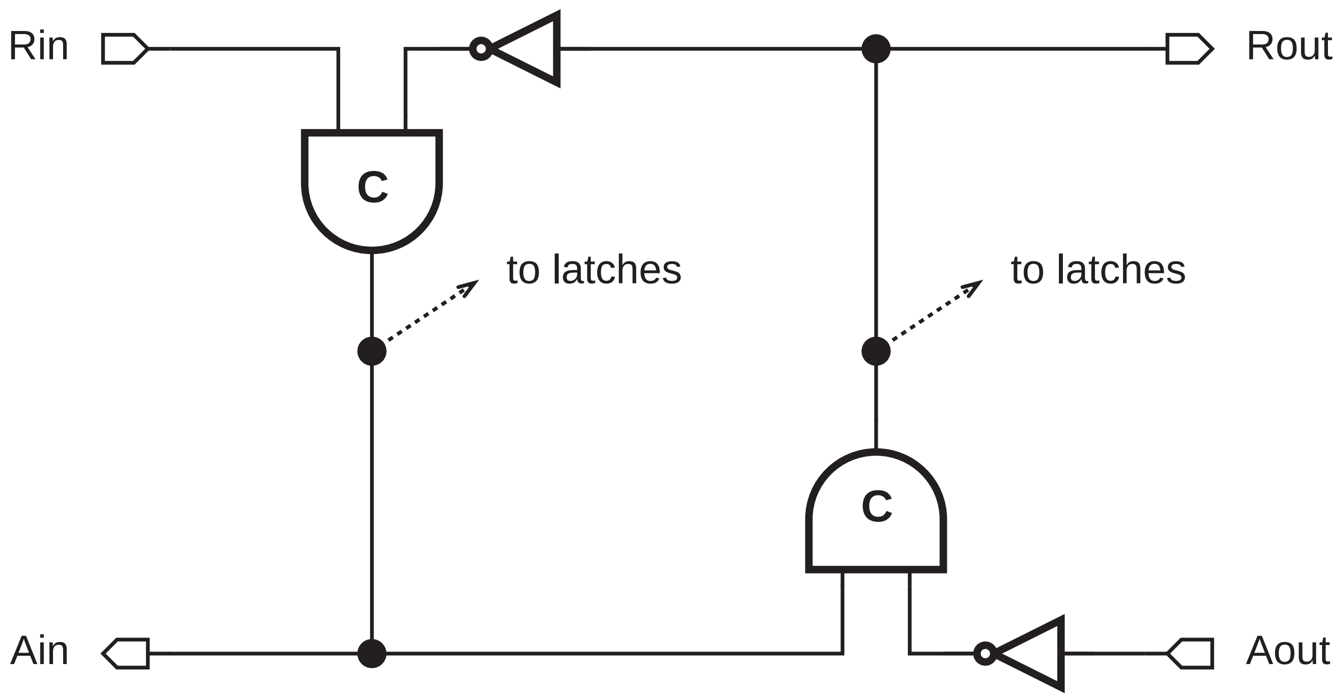


Improved asP* FIFO Control

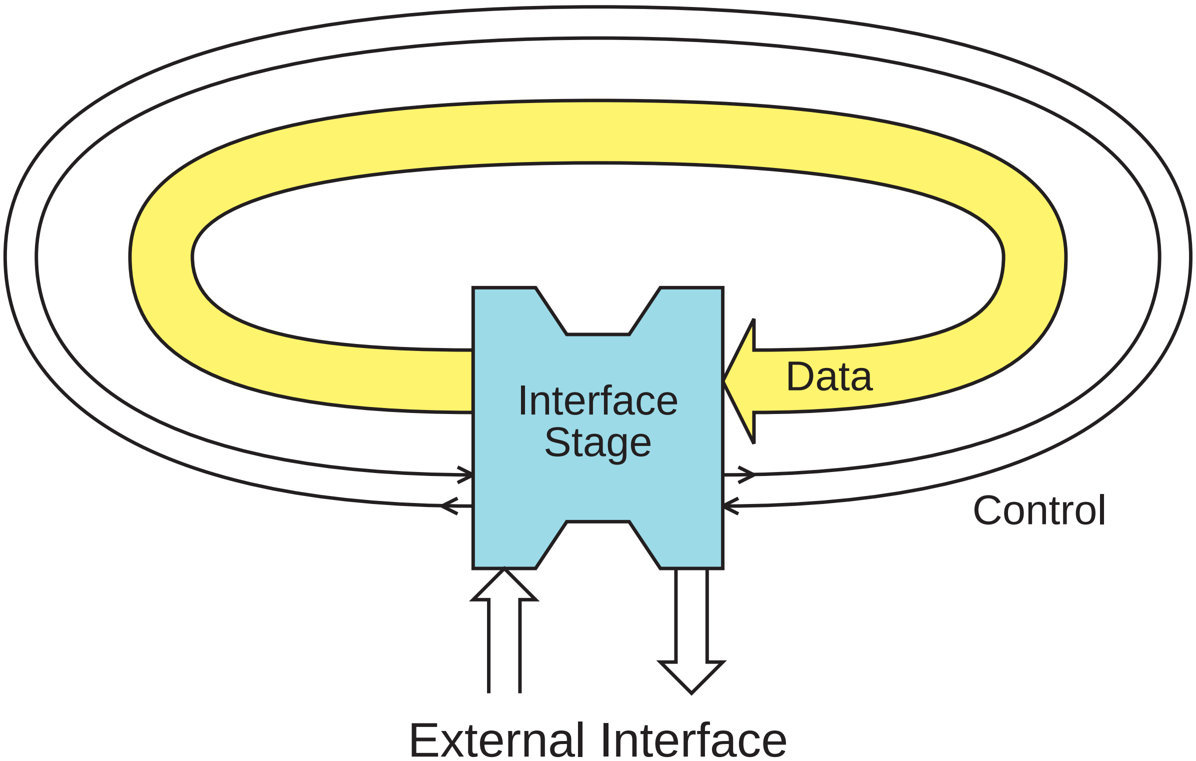
- **Move pulse generated by:**
  (not Empty[i]) & (not Full[i+1]).

- **Less sensitive to timing variations.**

- **No undesirable stable state.**



Micropipeline Control

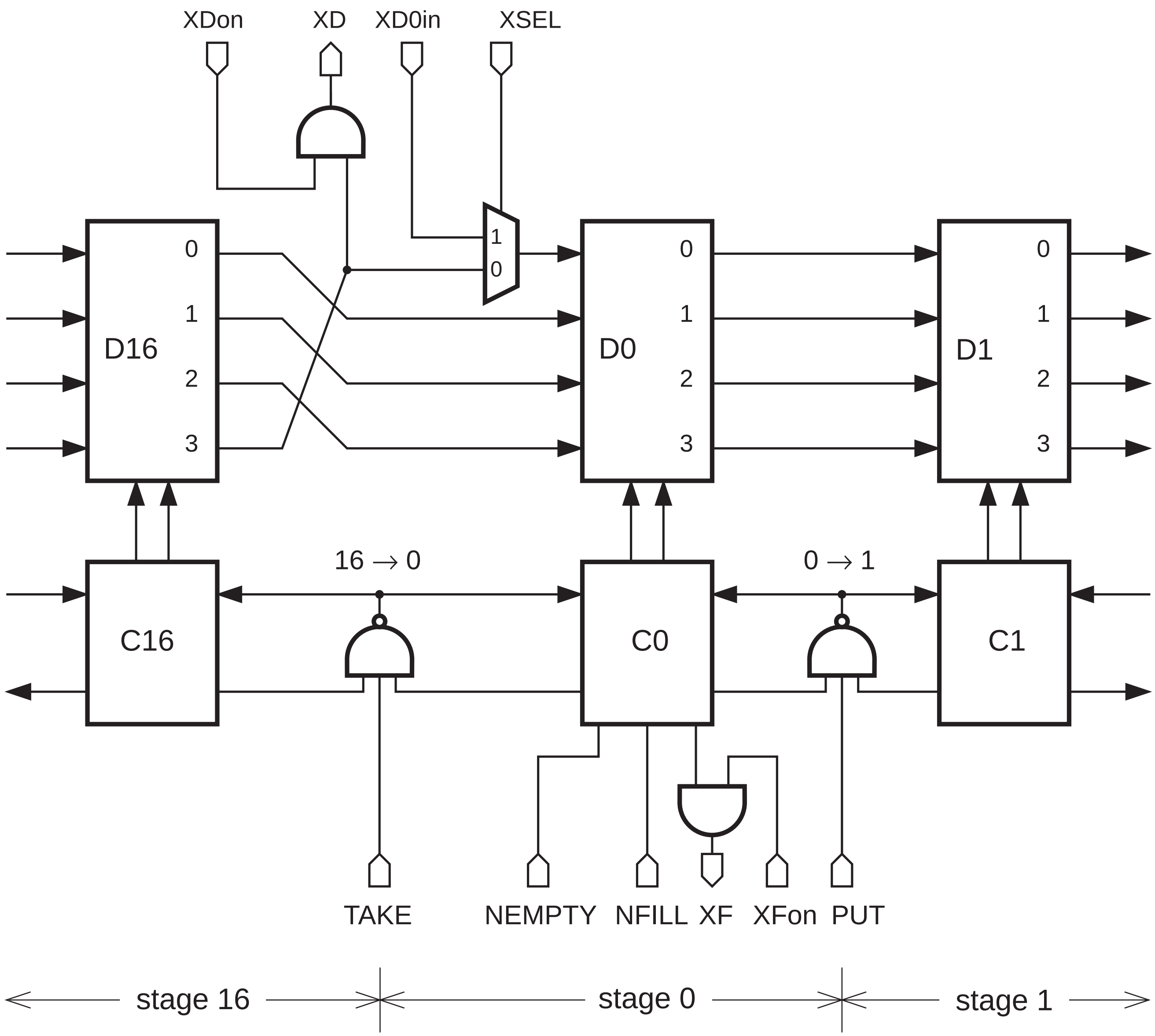


FIFO Ring Experiments

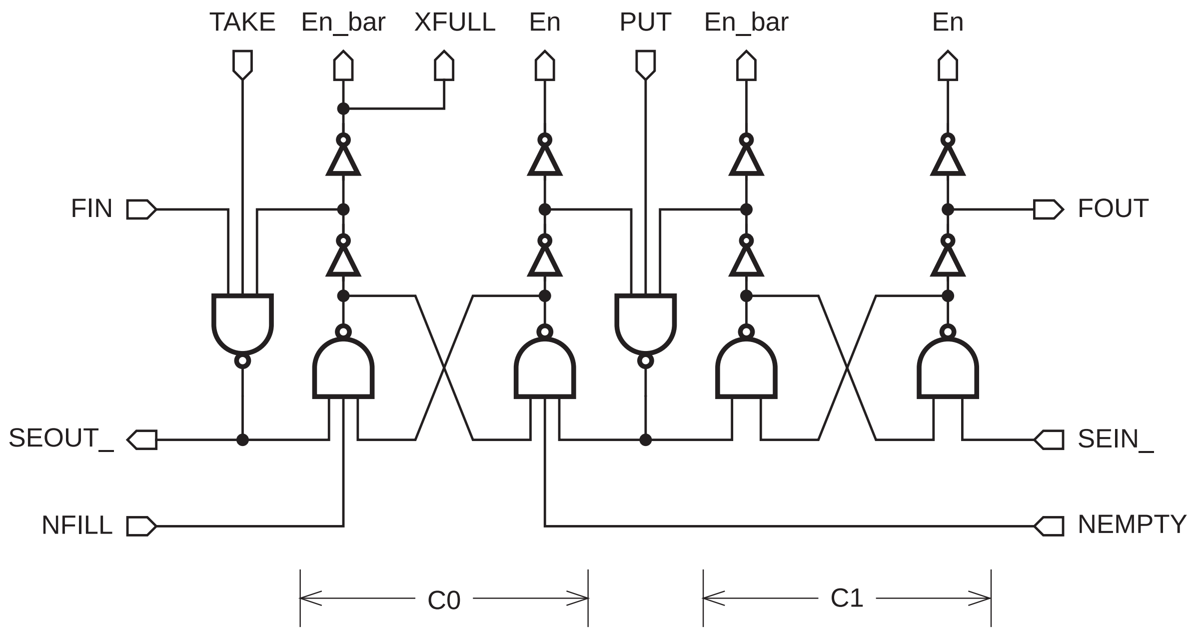
- 17 stages, 4-bit data path.
- Interface to initialise, load, unload, start, stop, and observe.

The Interface Stage - asP*

- Two external enable signals, TAKE and PUT.
- Observe data and control.
- Helical data path, one bit circular shift.
- One bit I/O.
- Can put 1-17 full cells into the ring.

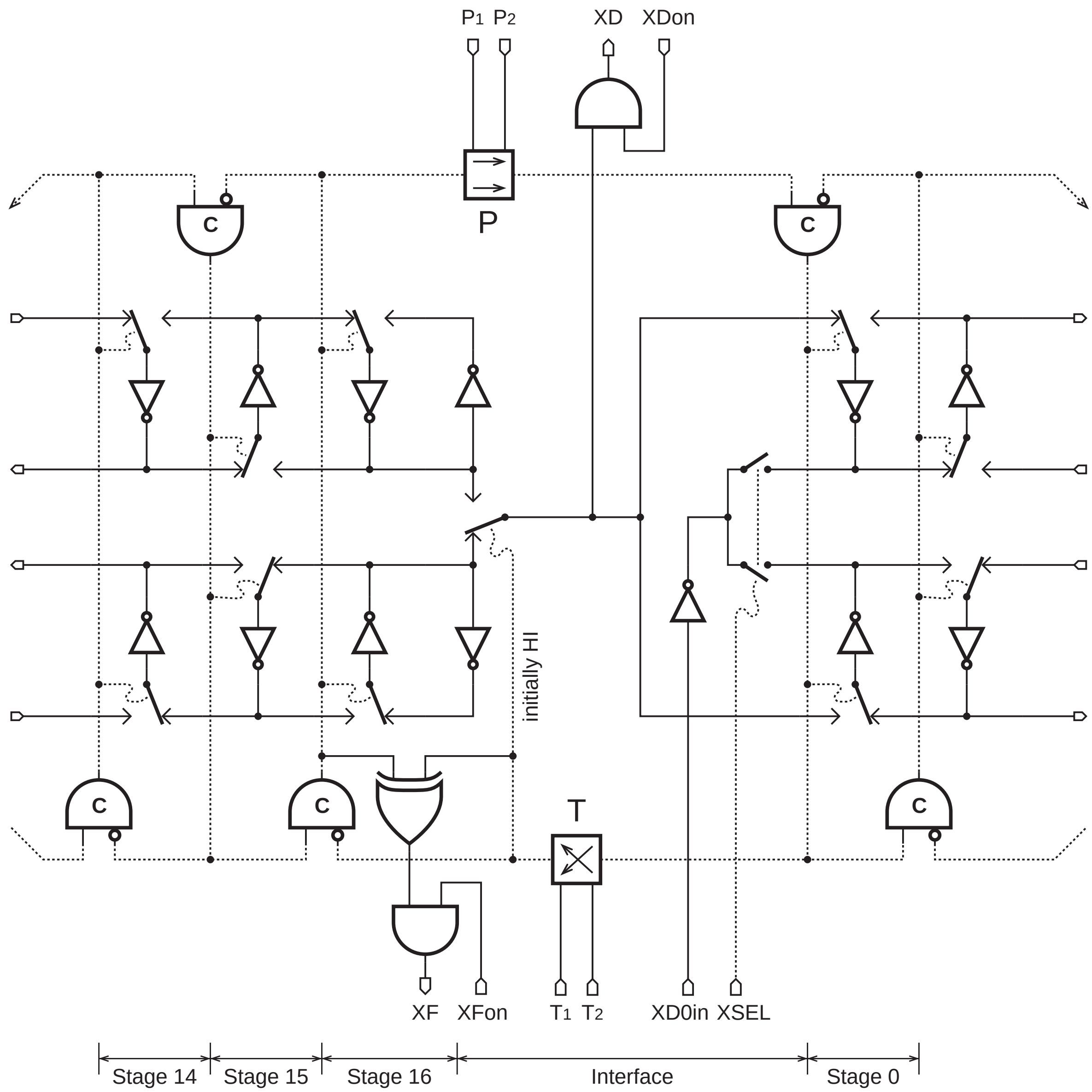


Interface Stage - asP*

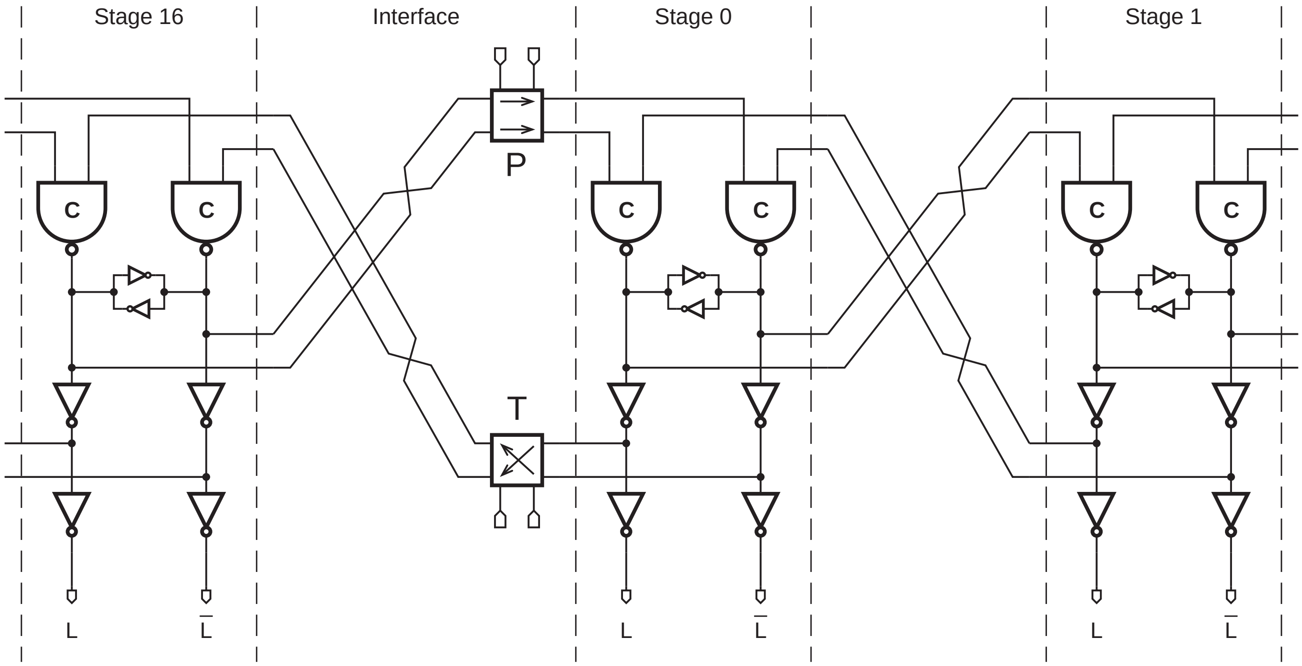


Interface Control Circuit - asP*

- **Additional delay, NAND2 ⇒ NAND3.**



Micropipeline Interface



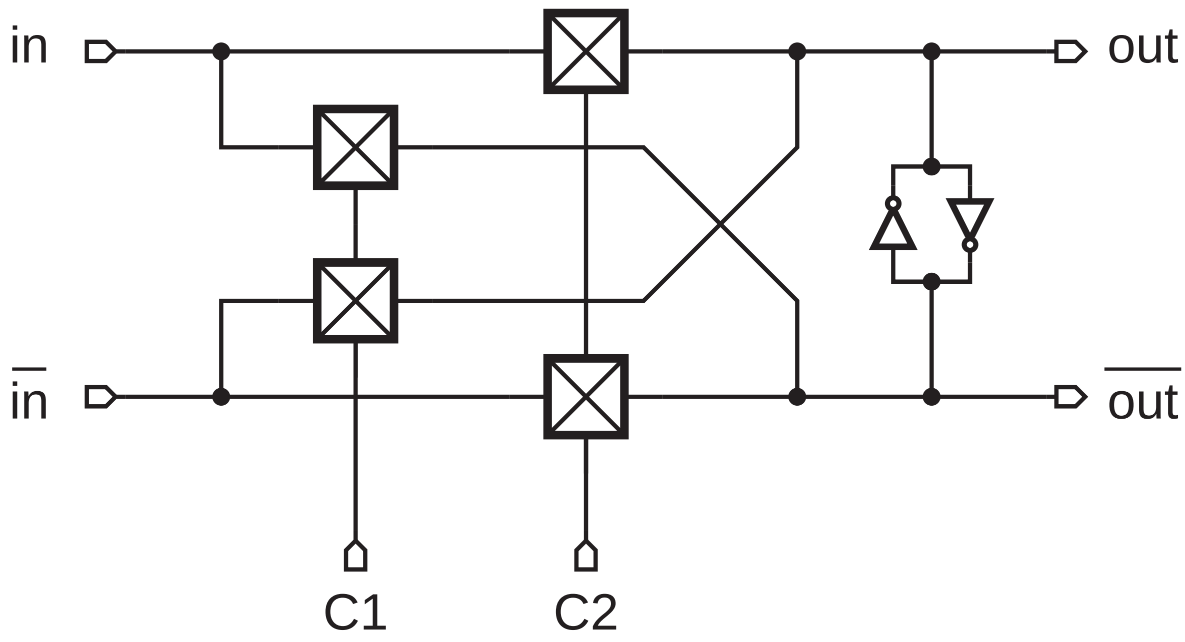
Dual-rail Micropipeline Control

- **Two forms of negation:**

  a) Real Inversion.

  b) Swap.

  - Odd number of real inversions in each control loop.



Switch Implementation

Two Useful Data Patterns

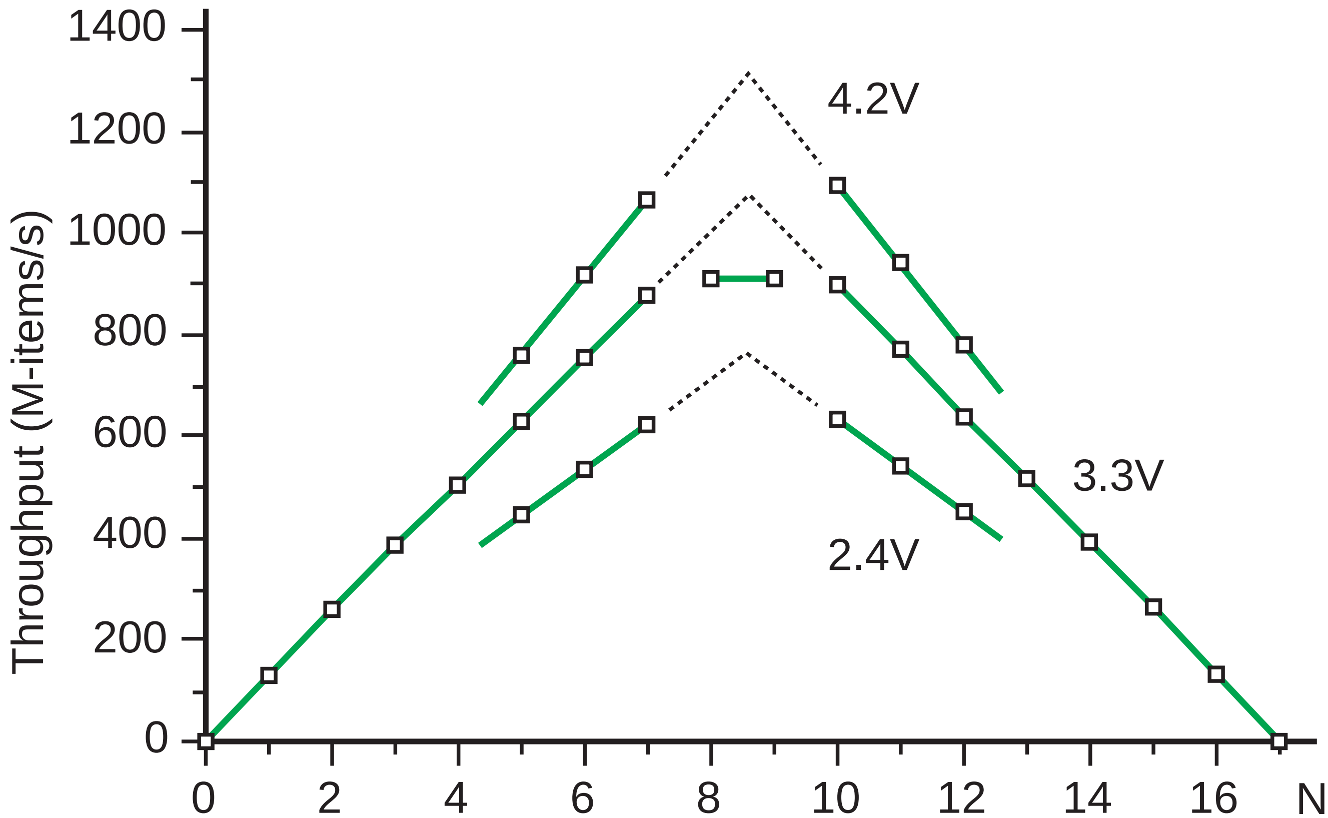
- **Half 1’s followed by half 0’s**
  - **lowest output frequency.**
- **All possible sequential combinations of 4 bits**
  - **check correct functionality.**

Testing Results - asP*

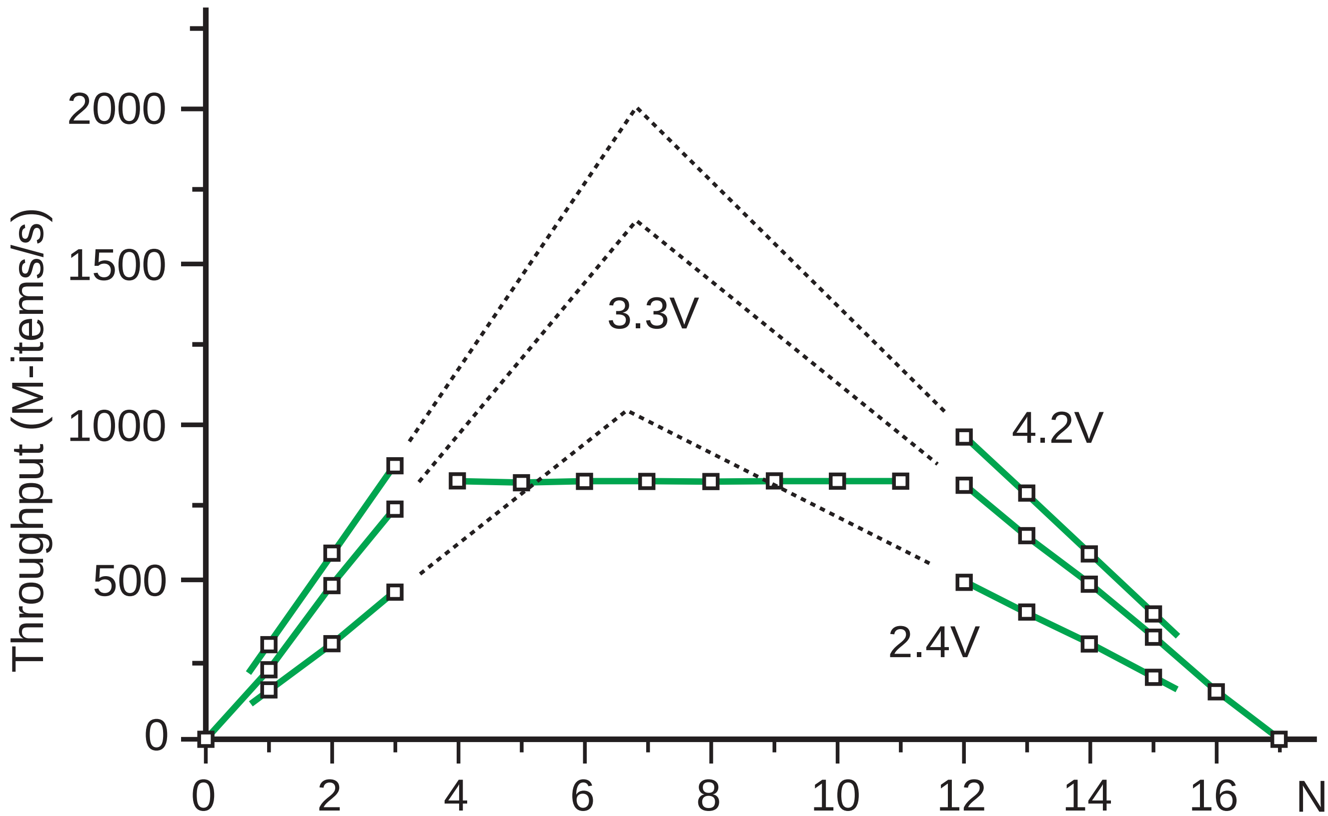
- 50 chips in MOSIS 0.6 m CMOS.
- 3.3V nominal Vdd.
- Peak measured throughput of 946 M data items per second at nominal Vdd.
- Interface stage was bottleneck.
- Would be 1.1 G data items per second without interface stage.
- Operates over a large range of voltages and temperatures.

Testing Results - Micropipeline

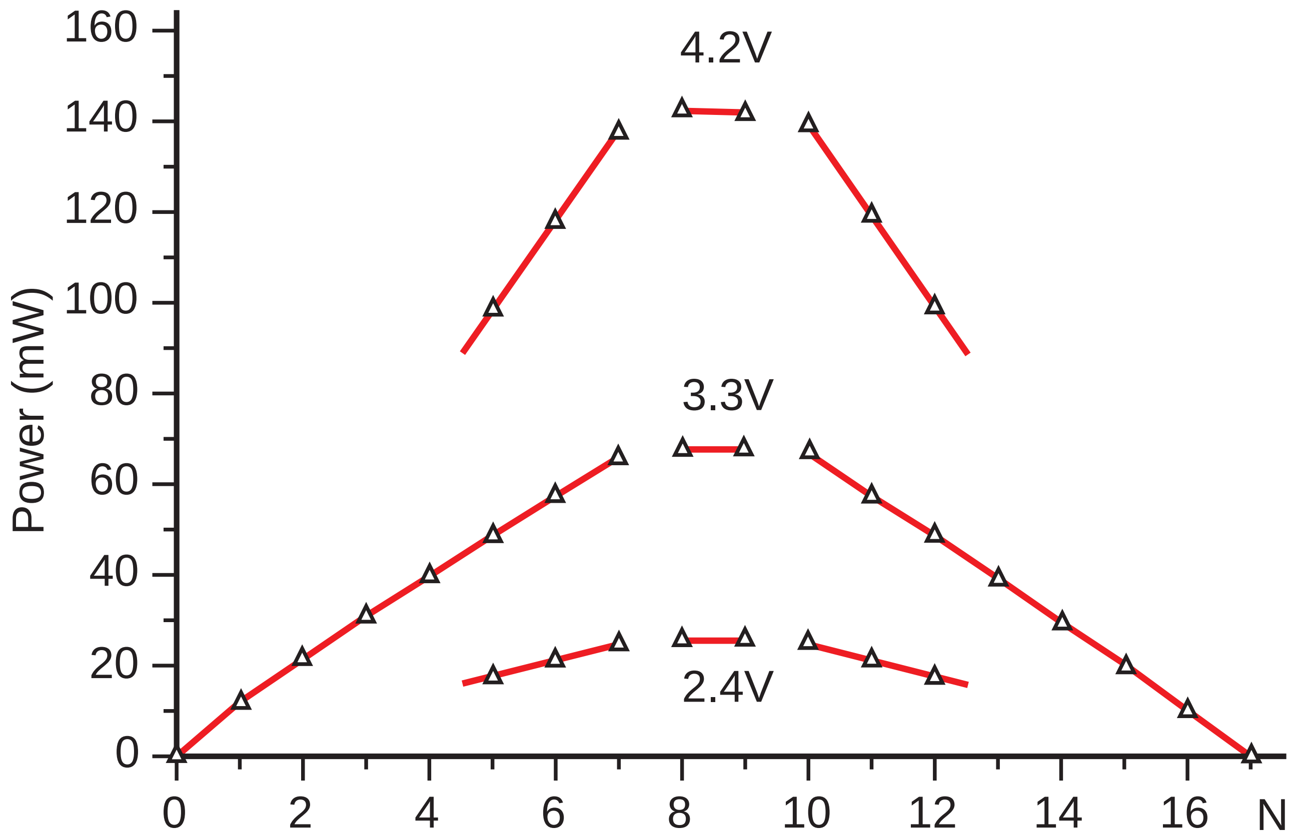
- 25 chips in MOSIS 0.6 m CMOS.
- 3.3V nominal Vdd.
- Peak measured throughput of 857 M data items per second at nominal Vdd.
- Interface circuit was bottleneck.
- Would be 1.7 G data items per second without interface circuit.
- Operates over a large range of voltages and temperatures.



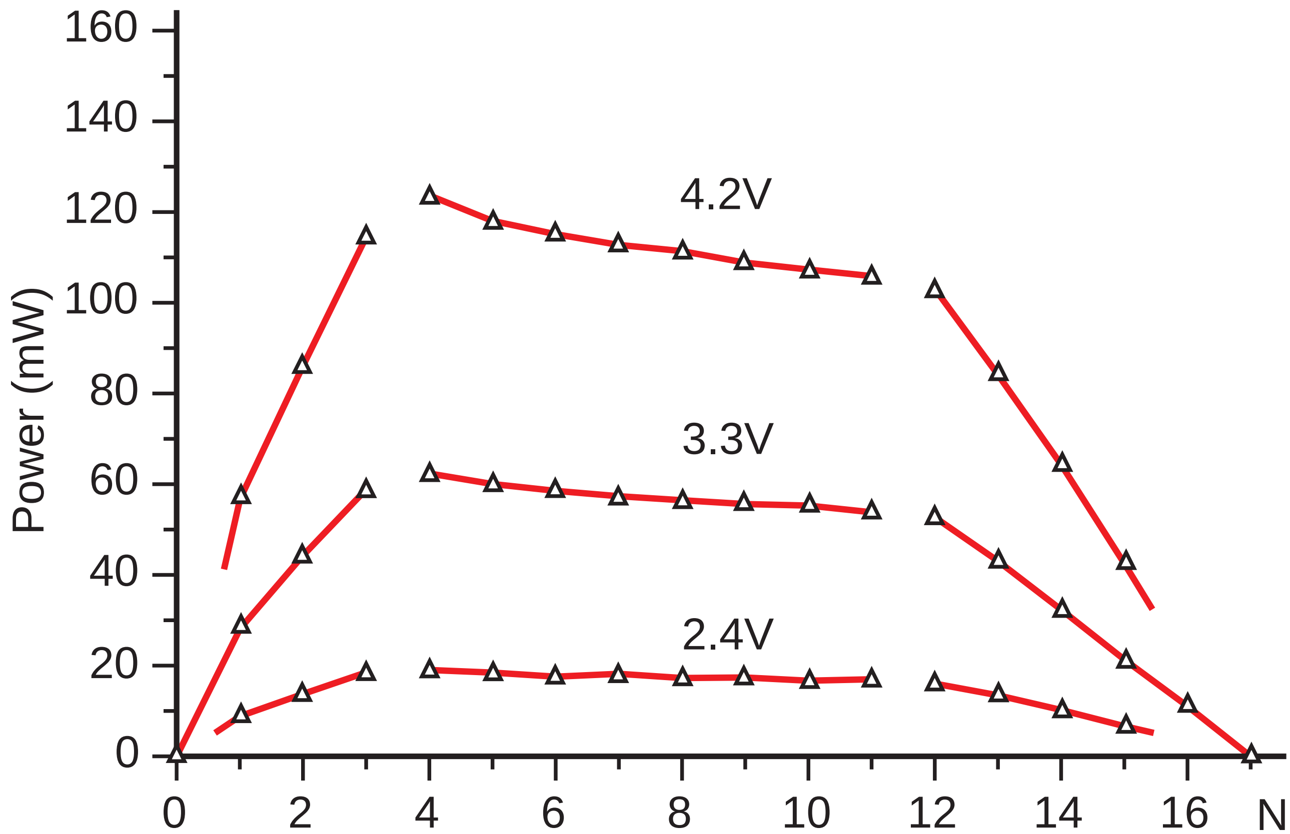
Throughput vs. Number of Full Cells - asP*



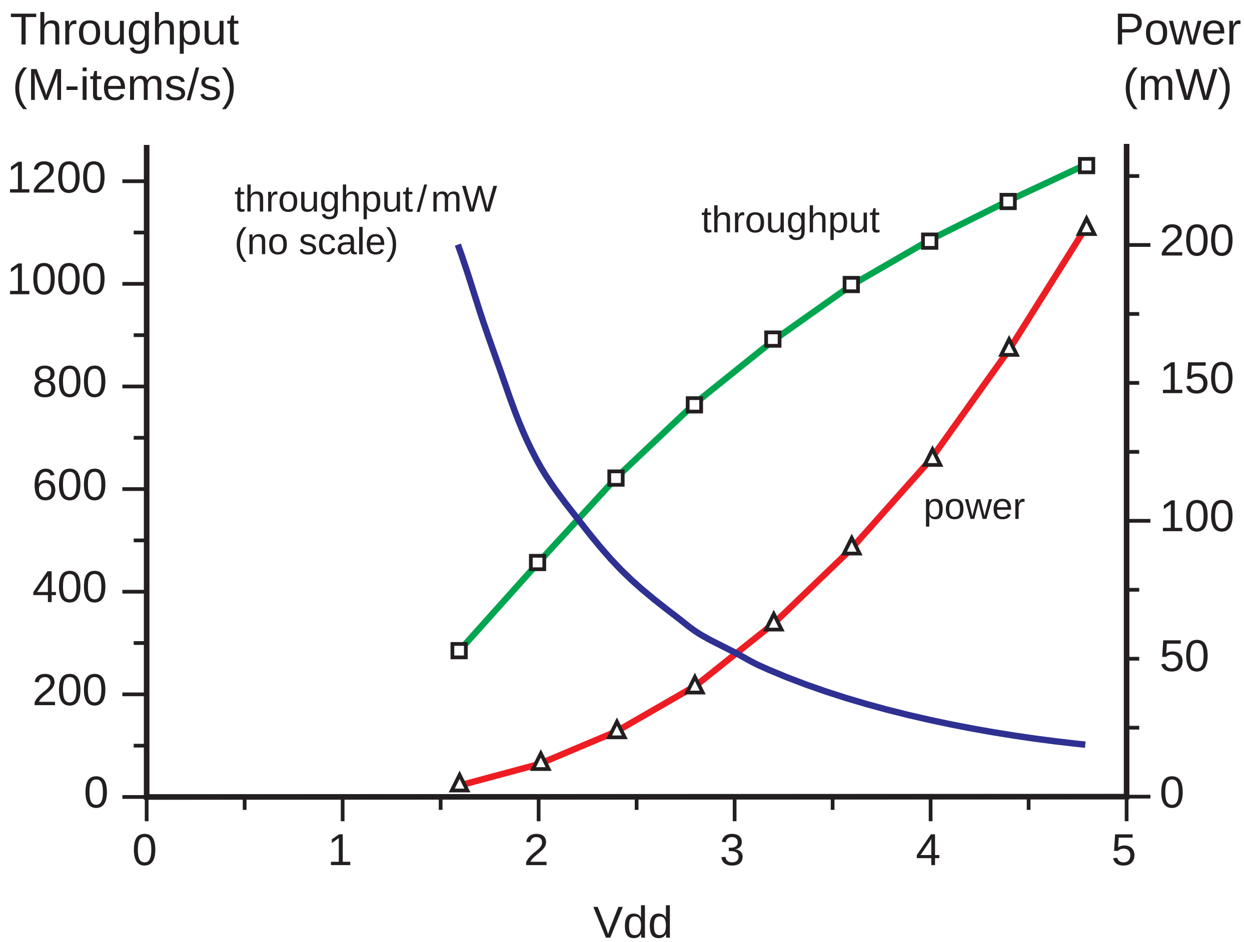
Throughput vs. Number of Full Cells - Micropipeline



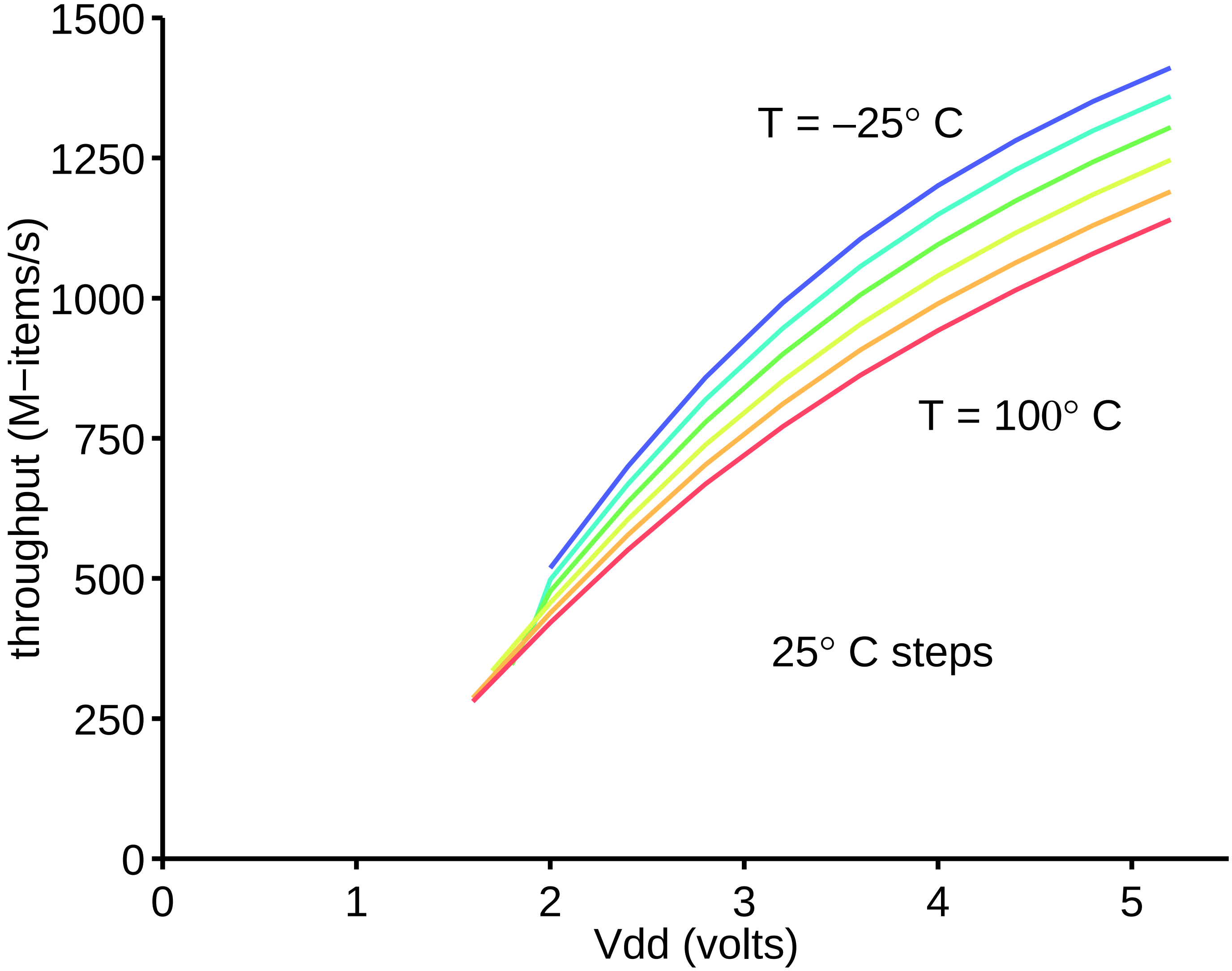
Power vs. Number of Full Cells - asP*



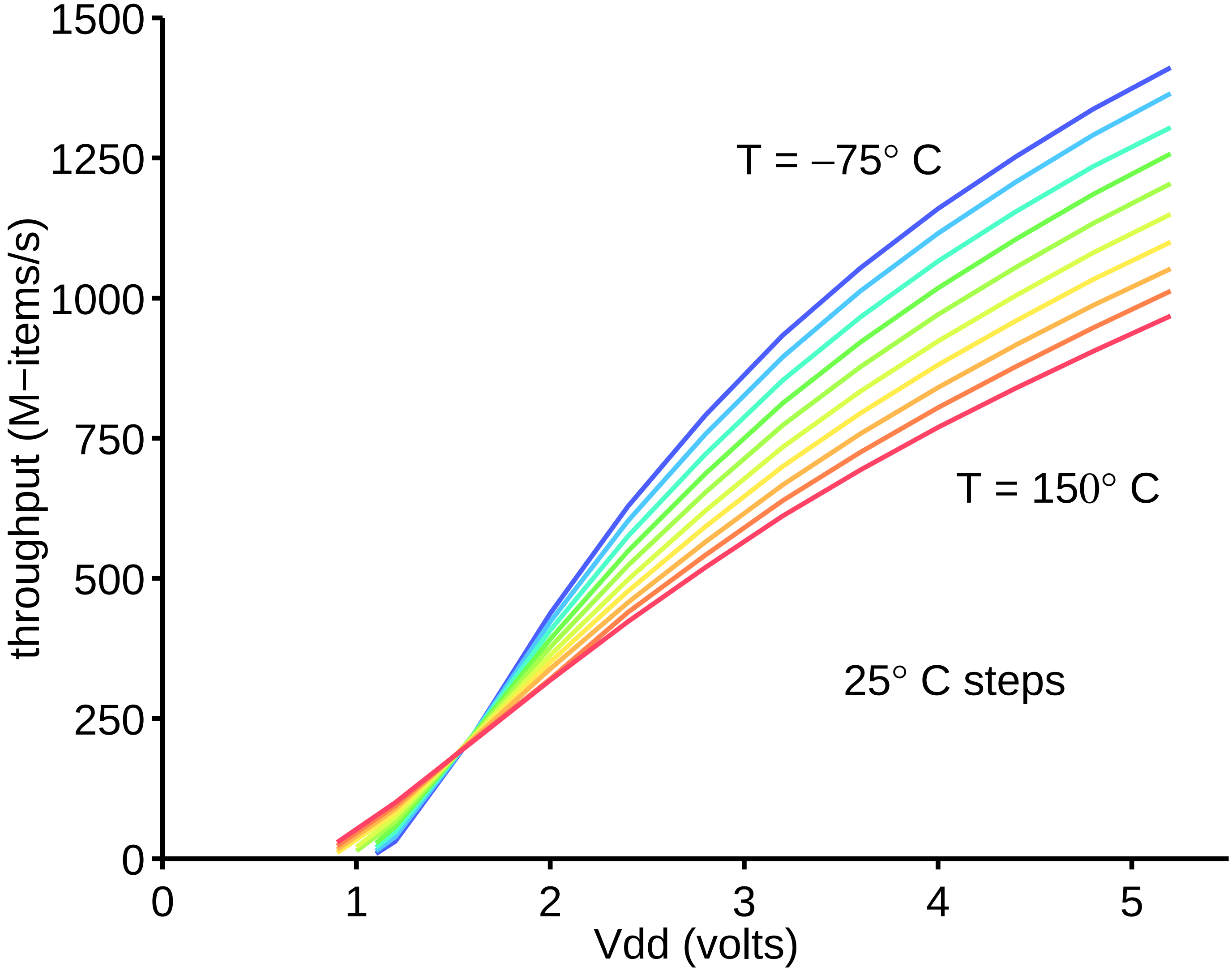
Power vs. Number of Full Cells - Micropipeline



Throughput and Power vs. Vdd - asP*



Throughput vs. Temperature for One asP* Chip



Throughput vs. Temperature for One Micropipeline Chip

Conclusions

- **Experiments build confidence that asynchronous circuits can be as fast as synchronous circuits.**
- **Local delays are manageable.**
- **Ring test procedure excellent.**
- **Helical data path helps instrumentation, but complicates test programs.**