Yossi Lev

Contact information
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Research Interests

Concurrent Programming
Parallel Algorithms
Transactional Memory
Concurrent Datastructures
Architectural Support

Education:

2004 - 2010   Brown University, Providence, RI, USA
PhD in Computer Science
Advisor: Prof. Maurice Herlihy
Thesis: Debugging and Profiling of Transactional Programs

2001 - 2004   Tel-Aviv University, Tel-Aviv, Israel
MSc in Computer Science, magna cum laude
Advisor: Prof. Nir Shavit
Thesis: A Dynamic-Sized Non-Blocking Work-Stealing Deque

1995 - 1999   Tel-Aviv University, Tel-Aviv, Israel
BSc in Mathematics & Computer Science

Awards and Honors

- Best Paper Award, PPoPP 2008

Publications: Refereed Conferences and Workshops
(Authors ordered alphabetically)

1. Dave Dice and **Yossi Lev** and Yujie Liu and Victor Luchangco and Mark Moir,
   "Using Hardware Transactional Memory to Correct and Simplify an Readers-Writer Lock Algorithm"
   PPoPP 2013

2. Irina Calciu and David Dice and **Yossi Lev** and Victor Luchangco and Virendra Marathe and Nir Shavit,
   "NUMA-Aware Reader-Writer Locks"
   PPoPP 2013

3. Aleksandar Dragojevic and Maurice Herlihy and **Yossi Lev** and Mark Moir,
   "On The Power of Hardware Transactional Memory to Simplify Memory Management"
   PODC 2011

4. Aleksandar Dragojevic and Maurice Herlihy and **Yossi Lev** and Mark Moir,
   "On The Power of Hardware Transactional Memory to Simplify Memory Management"
   PODC 2011

5. **Yossi Lev** and Mark Moir,
   "Lightweight Parallel Accumulators Using C++ Templates"
   IWMSE 2011

6. Fraincois Carouge and Luke Dalessandro and **Yossi Lev** and Mark Moir and Michael Scott and Michael Spear and Sean White,
   "Hybrid NOrec: A Case Study in the Effectiveness of Best Effort Hardware Transactional Memory"
   ASPLOS 2011

7. Dave Dice and **Yossi Lev** and Virendra J. Marathe and Mark Moir and Dan Nussbaum and Marek Olszewski,
   "Simplifying Concurrent Algorithms by Exploiting Hardware TM"
   SPAA 2010

8. Maurice Herlihy and **Yossi Lev**,
   "tm_db: A Generic Debugging Library for Transactional Programs"
   PACT 2009

9. **Yossi Lev**, Victor Luchangco and Marek Olszewski,
   "Scalable Reader-Writer Locks"
   SPAA 2009

10. **Yossi Lev**, Victor Luchangco, Virendra Marathe, Mark Moir, Dan Nussbaum and Marek Olszewski,
    "Anatomy of a Scalable Software Transactional Memory"
    TRANSACT 2009

11. Dave Dice, **Yossi Lev**, Mark Moir and Dan Nussbaum,
    "Early Experience with a Commercial Hardware Transactional Memory Implementation"
    ASPLOS 2009

12. **Yossi Lev** and Jan-Willem Maessen,
    "Split Hardware Transactions: True Nesting of Transactions Using Best-Effort Hardware Transactional Memory"
    Best paper award in PPoPP 2008

13. Dave Dice, Maurice Herlihy, Doug Lea, **Yossi Lev**, Victor Luchangco, Wayne Mesard, Mark Moir, Kevin Moore and Dan Nussbaum,
    "Applications of the Adaptive Transactional Memory Test Platform"
    TRANSACT 2008

14. Faith Ellen, **Yossi Lev**, Victor Luchangco, and Mark Moir,
    "SNZI: Scalable Non-Zero Indicators"
    PODC 2007

15. Lawrence Crowl, **Yossi Lev**, Victor Luchangco, Mark Moir, and Dan Nussbaum,
    "Integrating Transactional Memory into C++"
    TRANSACT 2007

16. **Yossi Lev**, Mark Moir, and Dan Nussbaum,
    "PhTM: Phased Transactional Memory"
    TRANSACT 2007

17. Maurice Herlihy, **Yossi Lev**, Victor Luchangco, Nir Shavit,
    "A Simple Optimistic Skip-List Algorithm"
    SIROCCO 2007 (also a brief announcement in OPODIS 2006)

18. Peter Damron, Alexandra Fedorova, **Yossi Lev**, Victor Luchangco, Mark Moir, and Dan Nussbaum,
    "Hybrid Transactional Memory"
    ASPLOS 2006

19. **Yossi Lev** and Mark Moir,
    "Debugging with Transactional Memory"
    TRANSACT 2006

20. **Yossi Lev** and Jan-Willem Maessen,
    "Towards a Safer Interaction with Transactional Memory"
    SCOOL 2005

21. David Chase and **Yossi Lev**,
    "Dynamic Circular Work-Stealing Deque"
    SPAA 2005

22. Danny Hendler, **Yossi Lev** and Nir Shavit,
    "Dynamic Memory ABP Work-Stealing"
    DISC 2004
    Invitation to contribute to a special issue

Publications: Journals

1. Danny Hendler, **Yossi Lev**, Mark Moir and Nir Shavit,
   Special Issue of DISC 2004: "A Dynamic-Sized Nonblocking Workstealing Deque"
   Distributed Computing 2006

Publications: Technical Reports

1. David Dice, **Yossi Lev**, Mark Moir, Daniel Nussbaum and Marek Olszewski,
   "Early Experience with a Commercial Hardware Transactional Memory Implementation"
   TR-2009-180, Sun Microsystems, October 2009

2. Danny Hendler, **Yossi Lev**, Mark Moir and Nir Shavit,
   "A Dynamic-Sized Nonblocking Work Stealing Deque"
   TR-2005-144, Sun Microsystems, November 2005

Publications: Posters

1. Dave Dice and **Yossi Lev** and Mark Moir,
   "Scalable Statistics Counters"
   PPoPP 2013

2. **Yossi Lev** and Mark Moir,
   "Fast Read Sharing Mechanism For Software Transactional Memory"
   PODC 2005

Talks

1. "Simplifying Concurrent Algorithms by Exploiting Hardware TM" SPAA 2010

2. "tm_db: A Generic Debugging Library for Transactional Programs" PACT 2009

3. "Anatomy of a Scalable Software Transactional Memory"
   TRANSACT 2009

4. "Debugging Transactional Programs"
   IPP Symposium on Standardizing Transactional Memory, 2009

5. "Preparing Debuggers for Transactional Programs"
   Dagstuhl Seminar "Transactional Memory : From Implementation to Application", 2008;
   Intel, Israel 2008

6. "Split Hardware Transactions: True Nesting of Transactions Using Best-Effort Hardware Transactional Memory"
   PPoPP 2008

7. "SNZI: Scalable Non-Zero Indicators"
   PODC 2007;
   INRIA, Paris 2007;
   Intel, Israel 2007;
   Technion Institute of Technology, Israel 2007

8. "Debugging with Transactional Memory"
   TRANSACT 2006

9. "A Simple Optimistic skip-list Algorithm"
   Brief announcement at OPODIS 2006

10. "Towards a Safer Interaction with Transactional Memory"
    SCOOL 2005

11. "Dynamic Circular Work-Stealing Deque"
    SPAA 2005

12. "Dynamic Memory ABP Work-Stealing"
    DISC 2004

Patents

1. "Breakpoints In A Transactional Memory-Based Representation Of Code",
   Issued Patent # 7620850

2. "Delayed Breakpoints",
   Issued Patent # 7840947

3. "Replay Debugging",
   Issued Patent # 7849446

4. "Concurrent lock-free skiplist with wait-free contains operator",
   Issued Patent # 7937378

5. "Read sharing using global conflict indication and semi-transparent reading",
   Issued Patent # 7711909

6. "Dynamic memory work-stealing",
   Issued Patent # 7779222

7. "Dynamic Circular Work-Stealing Deque",
   Issued Patent # 7346753

8. "Extendable memory work-stealing",
   Issued Patent # 7363438

9. "System And Method For Executing Nested Atomic Blocks Using Split Hardware Transactions",
   Issued Patent # 7516366

10. "System and method for split hardware transactions",
    Issued Patent # 7516365

11. "System And Method For Supporting Multiple Alternative Methods For Executing Transactions",
    Issued Patent # 7921407

12. "System and Method for Committing Results of a Software Transaction Using a Hardware Transaction",
    Application # 20110246725

13. "System and Method for Performing Visible and Semi-Visible Read Operations In a Software Transactional Memory",
    Application # 20110078385

14. "System and Method for Performing Dynamic Mixed Mode Read Validation In a Software Transactional Memory",
    Application # 20110125973

15. "Scalable Reader-Writer Lock",
    Application # 20100241774

16. "Conditioned Scalable Non-Zero Indicator",
    Application # 20100042997

17. "System and Method for Implementing Shared Scalable Nonzero Indicators",
    Application # 20090125548

18. "Simple Optimistic Skiplist",
    Application # 20090132563

19. "Efficient Implicit Privatization Of Transactional Memory",
    Application # 20080256074

20. "Watchpoints On Transactional Variables",
    Application # 20080127035

21. "Viewing And Modifying Transactional Variables",
    Application # 20070288901

22. "Atomic Groups For Debugging",
    Application # 20070288900

23. "Method And Apparatus For Improving Transactional Memory Interactions By Tracking Object Visibility",
    Application # 20070150509

24. Additional patents filled, titles are confidential.

Professional Service

Program Committees:

- TRANSACT, 2011

External Reviewer for:

- ACM Transactions on Computer Systems (TOCS), 2009

- ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2009

- ACM SIGPLAN Workshop on Transactional Computing (Transact), 2009

- ACM SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC), 2007

- (Sub-review) International Conference on Compiler Construction (ETAPS CC), 2005

- ACM Transactions on Computer Systems (TOCS), 2005

Research Experience

- **Research Assistant**,
  Brown University,
  Fall 2004 - Fall 2010

- **Intern**,
  Scalable Synchronization Research Group, Sun Microsystems Laboratories,
  Jan 2004 - June 2010

- **Researcher**,
  Scalable Synchronization Research Group, Oracle Labs,
  July 2010 - present

Research areas include: concurrent datastructures, design and development of software and hybrid transactional memory runtimes, integration of transactional memory in programming languages, debugging and profiling of transactional programs.

Teaching Experience

Teaching Assistant, Department of Computer Science, Brown University

- CS176: Introduction to Multiprocessor Synchronization (Fall 2005)
- CS176: Introduction to Multiprocessor Synchronization (Fall 2006)

Other Employment

- **Software Engineer**
  Seabridge
  Israel, September 1999 - April 2003

Work areas include: design and implementation of embedded code for communication switches, multi-threaded programming, embedded operating systems.

Immigration Status

Citizen of Israel, J2 visa to the US, full authorization to work in the US

References

- **Prof. Maurice Herlihy**, Brown University

- **Dr. Mark Moir**, Sun Microsystems Labs

- **Dr. Dan Nussbaum**, Sun Microsystems Labs

- **Dr. Victor Luchangco**, Sun Microsystems Labs

- **Prof. Nir Shavit**, Tel-Aviv University