A COUNTERFLOW PIPELINE EXPERIMENT

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"... their construction being as it were a wheel within a wheel"

Ezekiel, chapter 1, verse 16

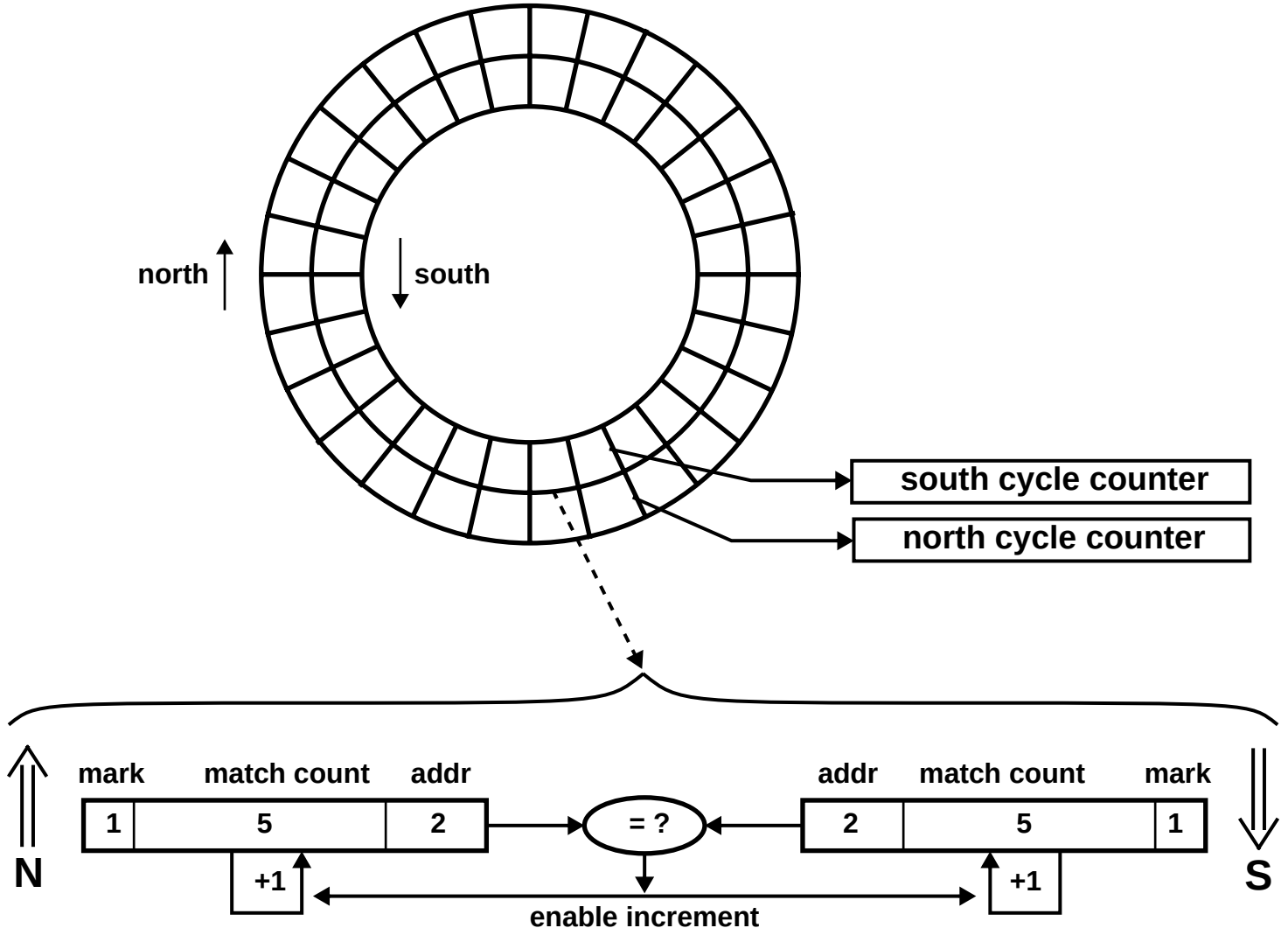
Presentation Outline

- **Background and Motivation**
- **Chip Overview**
- **Design and Implementation of Experiment**
- **Measured Results**
- **Conclusions and Ongoing Research**

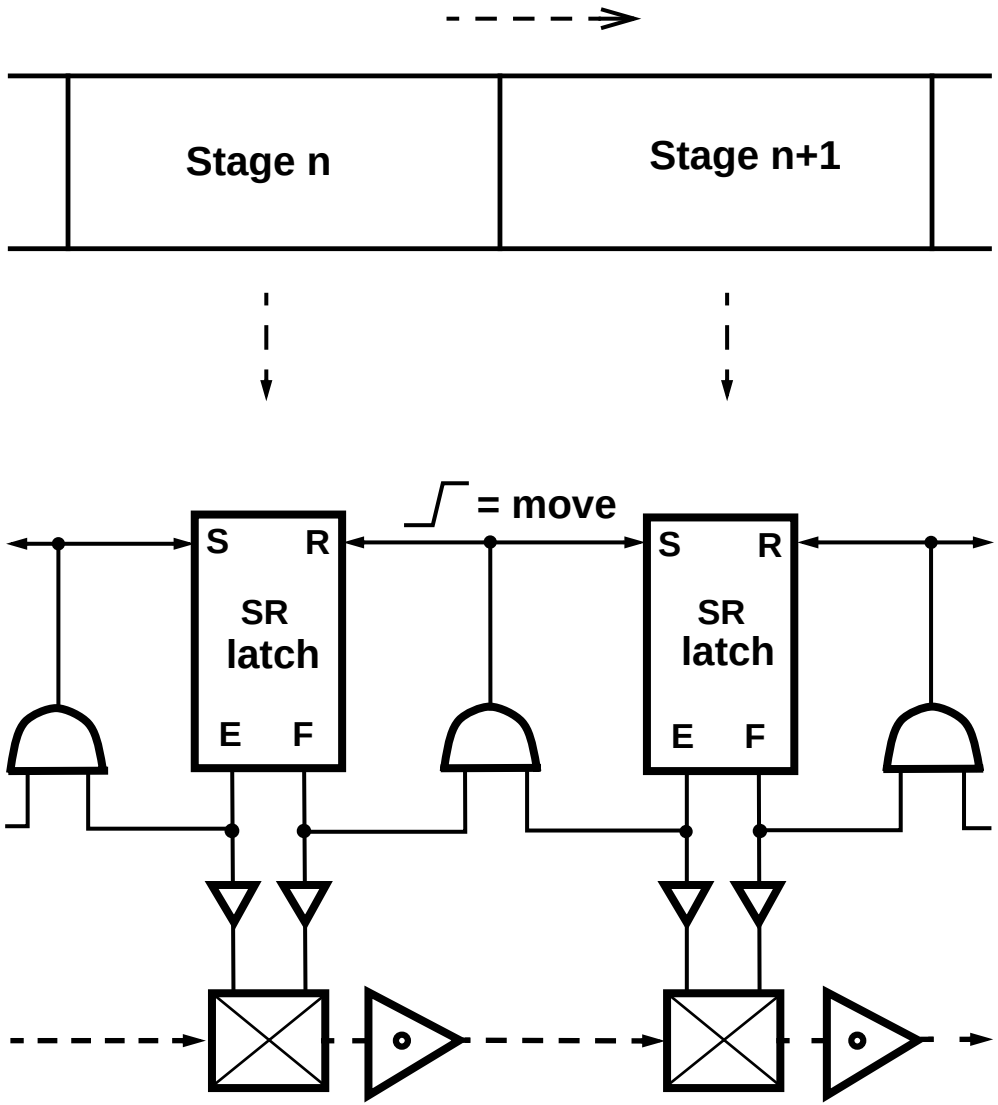
Background and Motivation

- **The Counterflow Pipeline Processor**
  - **Proposed by Sproull, Sutherland & Molnar in 1992**
  - **Counterflowing Instruction and Result streams**
- **Counterflow Pipeline Rules**
  - **Each instruction and result must interact**
  - **Mutual exclusion between boundary crossings**
- **Goals of Zeke Test Chip**
  - **Test correct operation - no “misses”**
  - **Focus on possible arbitration problems**
  - **Speed, speed, speed**
  - **Learn by building and measuring**

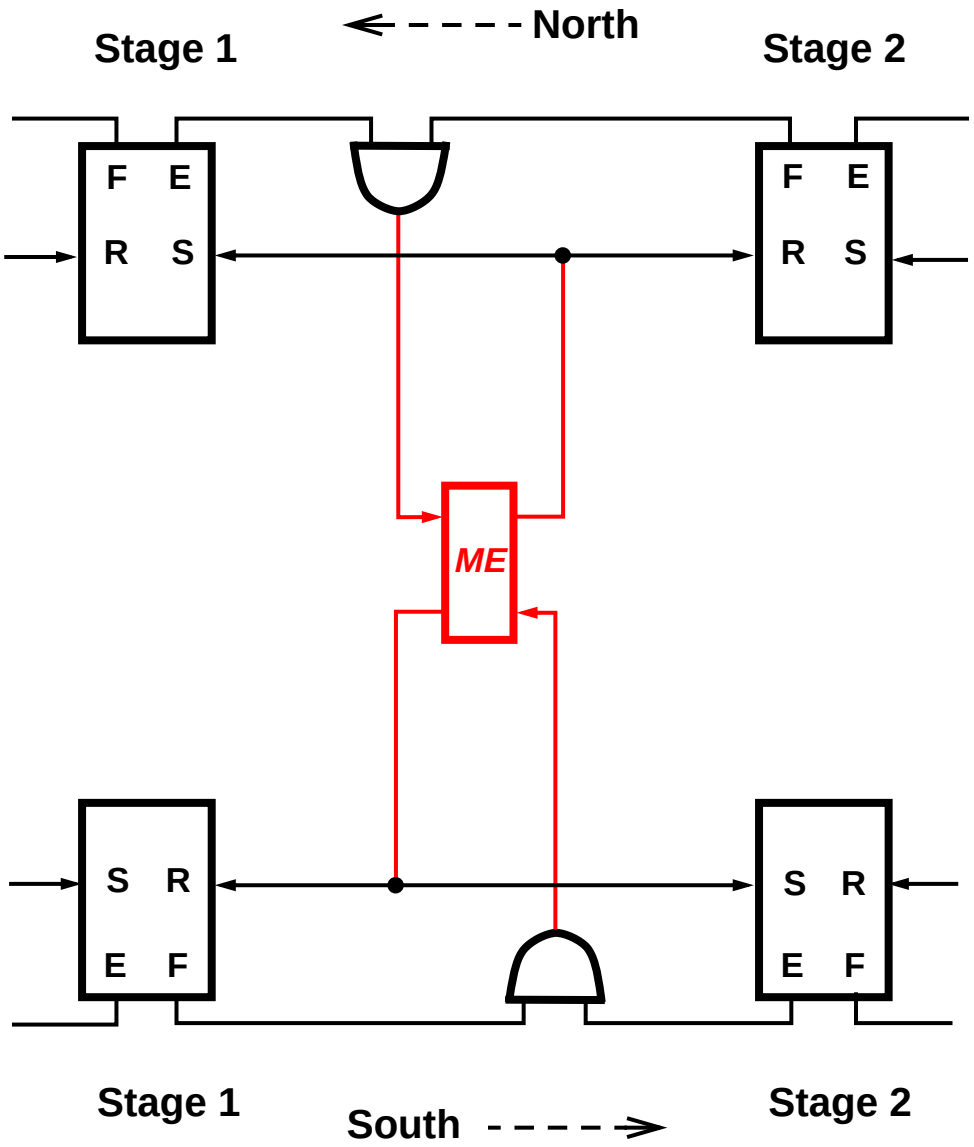
High-Level Chip Overview



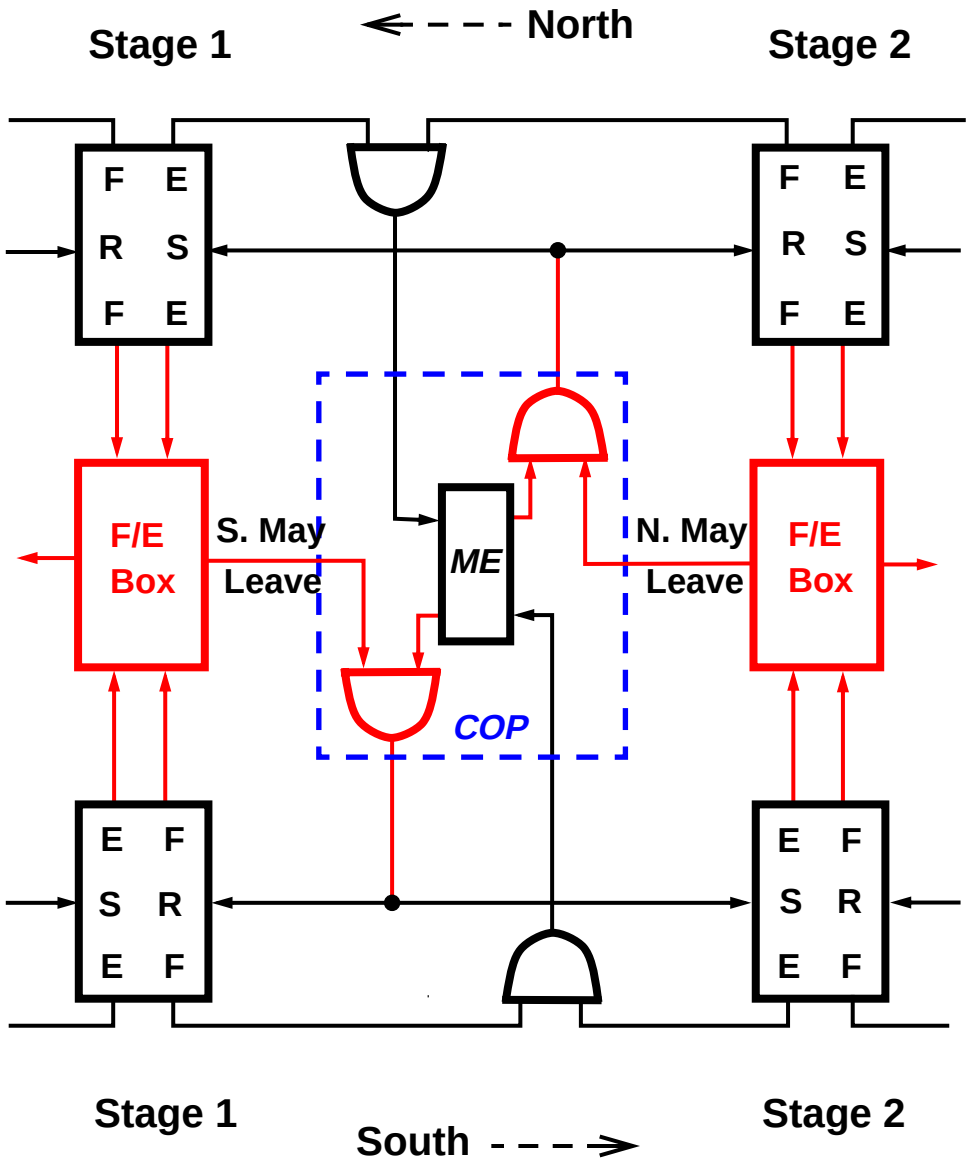
Basic asP Control Circuit*



Adding Mutual Exclusion

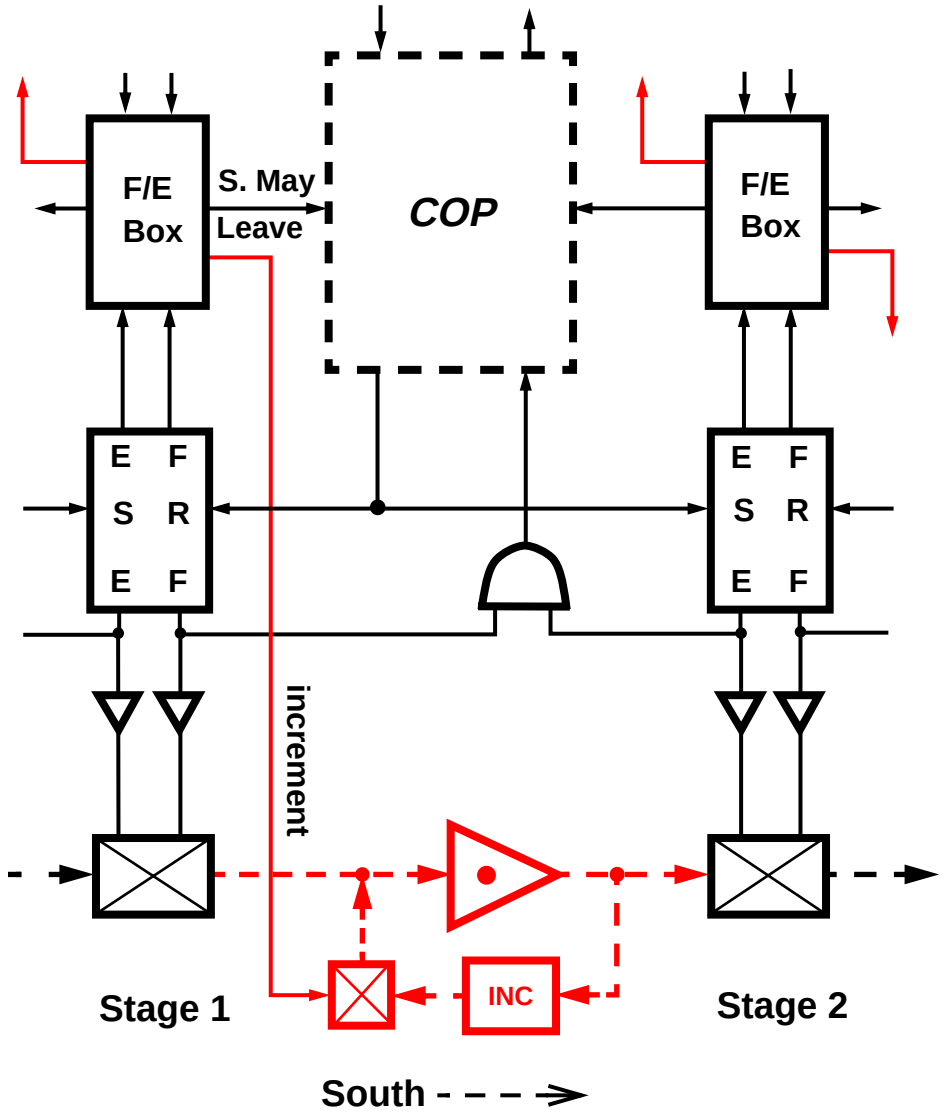


Adding Completion Dection



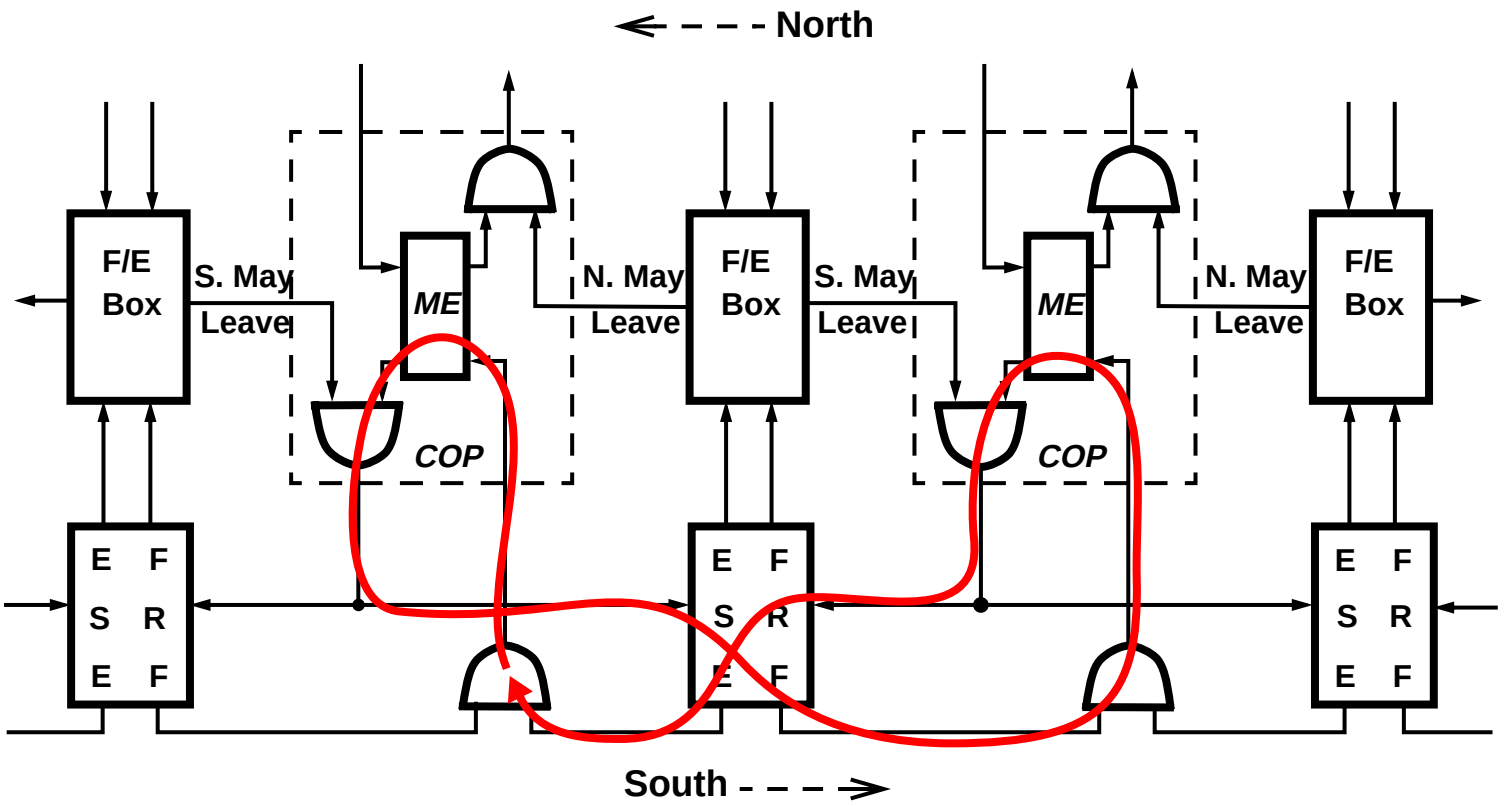
Adding the Data Path

- **One-latch loop for data increment**



Cycle Time Study

case	F/O4 delays	theoretical	measured
minimum cycle time	12	463 MDI/s	462(N) - 498(S) MDI/s (single)
+ matching (+ 2 * 2)	16	694 MDI/s	699 MDI/s (both)
+ increment (+ 2 * 5.5)	23	483 MDI/s	491 MDI/s (both)



External Test Interface

- No high-speed inputs
- High-speed outputs to measure speed
- Each stage is addressable

Simulation

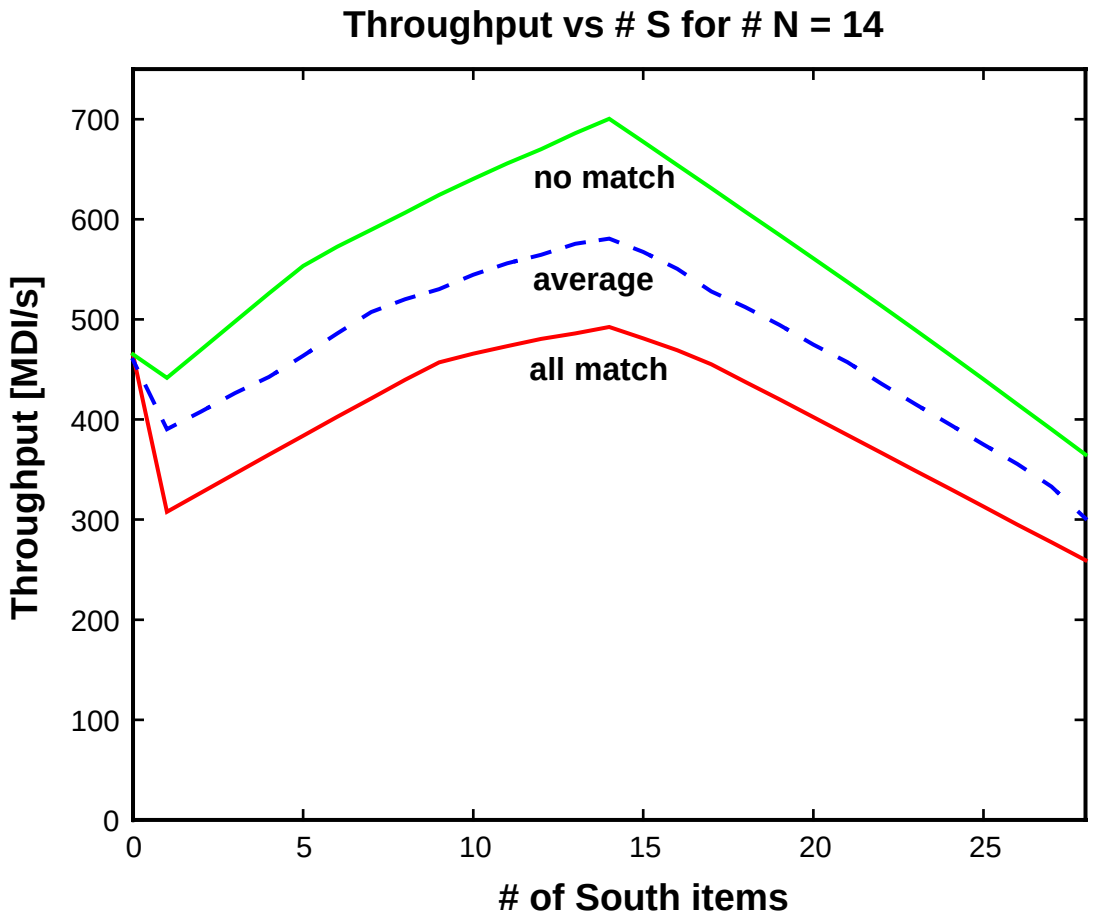
- IRSIM and verilog for chip-level simulation
- Spice circuit simulation for timing verification

Implementation

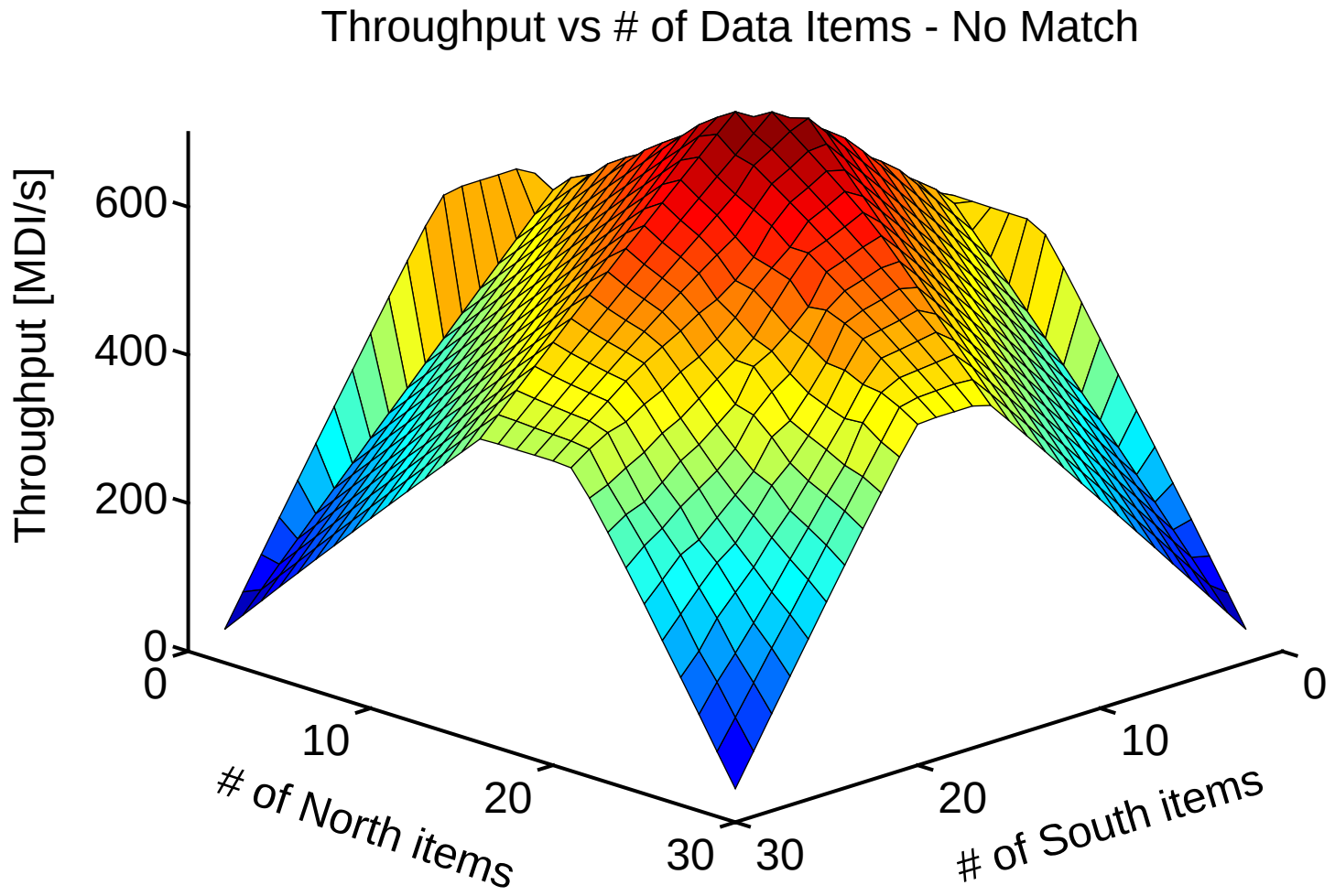
- Test chips fabricated on two separate 0.6μ MOSIS runs

2-D Throughput vs Occupancy Example

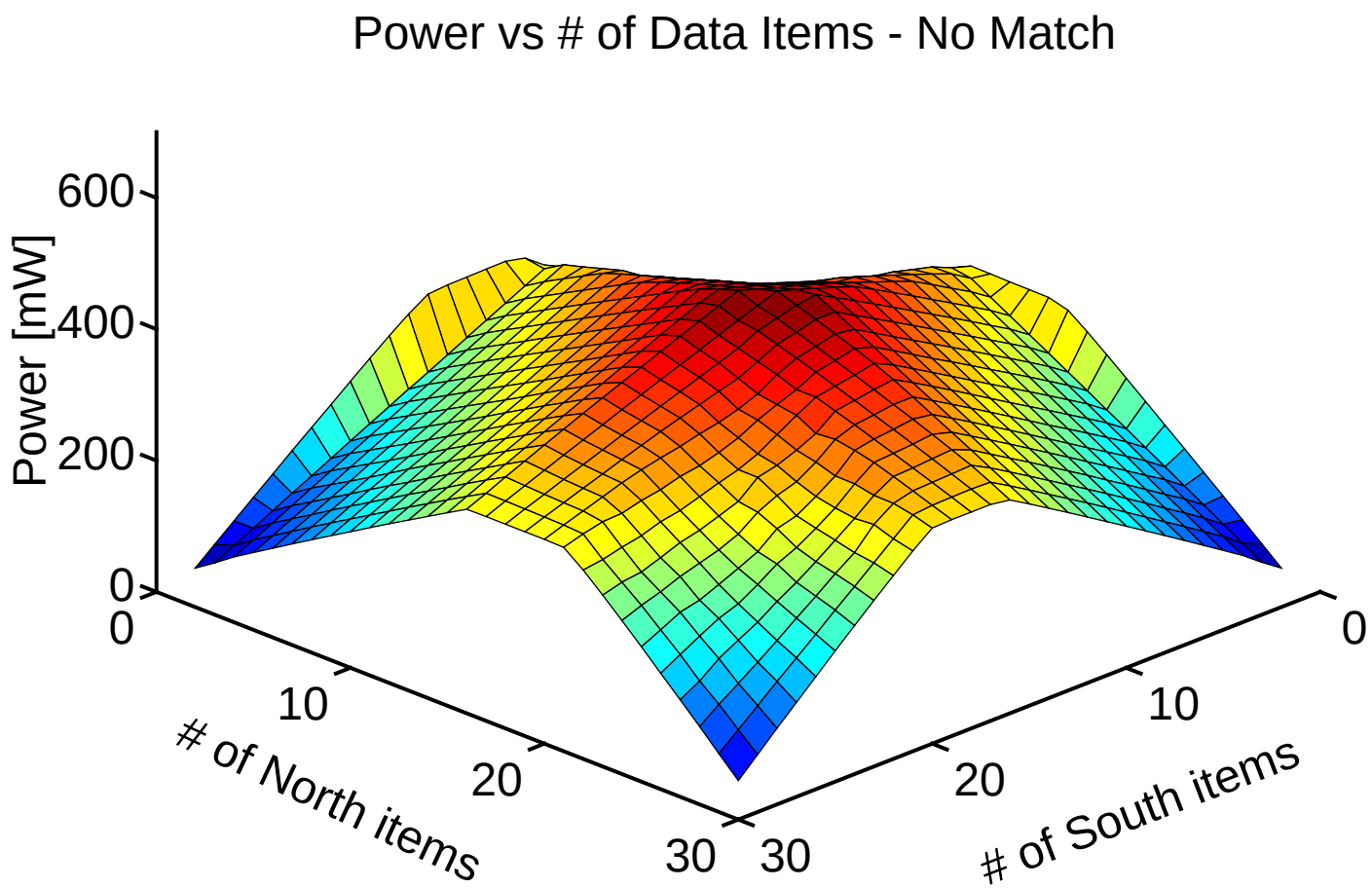
- **“average” case: only 1/4 of meetings result in a match**



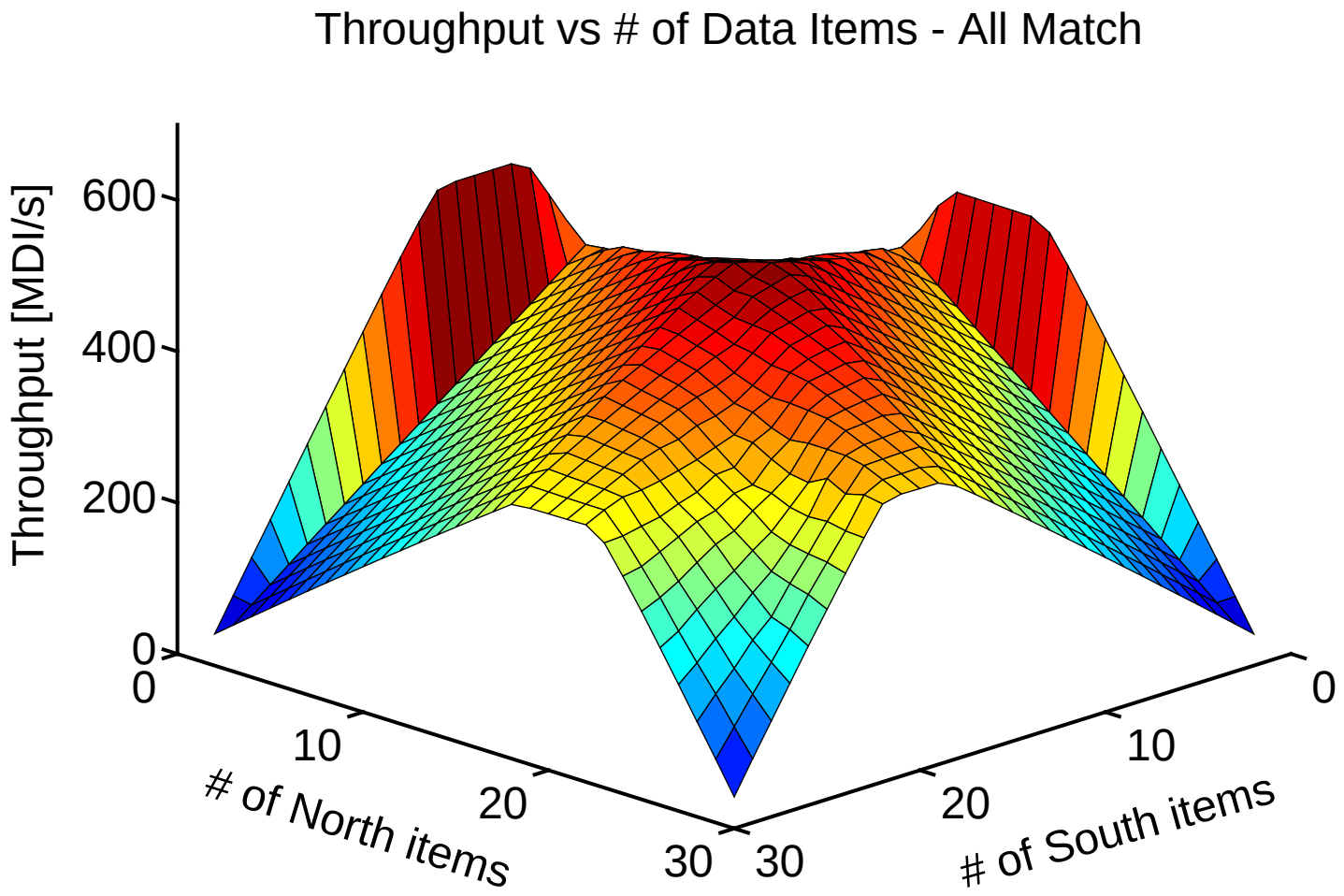
Total Throughput vs Occupancy - No Match



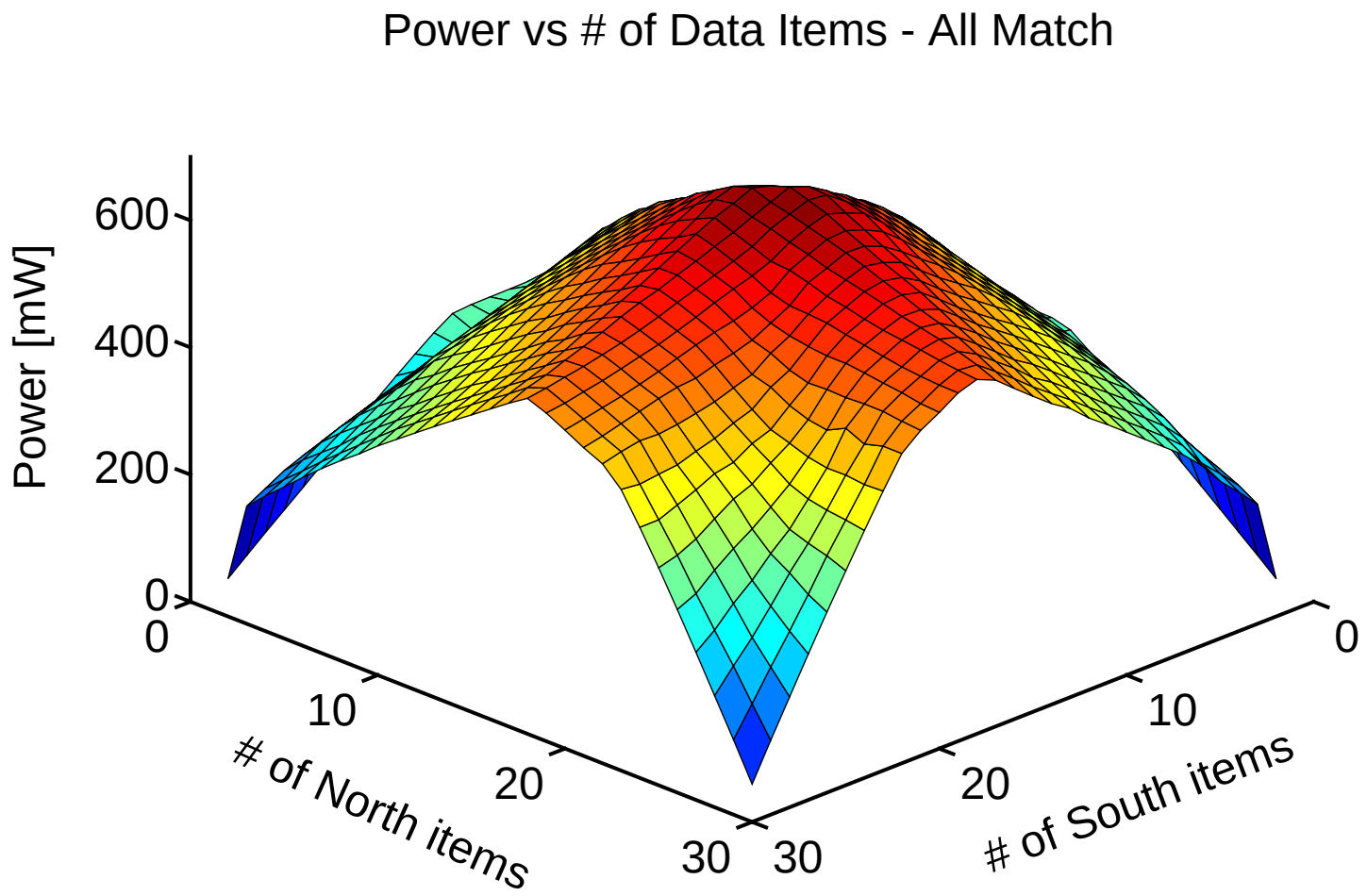
Total Power vs Occupancy - No Match



Total Throughput vs Occupancy - All Match

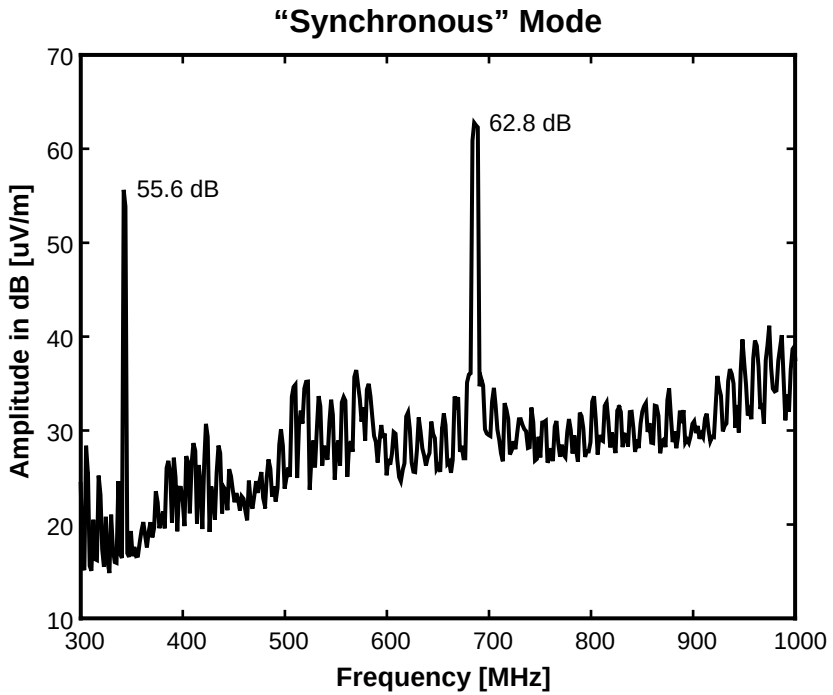


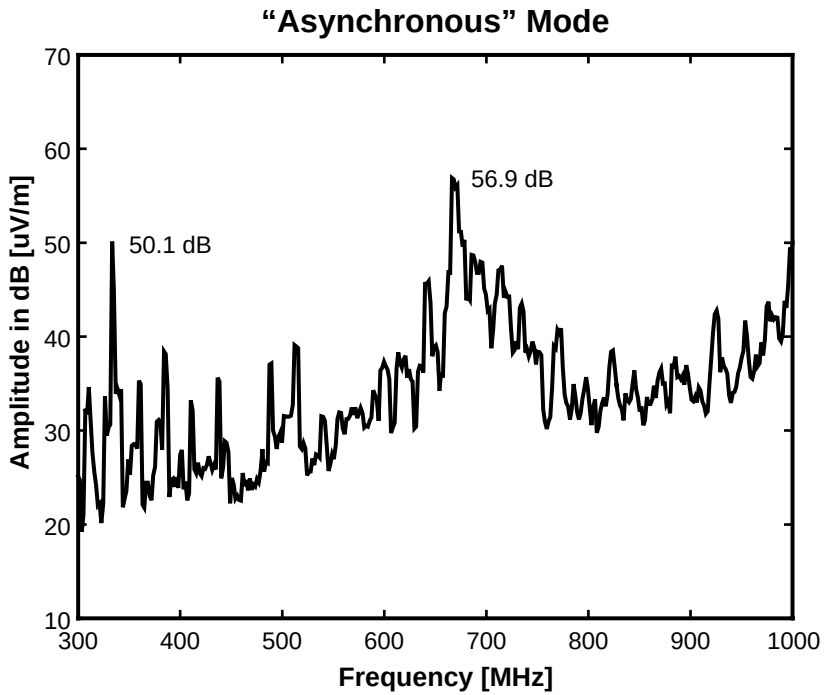
Total Power vs Occupancy - All Match



Electromagnetic Emission Spectra

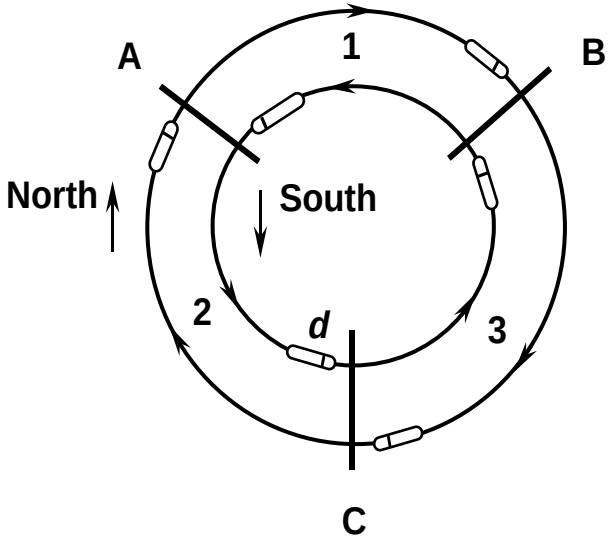
- **“synchronous” mode is N=14, S=14 (no matches)**
- **“asynchronous” mode is N=13, S=15 (six matches)**



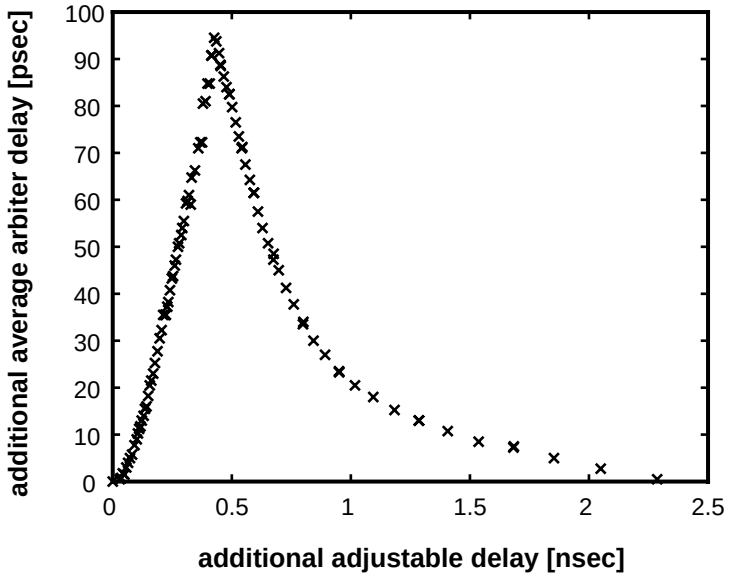


Stressing the Arbiter

- **3-stage counterflow pipeline ring with adjustable delays**
- **Can force one arbiter to be always contested**



Additional Average Arbiter Delay vs Delay Element Setting



Conclusions

- **asP* Design Style**
  - **Uses simple standard gate primitives [+]**
  - **Easy to include mutual exclusion and completion detection [+]**
  - **More delay constraints [-]**
- **Timing Constraints**
  - **Careful analysis of design required**
  - **Layout extraction necessary for accuracy**
- **EMC Tests**
  - **Can exhibit both “synchronous” and “asynchronous” modes**
  - **6 dB reduction shown in simple test case**

Conclusions (cont'd)

- **Demonstrated average case bahavior**
- **Predictions and measurements match closely**
- **Predictions for more complex pipelines**
- **Can we do better?**
- **Can counterflow architecture be competitive?**

Ongoing Research

- **More EMC work - “quasi-peak” measurement**
- **Timing analysis - parasitic extraction**
- **Operational “modes”**
- **Moving into new areas**

Full Cycle Time - Checkerboard Pattern