DESIGNING FAST ASYNCHRONOUS CIRCUITS

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Presentation Outline

- **Design Flow Overview**
- **Logical Effort**
- **Loop Circuits**
- **Width Calculation Method**
- **Micropipeline Example**
- **Conclusions**

Design Flow Overview

1. Assume Uniform Delays

2. Design Control Logic

- equal number of gates / loop (3/5)
- use gates with low logical effort
- break complex loops into simple parts

3. Extract Wire Lengths

4. Balance Transistor Widths

5. Double-Check with Spice

Logical Effort

***g* = logical effort**

***h* = electrical effort = C_{out} / C_{in}**
(step-up)

***p* = parasitic delay**

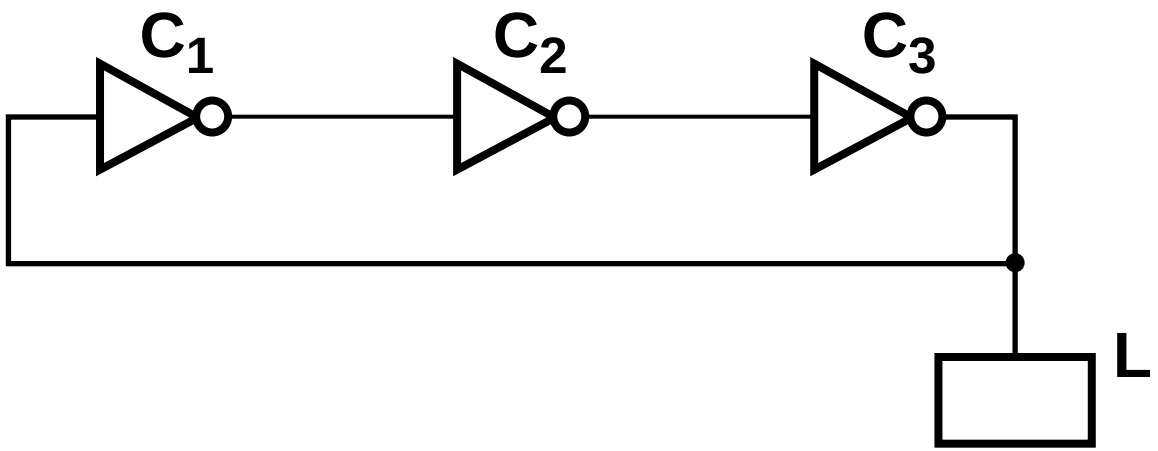
d* = *g* ∗ *h* + *p

***f* = *g* ∗ *h* = total effort**

***X* = effort expectation**
(stage effort)

Loop Circuits

3-stage inverter loop with load

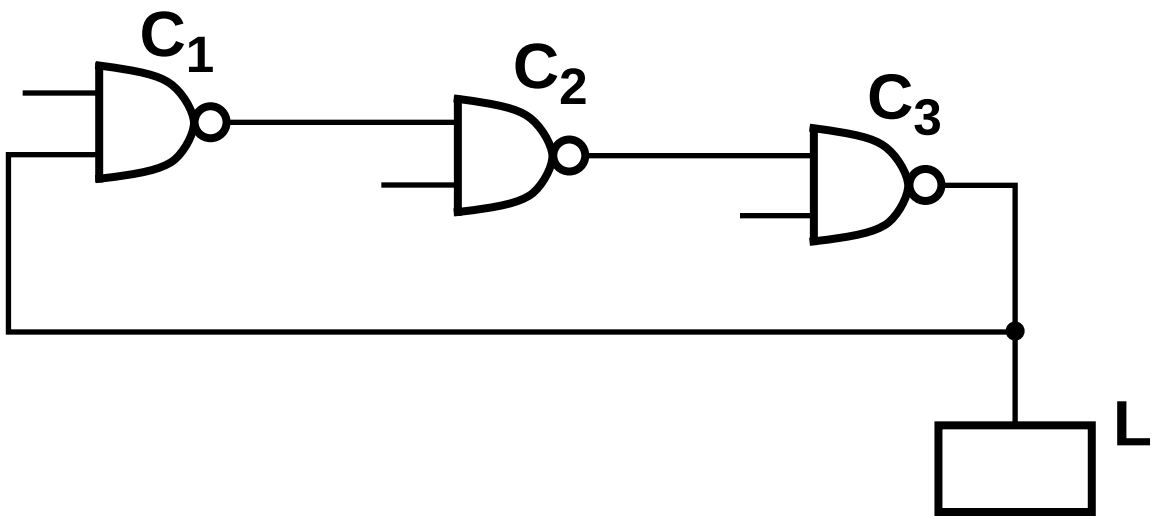


- If L = 0, any size inverter is fine
- For non-zero L and reasonable h_j, $C_1 \ll L$
- This is the simplest self-resetting circuit

Loop Circuits (cont'd)

Sun microsystems

3-stage NAND gate loop with load



now $f_j = g_j h_j$ or $h_j = \frac{f_j}{g_j}$

If g_j is small, then want h_j large and vice versa

Effort Expectation, X

Effort expectation (stage effort) is how much work each gate is expected to do

$$X^n = \prod(f_j)$$

$$C_1 = \frac{L\prod(g_j)}{X^n - \prod(g_j)}$$

min X, $X^n = \prod(g_j)$ is independent of L!

Effort Expectation (cont'd)

Sun microsystems

Choosing Effort Expectation, X

Large X:

- smaller transistors
- lower speed
- lesser area and power consumption

Small X:

- larger transistors
- higher speed
- greater area and power consumption

Automatic Width Calculation

Two models of each primitive gate:

1. Width model for size calculation

- **contains only current sources and resistors**
- **simulates very quickly in spice**
- **measured voltage gives transistor size**

2. Analog model for functional simulation

- **output is typical analog waveforms**

All except lowest level of hierarchy is common to both models

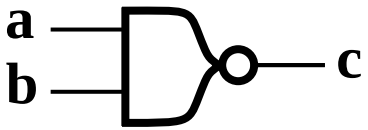
Automatic Width Calculation (cont'd)

Width model

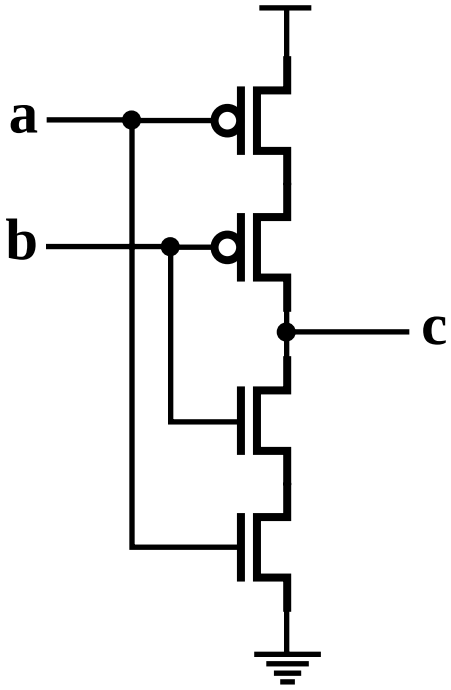
- **capacitive load represented by current**
- **1 amp = 1μm of transistor gate**
- **logic inputs => current sources**
- **logic outputs => current sinks**

Note that this is <u>backwards</u> from what you might expect

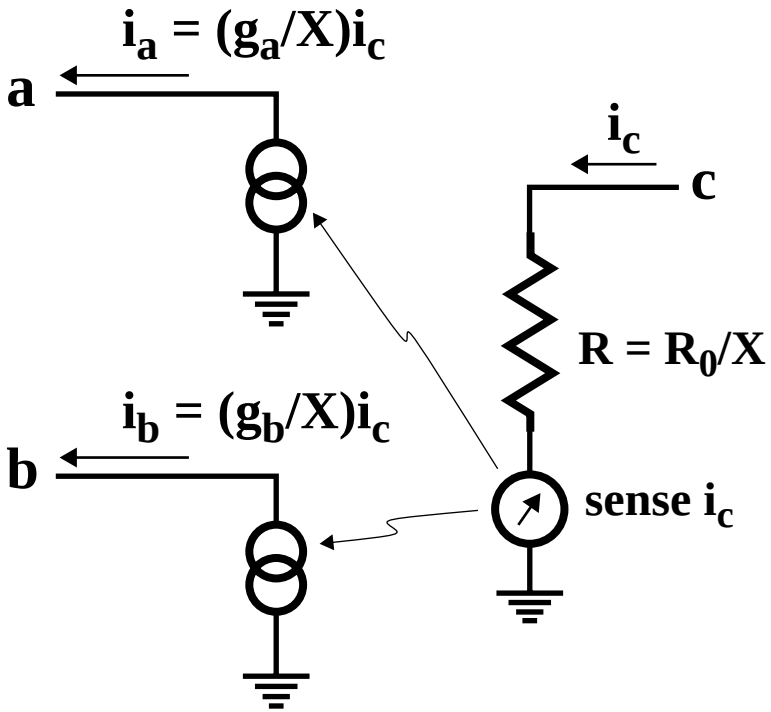
Gate Models



icon



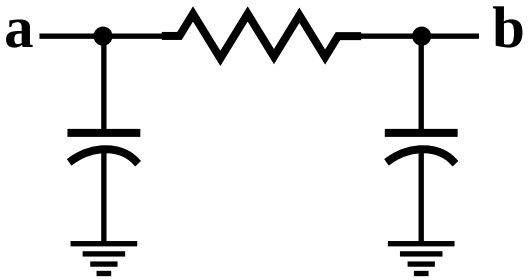
analog model



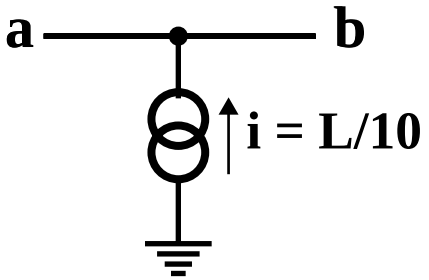
width model

Wire Models

icon



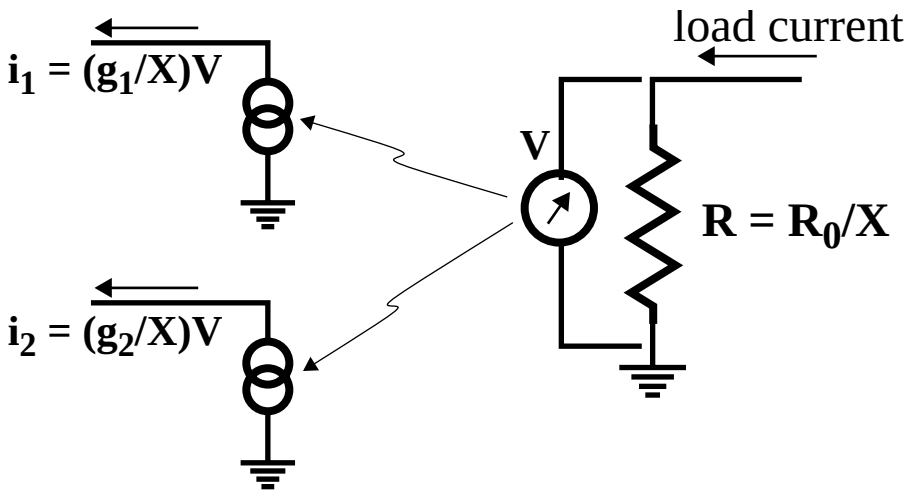
analog model



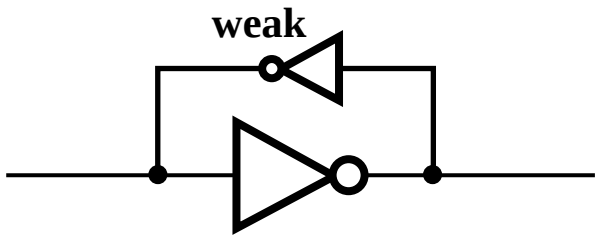
width model

Special Cases

Multiple drivers



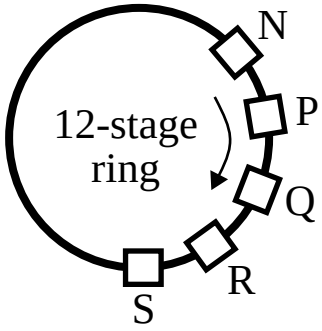
Keepers

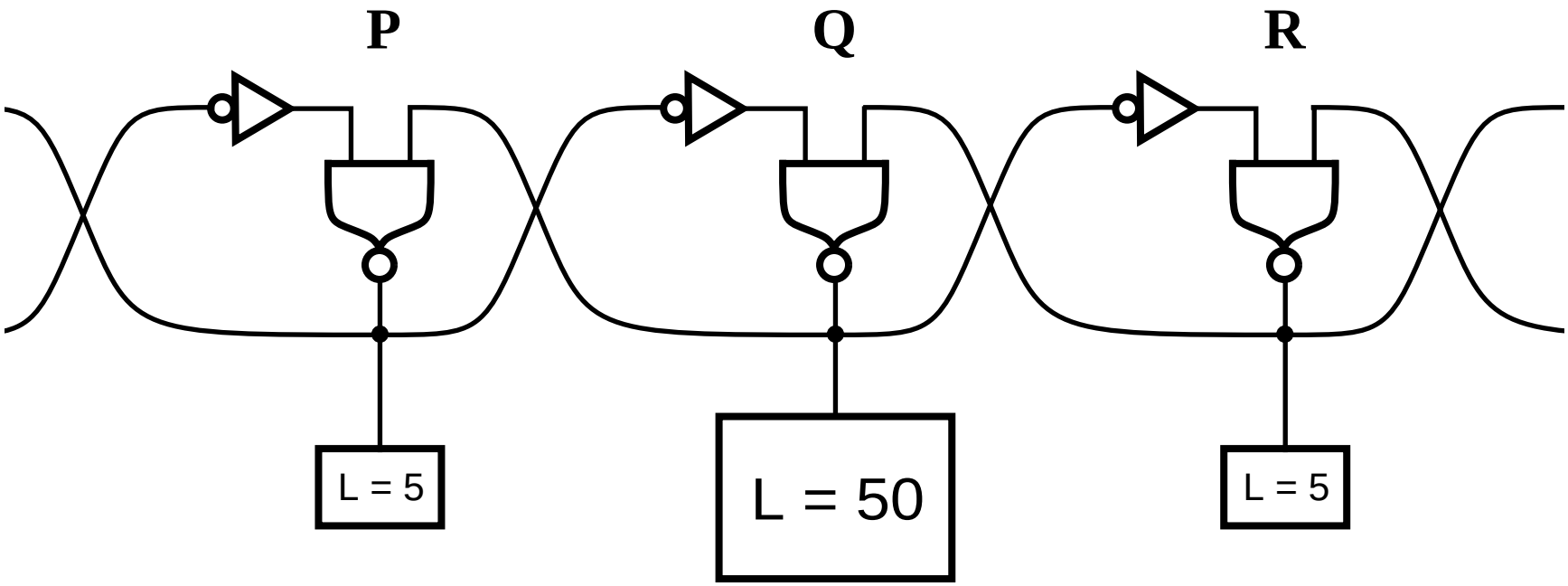


Minimum layout width

Fixed size gates

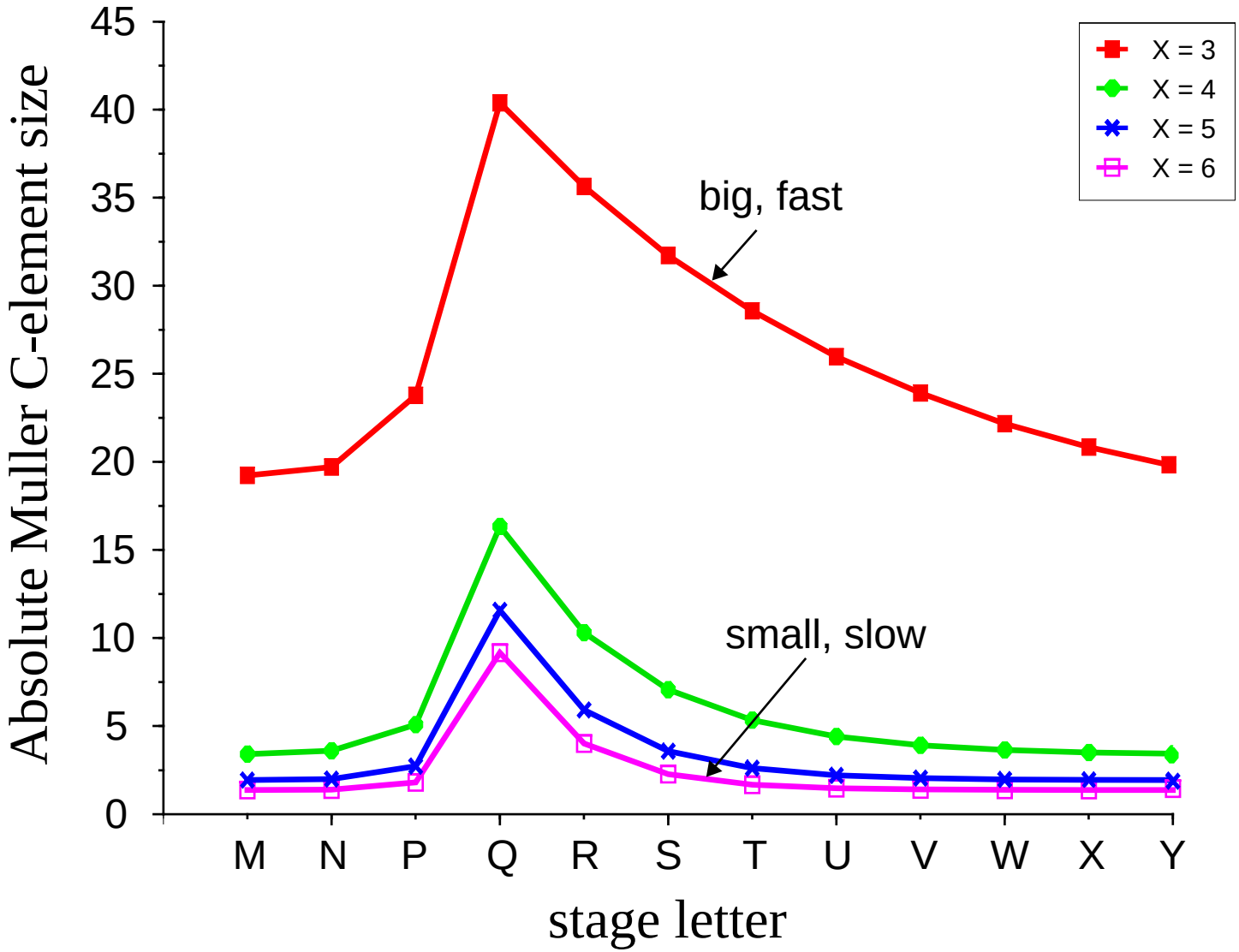
Micropipeline Example



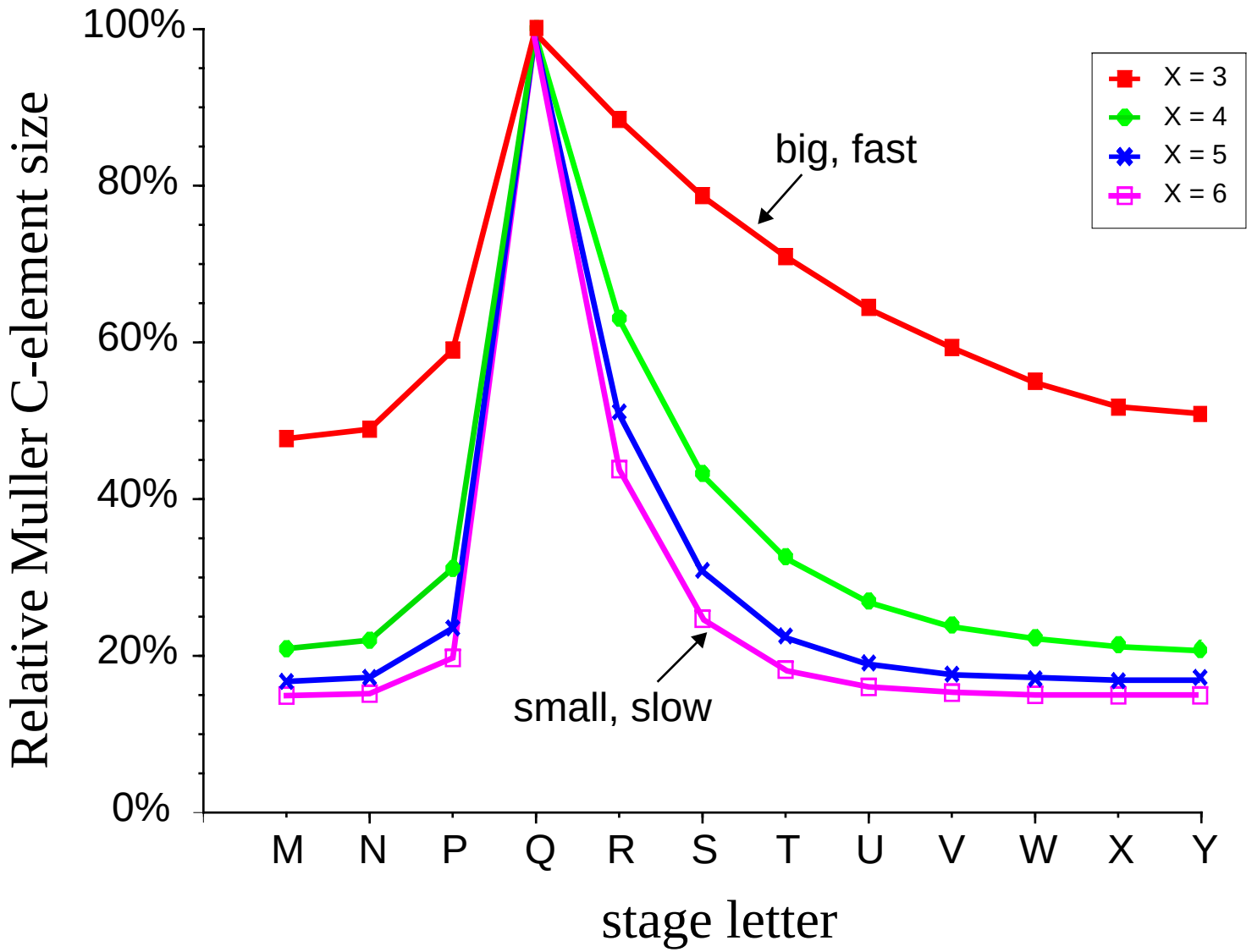


$$w_i = \frac{1}{X}\left[L_i + \frac{2w_{i+1}}{X} + 2w_{i-1}\right]$$

Micropipeline Example (cont'd)



Micropipeline Example (cont'd)



Conclusions

Design Flow:

1. Assume Uniform Delays
2. Design Control Logic
3. Extract Wire Lengths
4. Balance Transistor Widths
5. Double-Check with Spice

Conclusions (cont'd)

Uniform delay assumption makes design easier and encourages simple logic

Balancing transistor widths is easy

- **hand**
- **spreadsheet**
- **spice**
- **(integrated tool)**

Estimating wire loads is hard

Method is supported by chip successes