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How Big Should a Printed Circuit Board Be?

IVAN E. SUTHERLAND AND DONALD OESTREICHER

Abstract—**This correspondence outlines a theory for choosing printed circuit board dimensions in order to avoid crowding of printed wiring. Given a number of components to be mounted on the board and the dimensions of wiring, the theory predicts a minimum board size that should be easy to lay out. The theory does not tell how many components should be put on a board.**

The theory is based on a random placement model. The model seems to approximate the situation in complicated logic nets and provides an upper bound for more regular data-path circuitry. If moderately intelligent routing is combined with the random placement model, the expected number of wires crossing any center line of the board turns out to be ¼ of the number of active circuit pins, almost regardless of net size.

The theory predicts that for random placement, the board area required per component increases as the number of components increases and, therefore, that big boards are less efficient than small ones. The theory shows that the dual-in-line package (DIP) now in standard use is no worse than other possible pin configurations from the point of view of printed circuit board area required. Minimum board area for any component pin configuration is obtained with square boards, but the number of rows and columns in an optimum component array depends on the pin configuration of the individual components.

Index Terms—**Circuit board layout, component placement, wire routing.**

Introduction

We were recently faced with the task of establishing a new set of parameters for a new line of printed circuit boards. Manifold opportunities for choice were available. We could put as many or as few circuits on the board as we chose, we could provide as many or as few card-edge connector pins as we thought wise, and we could make the board any shape we thought desirable.

A lasting choice of board parameters was required. A family of printed circuit boards will be used for many years in a wide variety of functions, many of them unanticipated. Having established the overall board size and the number of components allowed on a board, its designers will make a substantial investment in computer layout programs, basic artwork patterns, inspection methods, stuffing equipment, flow soldering jigs, etc. Because the choices of basic board parameters must last, and because there is inadequate real information on which to base the choices, one must exercise "wisdom" rather than "science" in their execution. Wisdom is the art of making, in the face of inadequate knowledge, choices that will stand the test of time. Unfortunately, wisdom is so rare that we would far prefer to substitute science for it.

Our previous efforts at choice of board size proved inadequate in several respects: replacement cost was too high, and dimensional accuracy was too difficult to check but primarily, the circuits proved to be too difficult to lay out in printed circuit form. The new design would require enough board area to make printed circuit layout easy, but should still preserve some measure of economy. We needed to provide enough but not too much printed circuit board area for the number of components chosen, and we needed an arrangement of card-edge connectors and component locations conducive to easy wiring layout.

The great variety of printed circuit board types in use suggests that there is relatively little agreement about the size of printed circuit boards, the number of components on them, the spacing between and orientation of the components, and the size and placement of card-edge connectors. Some designers seem to prefer short wide cards, some seem to prefer tall narrow cards (see Fig. 1). What are the relative merits of each of these choices? Given some design goals, what is the rational choice of card shape? How should components be oriented? We hope that this paper may be some help—certainly it provides some guidelines.

Objectives of the Theory

A theory of printed circuit board layout should provide guidelines for board parameter choice relatively independent of the circuits to be implemented on the boards. We would prefer a theoretical approach to a statistical one because we cannot be sure that the statistics for as yet undesigned circuits will match those of existing circuits for which measurements can be made. An adequate theory should provide an upper bound for board parameters to ensure that all circuits will be easy to lay out, since the cost of a single difficult or impossible layout task can be very high. The theory should be applicable to a wide variety of board designs and component package types. The theory should be equally applicable to two-sided boards and to multilayer boards.

Obviously, a good theory should correctly predict the observed ease with which some circuit boards can be laid out and the extreme difficulty of others. Among our own main empirical observations are these.

Observation 1: For a given intercomponent spacing, small boards are vastly easier to lay out than big ones.

Observation 2: Most boards seem to run out of wiring space in one dimension before running out in the other dimension. Card-edge connectors seem to contribute heavily to the dimension which first exhausts wiring space.

In fact, the theory presented here does predict these observed phenomena. It provides for closer spacing of components on small boards and provides for differential spacing in the horizontal and vertical directions so that the space available for horizontal and vertical runs will be exhausted simultaneously. Our limited experience has revealed no board design that is hard to lay out where the theory says it should be easy. There are, however, many circuits for which the theory provides more board area than absolutely necessary.

Random Versus Patterned Wiring

There seem to be two types of circuits: data-path circuits and control circuits. Data-path circuits are often characterized by repetitive patterns of circuit topology and, thus, repetitive patterns of wires on the printed circuit board. Data-path layout is extremely sensitive to component placement. Because components are often connected together in simple sequences, great savings in wire lengths are possible if the components are placed in corresponding order on the board. The wires on a data-path circuit board usually connect one component to its immediate neighbors. The layout has a high degree of regularity.

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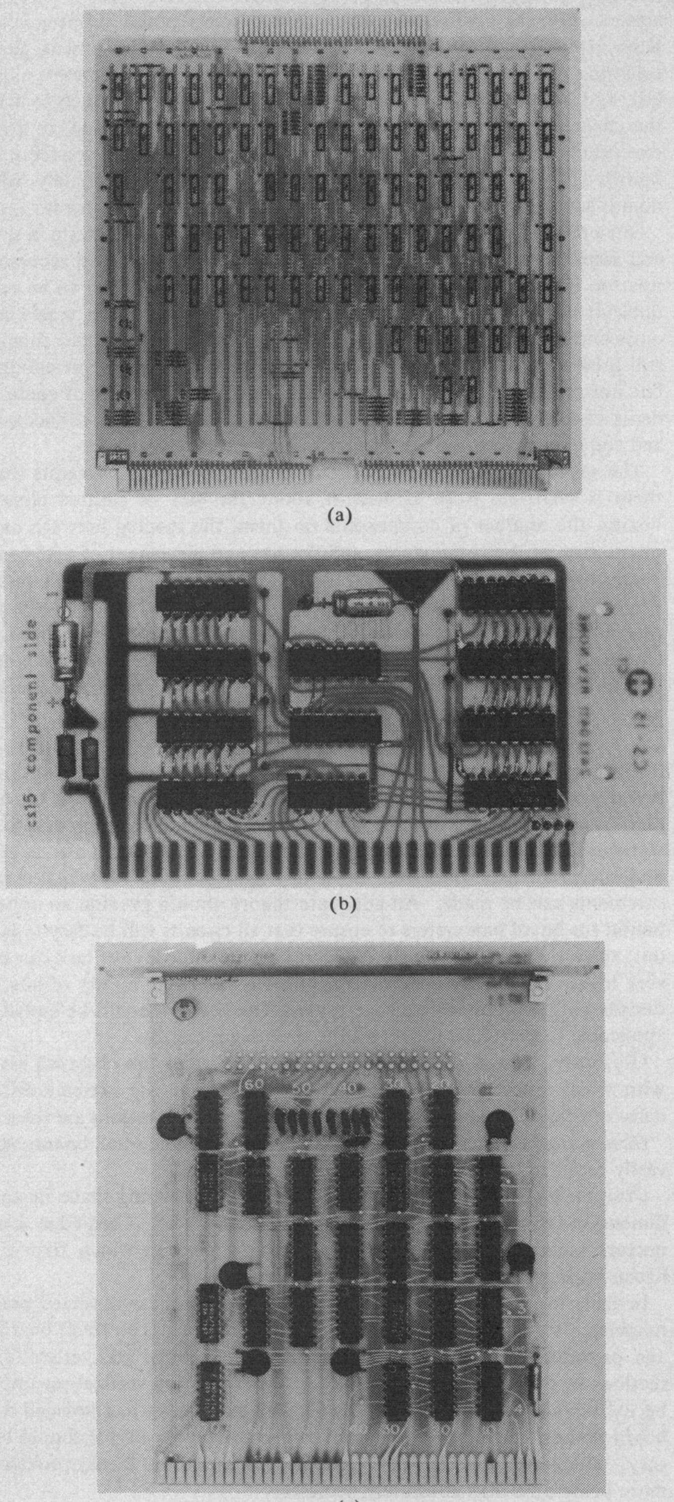

Fig. 1. Printed circuit boards come in many sizes and configurations.

On the other hand, control circuits seem almost to lack regularity. Logic nets in control circuits follow patterns dictated by the complex control functions that they implement. Individual signals serve a wide variety of functions and may be distributed to widely separated gates. Such circuits are very difficult to lay out, not only because optimum component placement is not much better than random component placement but also because the number and diversity of circuit connections is very large.

Our corporate circumstances dictate a heavy concentration on making

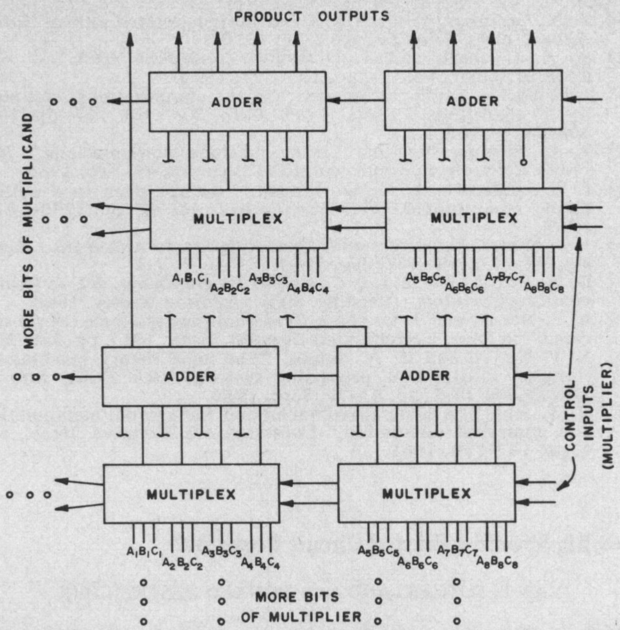

Fig. 2. An array multiplier—an example of highly patterned logic. Signals A, B, and C carry the bits of the multiplicand to all the multiplexers.

the control circuits easy to lay out. We often find that the design of data-path circuitry suggests optimum component placement during the design process. The array multiplier of Fig. 2, for example, suggests almost without effort a component placement that will result in a very short average wire length. On the other hand, the control circuitry for a machine is sufficiently complex in itself that the designer is saturated with just the logical considerations; he has no time or energy left over to consider component placement simultaneously. Moreover, design changes in control circuits are more prevalent; layout of control circuits is complicated by the lack of inherent regularity; and component placement is not nearly so obvious.

For these reasons we felt it reasonable to develop a theory based on random component placement with intelligent interconnection. We assume that each active circuit pin is equally likely to be in the same net as each of the other active circuit pins on the board, but that we are free to choose the order of connection, not necessarily linear. We assume a distribution of net sizes, some pins being connected in pairs, some in groups of three, of four, etc. We then discover where excessive crowding of wires is likely, and thus discover how much board area will be required.

Assuming random component placement is equivalent to saying that a change in component placement can be expected to have no effect on the wiring density or average wire length on the board. Obviously, the random placement model is not applicable to circuits that have a high degree of regularity, but it does provide an upper bound for them, since if judicious component placement is possible, using an optimum component placement can only help, not hinder subsequent wire routing. Our experience shows that for many control circuits careful component placement can obtain only small improvement over the random placement. The relatively rare cases where great circuit regularity permits greater packing density are not troublesome to lay out anyhow, and so we are willing to treat them as special cases to be handled on an individual basis.

Expected Number of Crossings

Given a net of randomly chosen active circuit pins to interconnect, we can compute the expected number of wires crossing any section of the board. By "net" we mean a set of pins to be electrically connected. By "section" we mean any line dividing the board into two parts. We are often interested in the "midsection," namely a section that divides the board into two equal parts horizontally or vertically. By "active circuit pins" we mean those involved in logic nets, as opposed to unused or power or ground pins.

If we let P_1 represent the fraction of active circuit pins on one side of the section and P_2 represent the fraction of active circuit pins on the other side of the section, then $P_1 + P_2 = 1$. For randomly chosen nets, the probability P_c that the interconnection wire crosses the section at least once is given by

$$P_c = 1 - P_1^n - P_2^n$$

where n is the number of pins involved in the net. P_1^n is the probability that the wire starts on one side of the section and connects only pins on that side, and P_2^n is the probability that the wire starts on the other side of the section and remains on that side.

The expected number of wires that must cross the section at least once can be found by multiplying the probability of crossing P_c by the total number of nets. If there are N active circuit pins total, then there are N/n nets, and the expected number of "essential crossings," wires that must cross the section at least once is

$$W = \frac{N}{n}(1 - P_1^n - P_2^n).$$

Obviously, the expected number of essential crossings reaches a maximum where $P_1 = P_2 = ½$. This corresponds to the notion that the most difficult section on a board is the section dividing the board into two equal parts. We will therefore choose our routing to have exactly one crossing per net for this most critical midsection.

It is interesting to examine the number of expected essential midsection crossings W_m as a function of net size n. These results are summarized in Table I. Here we see that for nets of two or three pins, the expected number of essential midsection crossings is exactly ¼ of the number of active circuit pins. For larger nets, the expected number of essential crossings is slightly smaller, decreasing gradually to a single essential crossing if a single net connects all pins.

The expected number of essential midsection crossings for nets with four or more pins is actually slightly higher than shown because either the horizontal or vertical midsection for such nets will require two crossings rather than one. Computations that account for this coupling are shown in the Appendix. These corrections bring the expected number of essential crossings closer to $N/4$.

The theory, then, rests on the simple observation that for nets of practical size the expected number of essential midsection crossings is approximately $N/4$. By using this simple observation, it is possible to make boards sufficiently large to accommodate these wires in both horizontal and vertical directions and thus ensure that boards will be easy to lay out. Some statistical justification for this approximation comes from a study of 30 board types which shows that relatively few nets with 5 or more pins are found in "typical" TTL circuitry.

TABLE I
EXPECTED NUMBER OF ESSENTIAL MIDSECTION CROSSINGS AS A FUNCTION OF NET SIZE

Net Size	Expected Crossings per Net	Expected Crossings
n	$C = 1 - P_1^n - P_2^n$	$W_m = \frac{N}{n}(1 - P_1^n - P_2^n)$
2	$1 - 1/2^2 - 1/2^2 = 1/2$	$\frac{N}{2} \times 1/2 = \frac{N}{4} = 0.25N$
3	$1 - 1/2^3 - 1/2^3 = 3/4$	$\frac{N}{3} \times 3/4 = \frac{N}{4} = 0.25N$
4	$1 - 1/2^4 - 1/2^4 = 7/8$	$\frac{N}{4} \times 7/8 = \frac{7N}{32} = 0.2185N$
5	$1 - 1/2^5 - 1/2^5 = \frac{15}{16}$	$\frac{N}{5} \times \frac{15}{16} = \frac{15N}{80} = 0.188N$
N	1	$\frac{N}{N} \times 1 = \quad = 1$

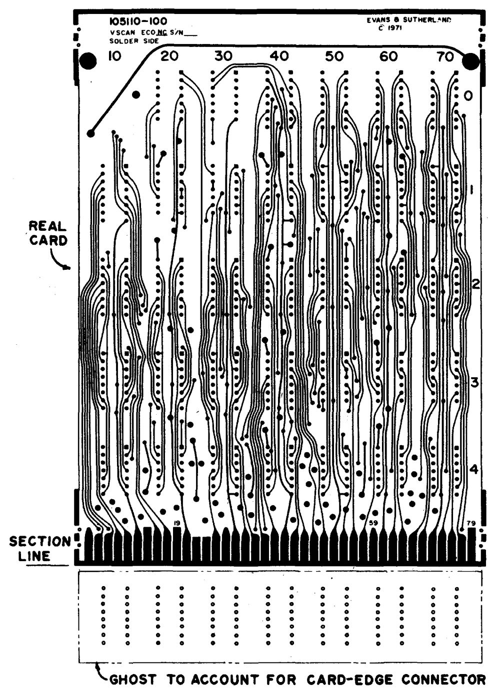

Fig. 3. Wires at the card-edge connector can be thought of as going to additional components on a "ghost."

ACCOUNTING FOR THE CARD-EDGE CONNECTOR

There are two ways to account for the card-edge connector: as a part of the active circuitry, or as a set of connections to additional circuitry off the board. If one treats the card-edge connector as a set of connections to additional off-the-board circuitry, one must make additional computations. As we shall see, these computations very nearly approximate the simpler situation.

A board with card-edge connector could be considered to be a part of a larger board cut at the card-edge connector location. Wiring on the larger board would be identical to that on the smaller board if the cut were made in such a location that the expected number of essential crossings at the section exactly equals the number of active card-edge connector pins. Such a situation is shown in Fig. 3. Thus, the board consists of two parts, the "real" part, with its given amount of circuitry, and the "ghost" part with just enough circuitry to account for as many wires as are required by the card-edge connector.

If the ghost part is small with respect to the total, then the expected number of essential crossings at the card-edge connector section will equal the number of active circuit pins in the ghost, since the probability of a net remaining entirely on the ghost side will be small. If, on the other hand, the ghost is about equal in size to the real part of the board, then the expected number of essential crossings at the card-edge connector will be ½ of the total number of active circuit pins on the real side (¼ of the total of both real and ghost). Thus, we can decide whether the ghost is large or small with respect to the real side by looking at the number of card-edge connector pins with respect to the total (real) active circuit pins involved. If there are half as many card-edge pins as active circuit pins, the ghost is large; if there are fewer than ⅕ as many card-edge pins as active circuits pins, then the ghost is small. On most practical printed circuit boards, the ghost is small. Thus, in most cases the card-edge pins can simply be treated as if they were active circuit pins.

HOW MUCH SPACE IS AVAILABLE—WIRING GEOMETRY

Given a geometry of the circuit components used and some conventions on wire size, it is easy to figure out how many wires can be placed vertically or horizontally in a given space. We have found it convenient to think of the pad space near each component pin as "blocking" some wires that might otherwise run there. Thus, the number of available wires can be computed on the basis of some number of wires per inch times the available width minus the number of wires blocked by the component pins. A typical geometry for 30 wires per in is shown in Fig. 4. 30 wires per in is particularly convenient for such computations because precisely two wires are blocked by each pad and every third wire is permitted to pass between adjacent pads on the conventional 1/10-in spacing. Using this geometry, the number of available vertical wires W_v and the number of available horizontal wires W_h is given as a function of board dimensions V and H and the number of rows R and columns C of components as

$$W_v = CW_c = 30H - 4C \quad \text{and} \quad W_h = RW_r = 30V - 16R.$$

We have found that for 14- or 16-pin dual-in-line digital circuits of low- or medium-scale integration, ten active pins per integrated circuit package is a good rule of thumb. If we apply this rule of thumb, the number of vertical wires per column W_c crossing the horizontal midsection of the board will depend on the number of packages in that column.

$$W_c = \frac{N}{4} = \frac{10R}{4} = 2.5R$$

and

$$W_r = \frac{N}{4} = \frac{10C}{4} = 2.5C.$$

Notice the interrelation of the column and row parameters. As more circuits are put in each column to make the board taller, each column will require more vertical wires, thus forcing the columns further apart. Similarly, as more circuits are put in each row to make the board wider, each row will require more horizontal wires, thus forcing the rows further apart. Thus, as more circuits are added to the board, the area *per circuit* will also increase, representing a loss of board efficiency.

At this point we might well ask what component configuration will provide a minimum board area given a certain number of components. As we shall see, the shape factor of the dual-in-line package (DIP) establishes the configuration of components, and the minimum board area is obtained when the horizontal and vertical board dimensions are equal. If we write an expression for the minimum required horizontal dimension H_m and minimum required vertical dimension V_m as a function of the number of rows and number of columns of components, we find

$$2.5RC = W_v = 30H_m - 4C$$

and

$$2.5RC = W_h = 30V_m - 16R$$

or

$$H_m = \frac{2.5RC + 4C}{30}$$

and

$$V_m = \frac{2.5RC + 16R}{30}.$$

And the corresponding board area

$$A_m = H_m \times V_m = \frac{RC}{900}(2.5^2RC + 2.5 \times 16R + 2.5 \times 4C + 64)$$

is minimized when $C = 4R$. Note that at minimum board area, the values of H_m and V_m are exactly equal. This corresponds to the notion that the minimum probable wire length will be obtained with a square board!

The fact that minimum board area requires four times as many columns as rows came about from the fact that a 16-pin DIP blocks four times as many horizontal as vertical wires. Suppose one were to use some other configuration of pins on the package, say a 4 X 4 array; would the minimum board area be smaller? The answer, remarkably enough, is no; the same minimum board area would apply, though the number of rows and columns of such square packages would be equal. The equations for the 4 X 4 square package shown in Fig. 5 are

$$2.5RC = W_v = 30H_m - 8C$$

and

$$2.5RC = W_h = 30V_m - 8R$$

or

$$H_m = \frac{2.5RC + 8C}{30}$$

and

$$V_m = \frac{2.5RC + 8R}{30}$$

giving a board area

$$A_m = H_m \times V_m = \frac{RC}{900}(2.5^2RC + 2.5 \times 8R + 2.5 \times 8C + 64).$$

Thus, we can conclude that the arrangement of pins in an integrated circuit package has no effect on the total board area required, provided only that the integrated circuit pins fill every location where both vertical and horizontal wires are blocked. In other words, any completely filled rectangular array is equally satisfactory.

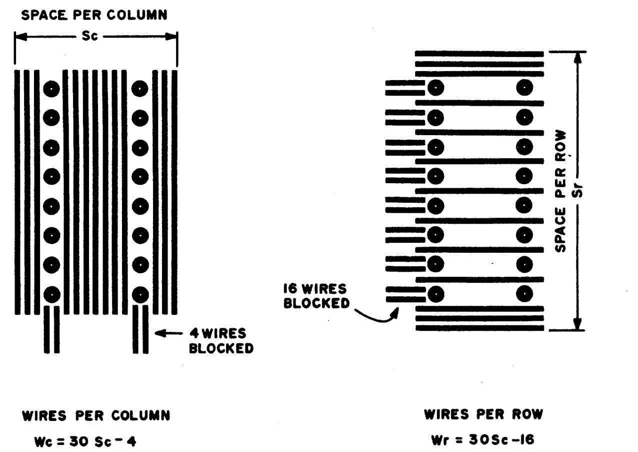

Fig. 4. Wiring geometry without power and ground—30 wires per inch; approximately 15-mil wires with 15-mil spaces; approximately 50-mil pads.

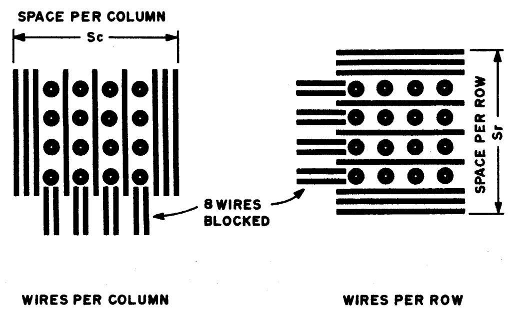

Fig. 5. Alternate pin configuration for 16-pin integrated circuits. This configuration provides the same board efficiency as the conventional 2 X 8 arrangement.

A Practical Example

We have found that in working a particular problem, tables of allowable configurations are often useful. Obviously, the number of rows and the number of columns of circuits must come out to be integers, and so one has only a finite number of choices of board configuration. Moreover, the expressions for width per column and height per row are

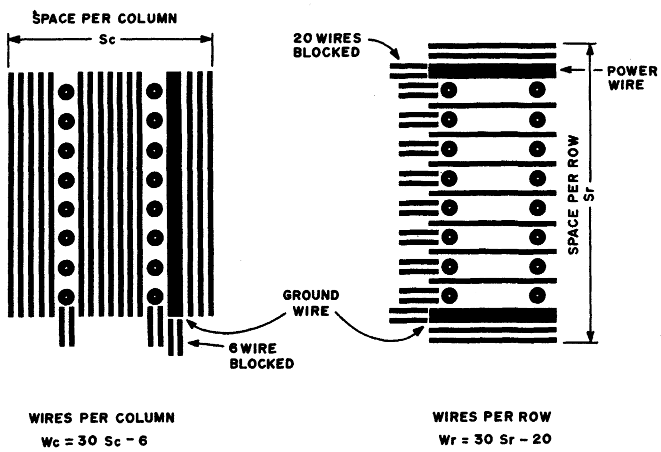

Fig. 6. Wiring geometry, including power and ground wires.

TABLE II
SOME CONFIGURATIONS OF BOARDS 5.25 IN WIDE

Number of Columns	Available Vertical Wires	Maximum Allowable Circuit Pins	IC Connections	IC Count ($R \times C$)	Number of Rows	Wires per Row	Height per Row	Board Height	Board Area	Cost (Area per Circuit)
C	$W_v = 150 - 60$	$N_t = 4W_v$	$N_{IC} = N_t - 70$	$I = \frac{N_{IC}}{10}$	$R = \frac{I}{C}$	$W_r = \frac{C \times 10}{4}$	$S_r = \frac{W_r + 20}{30}$	$V = S_r \times R$	$A = 5.25V$	$E = \frac{A}{I}$
1	144	576	506	50	50	2.5	0.9	46	242	4.84
2	138	552	482	48	24	5	0.9	22.6	119	2.48
3	132	528	458	46(45)	15	7.5	0.9	14.5	76	1.69
4	126	504	434	43(44)	11	10	1.0	12	63	1.43
5	120	480	410	41(40)	8	12.5	1.08	9.64	50.6	1.27
6	114	456	386	39(36)	6	15	1.17	8.02	42.1	1.17
				(42)	7	15	1.17	9.19	48.2	1.15
7	108	432	362	36(35)	5	17.5	1.25	7.25	38.1	1.09
8	102	408	338	34(32)	4	20	1.33	6.32	33.2	1.04
9	96	384	314	31(27)	3	22.5	1.42	5.26	27.6	1.02
10	90	360	290	29(30)	3	25	1.5	5.5	28.9	0.963
11	84	336	266	27(22)	2	27.5	1.58	4.16	21.8	0.991
				(33)	3	27.5	1.58	5.74	30.1	0.912
12	78	312	242	24	2	30	1.67	4.34	22.8	0.95
13	72	288	218	22(26)	2	32.5	1.75	4.5	23.6	0.91

actually nonlinear since it is not practical to space components more closely than their own physical dimensions.

The particular example which we will show here came about from the choice of a certain connector. Because of the connector dimension, we knew that the board should be 5.25 in wide. We also knew that we wanted about 25 to 40 integrated circuit packages on the board. As shown in Fig. 6, we had decided to provide power and ground in double-width horizontal wires associated with each row and ground in a double-width vertical wire associated with each column. 70 of the 80 connector pins were to be available for signal use; the remaining ones grounded. Given these conditions, we were able to describe all allowable configurations of components as shown in Table II.

The nonlinear nature of the computations shows up well in Table II. Notice that height per row is never allowed to be less than 0.9 because that is the minimum spacing that the package size will tolerate. Notice also that no more than 13 columns were plotted because at the minimum horizontal spacing of 0.4 in, no more columns will fit. We have arbitrarily added 1 in to the height of the board to account for the card-edge connector and the space for labeling the card at the top.

The choice of board dimensions now, once again, reduces to a matter of wisdom, but at least we have a set of alternatives any of which will be satisfactory from the ease of layout point of view. The tradeoff has been reduced to a choice between the number of circuit components we want on the board versus the area required per component. Having noticed that board efficiency improves only slightly below 6 or 7 columns and having in mind that 35 circuits is a good number for other reasons, we chose the 7 column design shown in Fig. 3.

CONCLUSIONS

The random placement theory provides a measuring stick against which any board may be judged. While it is obviously not necessary to provide as much wiring space as the random placement theory predicts, any scrimping on board space may result in difficulty in layout. We have found that our old boards (with space for 25 percent fewer midsection crossings than the theory recommends in the 70 DIP size) are nearly impossible to lay out when full of control logic, but quite satisfactory for data-path circuits, and quite satisfactory for control logic if not full of DIP's. In our new board design, we have chosen not to scrimp on board space, and have been well pleased with the ease of layout that has resulted.

The theory has correctly predicted that boards with more circuits on them require more board area per circuit. It is easy to convince oneself that the more dimensions in which one can run interconnections, the shorter each wire can be and, therefore, the less board area is required. Circuits wired in three dimensions would be better than those wired in merely two, but would be inordinately hard to service. Convolutions in the overall two-dimensional wiring structure serve as a part-way measure towards three-dimensionality; thus we see the common arrangement of cards plugged into a back panel. One might well choose a double-convolution structure of small cards on medium-sized ones on a panel to further reduce wire length and, thus, board area.

Interestingly enough, the theory shows that the minimum board area is obtained with a physically square board rather than with a square array of components. The minimum area board will have an array of components whose aspect ratio corresponds to the aspect ratio of the individual pin configurations of the components. It is good to know that the DIP is not any worse than a 4×4 square package would be.

Unfortunately, there are more considerations to layout than just the simple-minded computations presented here. Designers can still claim to be exercising good judgment to choose sizes and shape factors not approved by this theory. In our own design choice, for example, we felt that the difficulty of running wires horizontally through a forest of pins was prohibitive. We were influenced somewhat by our fear of the difficulty of utilizing all of the available horizontal wiring space because of the congestion of pins facing horizontal wires. We hope that more experience with automatic layout may lead to refinements of the random placement theory to account for such congestion.

Appendix

Expected Number of Essential Midsection Crossings Considering Horizontal/Vertical Coupling

Given a required interconnection of pins on a board, one can always choose several routings to satisfy the interconnection requirements. If the net involved contains four or more pins, these alternative routings may increase the expected number of midsection crossings above the values shown in Table I because connection of the net may require more than a single crossing of certain board sections. For example, if four pins, one at each corner of the board, are to be connected together, there will either be two crossings of the vertical midsection or two crossings of the horizontal midsection. Accordingly, we have corrected the values of Table I to account for the interrelation of horizontal and vertical midsection crossing.

Suppose that a board is divided into four quadrants by two perpendicular midsection lines. Each midsection line will be placed such that there are an equal number of active circuit pins on each side of it; midsection lines will not necessarily be at the geometric center of the board. There is then a probability of ¼ that any particular pin will be in any particular quadrant of the printed circuit board. Our goal is to estimate the number of essential crossings of the midsection lines for a given net of size n.

There are four cases that must be considered. They are based on the number of quadrants that wholly contain the signal net.

Case 1: This is the case in which the entire net is contained in one quadrant. The probability that Case 1 applies is shown in (1). This case contributes nothing to the essential crossings of the midsection lines.

$$P_1 = 4 \cdot 4^{-n}. \tag{1}$$

Case 2: This is the case in which the entire net is contained in two quadrants. The probability P_2 that Case 2 applies is shown in (2). There are three possibilities for the crossings. If the quadrants are horizontal or vertical, then one midsection crossing is required. If, however, the quadrants are diagonal, then one crossing is required of each midsection line. Therefore, P_{2c} the probability of a net contained in two quadrants generating a crossing of a particular midsection line, is $2/3\ P_2$ (3).

$$P_2 = 6 \cdot (2^n - 2) \cdot 4^{-n} \tag{2}$$

$$P_{2c} = 4 \cdot (2^n - 2) \cdot 4^{-n}. \tag{3}$$

Case 3: This is the case in which the entire net is contained in three quadrants. The probability of Case 3 occuring P_3 is shown in (4). Each net in this case will cross each midsection line at least once. Therefore, the probability of an essential crossing P_{3c} will be equal to P_3 as shown in (5).

$$P_3 = 4 \cdot (3^n - 3 \cdot 2^n + 3) \cdot 4^{-n} \tag{4}$$

$$P_{3c} = 4 \cdot (3^n - 3 \cdot 2^n + 3) \cdot 4^{-n}. \tag{5}$$

Case 4: This is the case in which the net occupies all quadrants. This will require either two crossings of the horizontal midsection line or two of the vertical midsection line. Therefore, we set P_{4c} (7) equal to $1.5 \times P_4$ (6).

TABLE III
EXPECTED NUMBER OF ESSENTIAL MIDSECTION CROSSINGS AS A FUNCTION OF NET SIZE

Net Size	Expected Crossings per Net	Expected Crossings per Pin
n	C	C/n
1	0	0
2	0.500	0.250
3	0.750	0.250
4	0.921	0.230
5	1.06	0.211
6	1.15	0.210
7	1.24	0.177
8	1.30	0.163
10	1.39	0.139
15	1.47	0.098
N	1.5	$1.5/N$

Note: Values corrected for correlation between vertical and horizontal midline crossings.

$$P_4 = (4^n - 4 \cdot 3^n + 6 \cdot 2^n - 4) \cdot 4^{-n} \tag{6}$$

$$P_{4c} = \tfrac{3}{2} \cdot (4^n - 4 \cdot 3^n + 6 \cdot 2^n - 4) \cdot 4^{-n}. \tag{7}$$

C is the expected number of essential crossings of a midsection line per net. C/n is the expected number of essential crossings per pin. It is this number as shown in (9) in which we are interested.

$$C = P_{2c} + P_{3c} + P_{4c} \tag{8}$$

$$C/n = (\tfrac{3}{2} \cdot 4^n - 2 \cdot 3^n + 2^n - 2) \cdot 4^{-n}/n. \tag{9}$$

Values for this equation are shown in Table III.

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Comments on "A Fast Computer Method for Matrix Transposing" and Application to the Solution of Poisson's Equation

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In the above correspondence,[1] an algorithm has been described that allows the transposing of a $2^n \times 2^n$ matrix by reading and writing n times at the most via direct access rows of the matrix and by permuting its data elements. The generalization to arbitrary square matrices has not been described, and the generalization to nonsquare matrices has been reported to be impossible.

The algorithm proposed is very similar to one described and proved completely in [1], which needs only two *sequential* data sets; it has

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