The Duchess Chips for Process-Specific Wire Capacitance Characterization

Ann Coulthard, Jonathan Gainsley,
Jon Lexau, and Ivan E. Sutherland

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Abstract:

This technical report releases a collection of ring oscillator experiments. Our first experimental chip, called *The Duchess*, gave us useful initial results. We followed it with a series of Duchess chips to measure values for other technologies as well as for other load conditions. Here one will find the designs, notes, experimental results, and conclusions from several of these experiments.

Moreover, this technical report reveals not only the experiments themselves, but also what we wrote about them at the time. These are the working documents we used as we developed the experiments. They reveal how our thinking evolved, what we left out of our initial efforts, and how we work. We recognize that some of the documents included here contain flaws; such flaws are a necessary part of an evolution of ideas.

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Introduction

The Duchess Chips for Process−Specific
Wire Capacitance Characterization

Ivan E. Sutherland

This technical report releases a collection of ring oscillator experiments. Our first experimental chip, called *The Duchess*, gave us useful initial results. We followed it with a series of Duchess chips to measure values for other technologies as well as for other load conditions. Here one will find the designs, notes, experimental results, and conclusions from several of these experiments.

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The Ring Oscillator Experiments

The oscillation frequency of a ring of identical inverters depends on the number of inverters in the ring and upon the load borne by each. As the load increases, so does the delay in each inverter, and the frequency of oscillation decreases accordingly. The minimum possible load is a combination of the inverter's own parasitic output capacitance and the input capacitance of the next inverter in the ring.

One can separate an inverter's own parasitic output capacitance from the input capacitance of the next inverter only indirectly. If each inverter drives two identical successors instead of one, it will slow down because of the additional load. If each inverter drives three identical successors instead of one, it will slow down further. In each case, only one of the successors is a part of the continuing ring; the extra ones serve only as dummy loads that increase the total load to a multiple of the load of the next inverter in the ring.

A graph of the delay in each inverter as a function of the number of inverters it drives is very nearly a straight line. The delay intercept of this line reveals how fast the inverter would be were it to drive only its own parasitic output capacitance. The slope of this line reveals the increase in delay for each unit increase of load driven. The intercept depends on the stray capacitance of the inverter structure itself. The slope depends on the fundamental speed of the transistors involved.

Remarkably, the oscillation frequency of a ring of identical inverters is almost independent of the widths of the transistors used. One might think that wider transistors, being more capable drivers, would run faster, but it is not so. Wider transistors are not only more capable drivers but they also present proportionally larger loads.

The oscillation frequency does depend somewhat on the geometric form of the inverters involved because some shapes have less parasitic load than others. The oscillation frequency also depends a little on the details of the interconnect between the inverters because of the stray capacitance of the interconnect wires themselves. Moreover, the amount of load presented by a load inverter depends slightly on how quickly it responds because of the extra load presented by Miller capacitance from its output back to its input. However, these are all second order effects. The primary effect is described well by the nearly straight line relationship between load and delay.

What's nice about ring oscillator experiments is how easily one gathers data from them: *One merely measures the frequency of a bunch of oscillators and then calculates the values one needs.* That's why we chose this form of experiment.

The Significance of Measurements

But why did we want the data? What we needed to know is how fast circuits will run when driving different loads. We didn't need to know the actual capacitance of a particular load in fempto−Farads, but only its capacitance relative to something we can actually control, namely the widths we choose for transistors. We wanted to know how wide to make transistors to drive particular loads at a desired speed.

We have measured various common structures using ring oscillators. Instead of using additional inverters as loads for each inverter in the ring, we use identical copies of a structure of interest. For example, we built rings in which each stage is loaded with 100 microns of wire. By comparing the oscillation frequency of such a ring to that of rings loaded by inverters, we can understand the relationship between wire load and transistor load. Such relative information is of value because it lets us interpret wire load as if it were the load of driving additional transistors of known width. For example, our experiments with a particular 350 nano meter transistor technology reveal that driving interconnect wire is about ten times easier than driving an equivalent width of transistor; 50 microns of wire is as hard to drive as 5 microns of transistor gate width. What a valuable "rule of thumb!"

I hope that readers will profit from observing our research methodology. I firmly believe that an idea is not an idea until it is captured in writing. All too often I see my finest ideas crumble to dust as I try to write them down. Our research group works by capturing increments of knowledge in short written documents. Here you will find a collection of such documents just as they appear in our archive. The blemishes are all there; I hope the gems are, too.

I also hope that others will measure and publish results from other ring oscillator experiments. A ring oscillator experiment makes an excellent first student project in integrated circuit design. It's easy to execute because of its repetitive layout and easy measurement process. Doing it well, however, requires advance thought about the approximate relative load of the various structures included, how the measured signals are to be taken off chip, and how to interpret the data.

By the way, the original Duchess was a dog after whom we named these chips. Designers, like parents, choose names for reasons known only to themselves.

Sun Microsystems Laboratories

Subject: **A Ring Oscillator Speed Test Proposal**
Date: **January 7, 2000**
From: **Ivan Sutherland**
SML#: **2000-0005**

References:

SML# 96-0218:	Four Ring Oscillators Test Chip, Coates et al, 24 May 1996
SML# 98-0365:	Inverter Delay Tests Using Ring Oscillators, Ivan Sutherland, 20 July 1998
SML# 99-0554:	Comparison of 3 and 5-inverter Ring Oscillators, Lexau and Ebergen, 14 Oct 1999
SML# 99-0636:	Wire Models for the HP GMOS10qa Process, Jon Lexau, 13 December, 1999
SML# 2000-0002	The Duchess Chip, Sutherland, Coulthard, Gainsley, 4 January 2000
Sue4	/proj/async/db/2000/duchess_2000_0002/schematics
Electric	/proj/async/db/2000/duchess_2000_0002/electric

PURPOSE

This memo proposes a chip with many ring oscillators intended to check the wiring capacitance models that we use. This chip will tell us the capacitance of various wiring configurations relative to that of a standard inverter. Sue4 diagrams and layout for this chip are located as indicated above. They will ultimately be packaged in a more accessible location. The chip is called "The Duchess".

THE RINGS

Each test consists of a 31 stage ring oscillator with all stages nearly identical. The test circuits have names of the form ring## where ## is a two digit designator. In the layout, each ring is composed of sub-circuits with names of the form inv##, where the ## designator matches the ring in question. The Sue diagrams for the rings loaded with wires use an inverter called invXX and a mass representation of the wire loads. The table on the next page enumerates the tests.

The layout for each ring consists of two rows: a row of 16 stages running from left to right and below it a row of 15 stages running from right to left. The 31 stages in each ring are almost identical except that the stages at the end of the row differ from the others in two ways: First, the metal1 connection between the rows is slightly longer than the connections between stages within a row. Second, a circuit called "driver" couples each ring to the output for measuring its frequency of oscillation. Driver presents an extra half load to the rightmost stage in the top row. The errors introduced by these variations are small, and if necessary we can use the data gathered from these experiments to compensate for them. Driver provides three stages of amplification to drive the long output wire.

THE TESTS

This section describes the tests listed in TABLE 1 below.

Table 1: The proposed tests

test	loading	comments
ring00	next inverter	N=2 microns, P=4 microns.
ring01	2 like inverters	with miller killers
ring02	3 like inverters	with miller killers
ring03	3 like inverters	no miller killers
ring10	next inverter	Twin, total N=4 microns, P=8 microns.
ring11	2 like inverters	with miller killers
ring12	3 like inverters	with miller killers
ring13	3 like inverters	no miller killers
ring20	next inverter	plus 50 m of polysilicon parallel load
ring21	next inverter	plus 100 m isolated metal1 load
ring22	next inverter	plus 100 m isolated metal2 load
ring23	next inverter	plus 100 m isolated metal3 load
ring24	next inverter	plus 100 m isolated metal4 load
ring30	next inverter	plus 50 m of polysilicon series load
ring31	next inverter	plus 100 m fingered metal1 load
ring32	next inverter	plus 100 m fingered metal2 load
ring33	next inverter	plus 100 m fingered metal3 load
ring34	next inverter	plus 100 m fingered metal4 load
ring41	next inverter	plus 100 m fingered metal1 w/ metal2 cross
ring42	next inverter	plus 100 m fingered metal2 w/ metal1 cross
ring43	next inverter	plus 100 m fingered metal2 w/ metal3 cross
ring44	next inverter	plus 100 m fingered metal3 w/ metal2 cross
ring45	next inverter	plus 100 m fingered metal4 w/ metal3 cross

The first few tests calibrate the transistor technology. Ring00, ring01, and ring02 are rings of ordinary inverters with exactly two transistors each: N=2 microns, P=4 microns. Each inverter in these rings drives 1, 2, or 3 similar inverters. Each of the extra loads drives its own "miller killer" load with a step up of 3. The miller killers share drains. Like ring02, ring03 drives 3 loads but

omits the "miller killers." Simulation suggests that ring03 will run slightly slower than ring02. The difference in speed is an indication of the strength of the miller effect.

Ring10, ring11, ring12, and ring13 are similar to the earlier rings except that they use twin inverters back to back, a total of four transistors, for a combined width of N=4 microns, P=8 microns. The back to back inverter form shares a single drain connection for each pair of transistors, thus reducing the self-capacitance in the drain. These rings should illustrate what advantage can be gained with the back to back inverter form.

All of the other rings use the simple inverters identical to those in ring00. Each carries a load composed of a different wiring pattern.

Ring20 and ring30 are each loaded with a loop of 50 microns of polysilicon wire. In ring 30 this wire is the only connection from the output of one inverter to the input of the next inverter. Thus the delay per stage in ring30 reflects both the capacitance and the resistance of the loop of polysilicon wire. In ring20 a short metal1 wire connects the two ends of the polysilicon loop so that only its capacitance loads the ring. These experiments should reveal the limitations of polysilicon wire for interconnect.

Ring21, ring22, ring23 and ring24 each bear a load of 100 microns of wire from the four levels of metal. The wires for these experiments are actually two wires, each 50 microns in length in a fork arrangement. The conductors are spaced on 24 lambda = 4.8 micron centers and separated by several microns from any other conductors except the substrate. These rings target the wire-to-substrate capacitance, relating it to the input capacitance of the inverters. Simulation suggests that 100 microns of wire is a suitable load to get oscillations rates similar to those of the earlier rings.

Ring31, ring 32, ring33 and ring 34 are like the earlier rings, but include "fingers" which are ground wires on both sides of the load wires and in the same level of metal. These tests should reveal the additional capacitance introduced by adjacent conductors. The adjacent wires will be spaced on the 8 lambda centers we ordinarily use for wiring rather than the minimum 6 lambda centers that the design rules permit.

Ring41, ring42, ring43, ring 44 and ring45 are much like the 30's rings. The include not only the adjacent ground wires used in the earlier rings, but also a set of perpendicular ground wires on 8 lambda centers in the layer above or below the test layer as indicated in the table. These tests should reveal the amount of additional stray capacitance introduced where wires on one level cross wires on another level.

USING THE RESULTS

I offer here some preliminary thinking about how to use the data we will gather from The Duchess. Detailed analysis of these data will be subject of a later memo.

There are 23 rings listed in Table 1. Thus the result of running one Duchess chip is 23 frequency numbers. We may choose to average the numbers from a number of Duchess chips. For each of these frequency numbers we will compute the average delay per stage which is just 1/(2*31*F).

A graph of the stage delays versus loading from ring00, ring01, and ring02 should give a familiar straight line. Its slope is the characteristic Tau for the process that we expect to be about 50 psec per load. Its intercept is the overhead cost of the inverter, a value that should also be about 50 psec. The delay from ring03 will confirm the value of including a "miller killer" in the other experiments.

A graph of the stage delays versus loading from ring10, ring11, and ring12 should also give a familiar straight line. Its slope should be very much like that from the other rings, but its intercept should be faster, indicating the reduced overhead delay obtained by sharing drains. I have no idea how great this improvement will be.

On the delay versus load graph from ring00, ring01 and ring02 will also plot the delay per stage for each of the wiring tests. We will use the measured delay per stage as the independent variable on the delay axis. From the load axis of the graph we can read the corresponding effective load, in units of similar inverter widths. This amount of inverter load, at 6 microns of transistor width per unit load, corresponds to the wiring load of that particular wire load test. Because we know the length of the wire loading each stage of the ring oscillator, we can compute the ratio of wiring capacitance per unit length of wire to gate capacitance per unit width of transistor.

Ring20 and ring30 use polysilicon wire loads between their inverter stages. In each case there is a loop of polysilicon 50 microns long between the stages, but in ring 20 its ends are also connected by a short metal1 wire. In ring 30, on the other hand, current to drive the input of the next stage must flow through the polysilicon wire.

Although I feel justified in ignoring the resistance of the metal wires used in this chip, we probably can't neglect the resistance of even fairly short polysilicon wires. Data from ring20 will give us an approximate value for the capacitance of polysilicon. The value is only approximate because the far end of the load wire may not experience the same voltage fluctuation as the near end.

Data from ring30 is of special interest. I believe that modern processes make an effort to reduce the resistance of polysilicon so that one can safely use polysilicon wires several tens of microns long. If ring30 runs nearly as fast as ring20, I will be willing to use fairly long polysilicon connections. If ring30 runs much more slowly than ring20, I will take steps to avoid long polysilicon runs. The analysis of data from ring20 will be much more complicated if ring30 indicates that polysilicon resistance is large.

LAYOUT CONSIDERATIONS

Preliminary layouts show that the inverter experiments are each about 200 microns wide and about 80 microns high. The wiring experiments will be taller, about 300 microns tall. Thus the total area required is less than 23 * 200 * 300 = 1380000 square microns, or about 1.38 square millimeters. With 28 pads the chip turns out to be about 1300 by 1600 microns in size.

To simplify turning experiments on and off they are arranged in three columns of eight experiments each. Separate Vdd connections are provided to many of the experiments, though due to pin limitations some of them are connected in pairs. An eight-input OR gate for each column delivers the frequency from the selected experiment to an output pad.

POSSIBLE PROBLEMS

The biggest problem with this experiment is what to include in the "overhead" load of an inverter. Should one include the short section of wire used to connect the inverter to its neighbors or should one omit that? What about the wire that connects the working inverter to the dummy loads?

The layout for ring00, ring01 and ring02 in the Duchess chip all include a common stub of metal1 wire 17 microns long. In ring02 this wire connects to the inputs of the dummy loads. In ring01 the bottom half of this wire is used to connect to one load, but the top half could have been omitted. In ring00 we could have omitted the entire length of this wire. Thus the over-

head delay in all cases includes the delay to drive this wire, but the incremental cost of adding an inverter load includes only the short connection between this stub and the inverter's input terminal.

Another problem with this experiment involves folding the wire loads. To make the 100 micron wire loads more compact I folded them, using two 50 micron wires in parallel. The loads are in the shape of a tuning fork. The tines of this fork are 4.8 microns on centers. I believe that this is enough separation to avoid significant interaction between the two tines. It may, however, be important to understand the exact geometry in order to interpret the results. A short connection to the wire loads replaces the stub in the earlier rings, but is somewhat shorter. It may turn out to be important to correct the results for this difference in overhead loading.

Sun Microsystems Laboratories

Subject: **The Duchess Simulation Results**
Date: **January 12, 2000**
From: **Ivan Sutherland**
SML#: **2000-0021**

References:

SML# 2000-0002: The Duchess Chip, Sutherland, Coulthard, Gainsley, 4 January 2000
SML# 2000-0005: A Ring Oscillator Speed Test Proposal, Ivan Sutherland, 7 January 2000
SML# 2000-0020: The Duchess Layout, Sutherland, Gainsley and Coulthard, 13 January 2000
/proj/venturi/cad/mosis/hp_gmos10/hp_models/hp_models.sp

PURPOSE

This memo records the simulated speeds of many rings in the Duchess. It omits simulations of rings whose speed depends on wire-to-wire capacitance because we have no spice models for them. Although it offers simulations for the rings with polysilicon wire, they are flawed, again because our spice wire models are inadequate.

DATA SHEET: The last page of this memo offers a form for collecting data from Duchess chips.

SIMULATION DATA

Table 1 on the next page summarizes the simulated delays as measured from a spice simulation using the parameters referenced above. I measured the ring delay from rise to rise in each case. In some cases I also measure the rise to rise and fall to fall delay of a pair of stages within the ring. The final column shows the ring delay divided by 62, which is the average rise or fall delay for the inverters in that ring.

When I first did these simulations, the bottom two rows gave the same data. An improved polysilicon wire model provided by Jon Lexau fixed that problem to give the values reported here. The "as built" sue4 files give the older polysilicon wire model, but that makes no difference to what was actually built. The new model is available in:
/home/ivans/2000/chips/duchess-2000-0002/sim/wire0

The new models show a difference of 240 psec between the periods of ring20 and ring30. Moreover, because these values are between those of ring00 and ring02, calibration of the measured polysilicon capacitance will be relatively easy. If the model of polysilicon wire used here is approximately correct, the duchess will provide good values for us to use.

TABLE 1: Simulated Delay			
Ring	Spice data: ring delay rise-to-rise, nsec	Spice data: two stage delay: rise, fall, psec	Stage delay = ring delay / 62, psec
ring00	3.43	108.06, 111.52	55.323
ring01	4.98	159.43, 160.72	80.323
ring02	6.61	211.10, 214.99	106.613
ring03	7.08	228.87, 227.8	114.194
ring10	3.41		55.000
ring11	4.97		80.161
ring12	6.60		106.452
ring13	7.06		113.871
ring21	6.26	201.01, 201.73	100.968
ring22	6.12	197.34, 197.23	98.710
ring23	5.98	191.57, 192.45	96.452
ring24	5.84	187.74, 187.10	94.194
ring20	4.66		75.16
ring30	4.92		79.35

Measured Delay Information			
Date _____	Chip # _____	Voltage _____	Who _____
Ring	Oscillating frequency, GHz	Ring delay = 1/frequency, nsec	Stage delay = ring delay / 62, psec
ring00			
ring01			
ring02			
ring03			
ring10			
ring11			
ring12			
ring13			
ring20			
ring21			
ring22			
ring23			
ring24			
ring30			
ring31			
ring32			
ring33			
ring34			
ring41			
ring42			
ring43			
ring44			
ring45			

Sun Microsystems Laboratories

Subject: **The Duchess Layout**
Date: **January 14, 2000**
From: **Ivan Sutherland, Jon Gainsley and Ann Coulthard**
SML#: **2000-0020**

References:

SML# 2000-0002:The Duchess Chip, Sutherland, Coulthard, Gainsley, 4 January 2000

PURPOSE

This document describes the layout of the Duchess chip. Table 1 and Figure 1 show the wiring patterns used as loads on the ring oscillators. Two diagrams from Electric identify the load wire facets and inverter facets we used in the layout. N.B. In Electric, a "facet" is a shape definition.

Table 1: Conductor Layers in Various Rings

ring	figure	vertical	horizontal
ring20	G	polysilicon shunt in layout series in Sue	not applicable
ring21	A	metal1	none
ring22	A	metal2	none
ring23	A	metal3	none
ring24	D	metal4	none
ring30	G	polysilicon series in layout shunt in Sue	not applicable
ring31	B	metal1	none
ring32	B	metal2	none
ring33	B	metal3	none
ring34	E	metal4	none
ring41	C	metal1	metal2
ring42	C	metal2	metal1
ring43	C	metal2	metal3
ring44	C	metal3	metal2
ring45	F	metal4	metal3

OVERVIEW

The Duchess chip contains 23 ring oscillators all very similar in structure. Each has a two digit designator, e.g. 41. In the layout we usually used three "facets" associated with each such designator: a ring facet, e.g. ring41, an "inverter" facet, e.g. inv41, and a "wire" facet, e.g. wire41. An index facet called "invIndex" displays an instance of each inverter we used, and an index facet called "wireIndex" displays an instance of each load wire facet we used. These index facets play no role in the layout of the chip actually built; they are merely a convenience for accessing the different facets and for documentation. They appear in outline form at the end of this memo. In the final "as built" Electric files for the Duchess chip, these index facets may be incomplete.

The main part of the layout is a facet called "ringGuts" that contains an instance of each of the 23 rings. It also contains the power and ground wiring for them as well as the OR gates that deliver their output.

Jon Gainsley assembled the final chip from a pad ring defined in Cadence and a version of ringGuts translated from Electric into Cadence. He used Cadence to add wires connecting ringGuts to the pad ring. He also added a ground ring that surrounds ringGuts.

METAL WIRE LOADS

Figure 1 shows six forms of wire load. The medium weight lines in figures A, B, and C represent load wires 3 lambda wide on 8 lambda centers, a typical spacing that we use for metal1, metal2 and metal3. Black and gray lines represent different metal levels. Minimum spacing for metal wires in these levels would be 6 lambda centers, but we rarely put them that close together. The widest lines in figures D, E, and F represent metal4 load wires 6 lambda wide on 12 lambda centers.

The very narrow lines in Figure 1 show connections to the load wires and adjacent ground wires. These connections use metal levels that don't interfere with the load wires. Review the Electric files to see which level is used in each case.

Notice that each load wire is a fork, like that of figure A or D, possibly adjacent to other structures that are grounded. Table 1 on the previous page tells what levels of metal appear in each of the wire loads.

The two "tines" of this fork each contain 50 microns of wire, for 100 microns total. We measure wire lengths along the centerline of the wire up to the center of the last 3 lambda by 3 lambda square at the end of the wire. Measured in this way, each of the vertical bars in the fork is 238 lambda long. The horizontal bar connecting the two verticals is 24 lambda long. The total length is thus 238 + 238 + 24 = 500 lambda or 100 microns.

Figures C and F show a pattern of gray horizontal lines. These are grounded wires on an adjacent level of metal. The table on the first page says which levels are involved. There are exactly 25 such horizontal wires, each 3 lambda wide on 8 lambda centers, making a total of 50 crossings. There is enough space between the vertical connections at the ends of the horizontal wires to "hide" them from the active fork.

POLYSILICON WIRE LOADS

Ring20 and ring30 place 50 microns of polysilicon wire between stages, see Figure 1G. The wire involved forms the shape of a "hat" with two long verticals connected by short horizontal segments at beginning, middle, and end. The vertical segments are 116 lambda long spaced 15 lambda on centers. The three horizontal parts add up to 20 microns long between the inner edges of the contact pads at each end of the wire. The total length, measured along the center line is thus 20 + 116 + 116 = 252 lambda or slightly over 50 microns.

In ring20 on the actual chip a metal1 wire connects the two ends of this polysilicon loop. Ring30 omits this connection. The sue4 diagrams reverse these two conditions. THIS IS A KNOWN DIFFERENCE BETWEEN THE SCHEMATICS AND THE LAYOUT. Sadly, it is invisible to our checking tools, but fortunately it leaves the usefulness of the Duchess intact. We expect that in the real chip ring20 will run slightly faster than ring30, whereas in simulations the reverse is true.

LAYOUT METHOD AND TOOLS

Ivan laid out the most complex rings using Electric. Ann then assembled subsequent rings by modifying the complex ones. We used the "mimic stitching" and "change" functions in Electric to good effect. Mimic stitching puts in many connections where similar connections are appropriate. Change replaces an instance of a facet with an instance of a similar facet. Without these features the layout would have taken much longer.

Jon Gainsley did the final design rule check (DRC) and layout versus schematic (LVS) checks using Cadence tools. This was necessary because Electric is deficient in DRC and LVS. We modified the Electric layout to fix the bugs Jon found, mainly notch rule violations. Jon also did the pad ring design in Cadence because we used existing pad drivers.

We found that Electric worked well enough for our needs. Steve Rubin was very helpful in teaching us about Electric's features, fixing software bugs that we found, and improving Electric to meet our specific requests.

Electric served us better at the small circuit level than for high level layout. When the amount of material presented exceeds the screen capacity, it becomes necessary to jump back and forth between overall and expanded views. In Electric, this took us longer than we liked, perhaps because we're not yet highly skilled users.

Sun Microsystems Laboratories

Title: **Pinout for the Duchess Chip**
Date: **10 Jan 2000**
Author: **Jonathan Gainsley**
SML #: **2000-0012**

References:

[1] SML# 2000-0002: "The Duchess Chip," *Sutherland, Coulthard, Gainsley,* 4 Jan 2000
[2] SML# 2000-0005: "A Ring Oscillator Speed Test Proposal," *Ivan Sutherland,* 5 Jan 2000

Introduction

This memo describes the package pin assignments for the Duchess Chip [1]. The Duchess Chip consists of many ring oscillators with different stage loading which will be used to validate wiring capacitance and resistance models for various wiring configurations. Reference [2] discusses what's on the chip, the proposed tests for the chip, and what information we expect to extract from those tests.

Pin Assignment

The Duchess Chip fits into a 28 pin DIP package. There are 2 dirty vdds, 2 dirty grounds, 1 clean vdd, 3 clean grounds, 17 local vdds, and 3 signal output pins, for a total of 28 pins.

There are 23 ring oscillators on the Duchess Chip. Each of the 17 local Vdds power either one or two rings: 6 power two rings, 11 power single rings. Only one local Vdd will be set high at one time, the others will be low, disabling their respective rings. This means in the worst case at most two rings will be running at the same time. Ideally only one ring would be running during testing to prevent interference from the oscillations of another ring. Figure 1 shows a block diagram of the core with the local Vdd connections to the rings.

The three 8-input OR gates shown in Figure 1 OR the outputs of the ring oscillators. This was done to reduce the total output pin count from 23 to 3. Each OR input has a weak 1u/1u NMOS pull down, which holds the input wire at low when its corresponding ring oscillator is not powered. Note that the labeled pins in Figure 1 correspond to the pins of the chip.

Table 1 lists the local Vdd pins used to power the ring oscillators, and the corresponding output pin for each ring oscillator. Table 2 lists the output pins used to measure the frequency of a ring oscillator. Finally, Table 3 lists the clean and dirty power supply pin assignments.

Figure 2 shows the bonding diagram for the Duchess Chip.

Table 1: Local Vdd Pin Assignments

pin name	pin number	local vdd for:	ring output goes to:	pad type
vddA	17	ring00	outA	RAW
vddB	16	ring01		RAW
vddC	15	ring02		RAW
vddD	14	ring03		RAW
vddE	13	ring21		RAW
vddF	12	ring22		RAW
vddG	11	ring23		RAW
vddH	10	ring24		RAW
vddJ	9	ring44	outB	RAW
vddK	7	ring34	outC	RAW
vddL	6	ring43 ring33	outB outC	RAW
vddM	5	ring42 ring32	outB outC	RAW
vddN	4	ring41 ring31	outB outC	RAW
vddP	3	ring45 ring13	outB outC	RAW
vddR	2	ring12	outC	RAW
vddS	1	ring30 ring11	outB outC	RAW
vddT	28	ring20 ring10	outB outC	RAW

Table 2: Frequency Output Pin Assignments

pin name	pin function	pin number	pad type
outA	frequency output	21	OUT (Boz Pad)
outB	frequency output	23	OUT (Boz Pad)
outC	frequency output	25	OUT (Boz Pad)

Table 3: Power and Ground Pin Assignments

pin name	pin function	pin number(s)	pin count	pad type
vdd	clean power	19	1	VDD
gnd	clean ground	8,18,27	3	GND
dvdd	dirty power	20,26	2	DVDD
dgnd	dirty ground	22,24	2	DGND

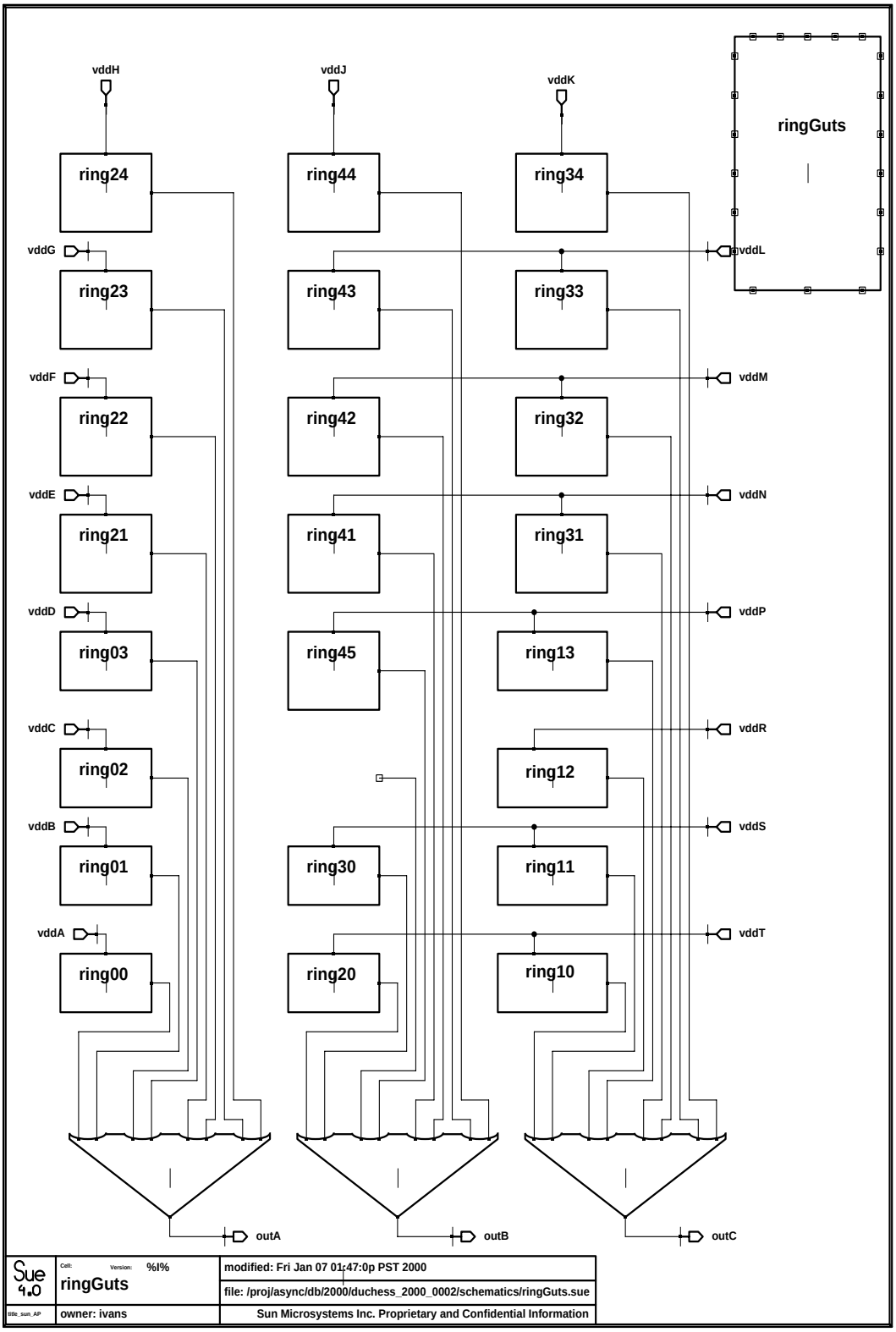


Figure 1: Connections Between Ring Oscillators, Local Vdds, and Output Pads

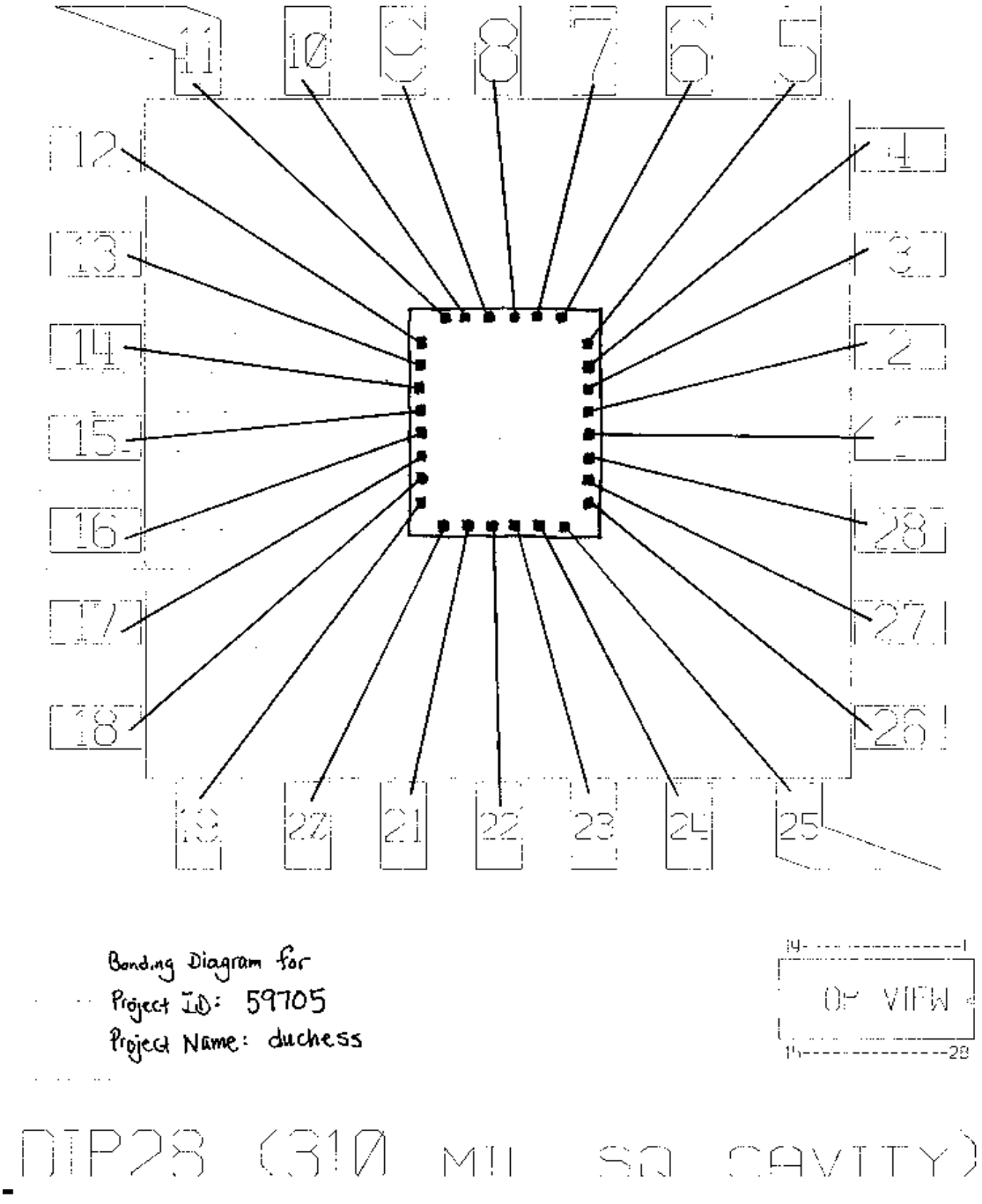


Figure 2: Bonding Diagram for the Duchess Chip

Sun Microsystems Laboratories

Title: **Revised Pinout for the Duchess Chip**
Date: **9 May, 2000**
Author: **Jonathan Gainsley**
SML #: **2000-0223**

References:

[1] SML# 2000-0012: “Pinout for the Duchess Chip,” *Gainsley,* 10 Jan 2000
[2] SML# 2000-0002: “The Duchess Chip,” *Sutherland, Coulthard, Gainsley,* 4 Jan 2000

Introduction

The pinout for the Duchess Chip [2] as documented in [1] is incorrect due to an error by MOSIS when bonding the pads of the chip to the package. Unlike the bonding as drawn in the bonding diagram in [1], which was sent to MOSIS, the bond wires are shifted clockwise one package pin.

Consider OutC, the right most pad on the bottom edge of the die in the bonding diagram in [1]. In that bonding diagram, OutC connects to package pin 25. In the actual chip, the bonding wire is shifted clockwise one package pin, and OutC connects to pin 24. The same is true for all of the bonding wires.

Subtracting 1 from the pin number that the die pad is supposed to connect to will yield the correct pin number it is actually bonded to on the chip.

I believe Jo ran into the same problem with the Square FIFO. Jo called MOSIS to inform them of their mistake.

Revised Pinout Tables

Tables 1 through 3 are the revised pin assignments.

Table 1: Local Vdd Pin Assignments

pin name	pin number	local vdd for:	ring output goes to:	pad type
vddA	16	ring00	outA	RAW
vddB	15	ring01		RAW
vddC	14	ring02		RAW
vddD	13	ring03		RAW
vddE	12	ring21		RAW
vddF	11	ring22		RAW
vddG	10	ring23		RAW
vddH	9	ring24		RAW
vddJ	8	ring44	outB	RAW
vddK	6	ring34	outC	RAW
vddL	5	ring43 ring33	outB outC	RAW
vddM	4	ring42 ring32	outB outC	RAW
vddN	3	ring41 ring31	outB outC	RAW
vddP	2	ring45 ring13	outB outC	RAW
vddR	1	ring12	outC	RAW
vddS	28	ring30 ring11	outB outC	RAW
vddT	27	ring20 ring10	outB outC	RAW

Table 2: Frequency Output Pin Assignments

pin name	pin function	pin number	pad type
outA	frequency output	20	OUT (Boz Pad)
outB	frequency output	22	OUT (Boz Pad)
outC	frequency output	24	OUT (Boz Pad)

Table 3: Power and Ground Pin Assignments

pin name	pin function	pin number(s)	pin count	pad type
vdd	clean power	18	1	VDD
gnd	clean ground	7,17,26	3	GND
dvdd	dirty power	19,25	2	DVDD
dgnd	dirty ground	21,23	2	DGND

Sun Microsystems Laboratories

Title: **Preliminary Duchess Chip Testing Results**
Date: **17 Apr 2000**
Author: **Jonathan Gainsley**
SML #: **2000-0188**

References:

[1] SML# 2000-0002: "The Duchess Chip," *Ivan Sutherland*, 4 Jan 2000
[2] SML# 2000-0005: "A Ring Oscillator Speed Test Proposal," *Ivan Sutherland*, 7 Jan 2000

Background

The Duchess Chip [1] consists of 23 ring oscillators of 31 stages each, with different amounts of transistor or wire loading on each inverter stage. It's purpose is to determine the loading wire places upon a transistor for the TSMC 0.4u (0.35u) process. It also looks at the effect of Miller killers, folded transistors, and poly loading on gate speed.

Introduction

These are the numbers obtained from testing three of the Duchess Chips [1]. They are presented simply for documentation; Jon Lexau will follow up with an analysis at a later date. Table 6 contains the data from all three chips, including the average and percent differences between measurements for subsequent chips. I felt the percent difference between measurements gave a better idea of the similarity of numbers between different chips. A standard deviation calculation resulted in large deviations because of the small sample set, and did not convey any useful information.

I've included the results for Chip #1 in the first 5 tables. The first 5 tables describe what the different rings are, and general trends can be easily seen by looking at them. For a more in-depth description of the rings, refer to [2]. Note that I stole tables 1 through 5's format from [2].

The contents of Table 6 are saved as a StarOffice spreadsheet:
/proj/async/db/2000/duchess_2000_0002/tester/rings2.dat.sdc

and as a tab-deliminated text file:
/proj/async/db/2000/duchess_2000_0002/tester/rings2.txt

Table 1: Effect of Inverter Loading on Folded Transistor Ring Oscillators

Ring#	Loading	Frequency	Ring Description
ring10	next inverter	280.9 MHz	Twin transistors, total N=4u, P=8u
ring11	2 like inverters	195.3 MHz	with Miller killers
ring12	3 like inverters	148.8 MHz	with Miller killers
ring13	3 like inverters	141.5 MHz	no Miller killers

Table 2: Effect of Isolated Wire Loading on Speed of 31 Stage Ring Oscillators

Ring#	Loading	Frequency	Ring Description
ring00	next inverter	214.9 MHz	N=2u, P=4u
ring21	next inverter	161.3 MHz	plus 100u of isolated metal1 load
ring22	next inverter	179.6 MHz	plus 100u of isolated metal2 load
ring23	next inverter	182.0 MHz	plus 100u of isolated metal3 load
ring24	next inverter	178.1 MHz	plus 100u of isolated metal4 load

Table 3: Effect of Additional Capacitance from Adjacent Ground Wires

Ring#	Loading	Frequency	Ring Description
ring00	next inverter	214.9 MHz	N=2u, P=4u
ring31	next inverter	145.6 MHz	plus 100u of fingered metal1 load
ring32	next inverter	151.1 MHz	plus 100u of fingered metal2 load
ring33	next inverter	151.5 MHz	plus 100u of fingered metal3 load
ring34	next inverter	132.6 MHz	plus 100u of fingered metal4 load

Table 4: Effect of Polysicilcon Loading

Ring#	Loading	Frequency	Ring Description
ring00	next inverter	214.9 MHz	N=2u, P=4u
ring20	next inverter	176.1 MHz	plus 50u of polysilicon parallel load
ring30	next inverter	158.7 MHz	plus 50u of polysilicon series load

Table 5: Effect of Capacitance from Different Metal Layers Crossing

Ring#	Loading	Frequency	Ring Description
ring00	next inverter	214.9 MHz	N=2u, P=4u
ring41	next inverter	140.9 MHz	plus 100u of fingered metal1 load w/ metal2 cross
ring42	next inverter	147.9 MHz	plus 100u of fingered metal2 load w/ metal1 cross
ring43	next inverter	146.6 MHz	plus 100u of fingered metal2 load w/ metal3 cross
ring44	next inverter	147.9 MHz	plus 100u of fingered metal3 load w/ metal2 cross
ring45	next inverter	127.2 MHz	plus 100u of fingered metal4 load w/ metal3 cross

Table 6: Duchess Chip Test Results

	Chip#1		Chip#4		Chip#5		%diff #1 to #4	%diff #4 to #5	%diff #5 to #1	Average	
Ring#	period (ns)	freq (MHz)	period (ns)	freq (MHz)	period (ns)	freq (MHz)				period (ns)	freq (MHz)
00	4.65	215.05	4.53	220.75	4.48	223.21	2.58%	1.10%	-3.66%	4.55	219.78
01	6.30	158.73	6.16	162.34	6.07	164.74	2.22%	1.46%	-3.65%	6.18	161.81
02	7.96	125.63	7.82	127.88	7.69	130.04	1.76%	1.66%	-3.39%	7.82	127.88
03	8.14	122.85	7.92	126.26	7.80	128.21	2.70%	1.52%	-4.18%	7.95	125.79
10	3.56	280.90	3.48	287.36	3.42	292.40	2.25%	1.72%	-3.93%	3.49	286.53
11	5.12	195.31	5.01	199.60	4.94	202.43	2.15%	1.40%	-3.52%	5.02	199.20
12	6.72	148.81	6.57	152.21	6.47	154.56	2.23%	1.52%	-3.72%	6.59	151.75
13	7.07	141.44	6.88	145.35	6.77	147.71	2.69%	1.60%	-4.24%	6.91	144.72
20	5.68	176.06	5.61	178.25	5.53	180.83	1.23%	1.43%	-2.64%	5.61	178.25
30	6.30	158.73	6.19	161.55	6.11	163.67	1.75%	1.29%	-3.02%	6.20	161.29
21	6.20	161.29	6.03	165.84	5.96	167.79	2.74%	1.16%	-3.87%	6.06	165.02
22	5.65	176.99	5.51	181.49	5.43	184.16	2.48%	1.45%	-3.89%	5.53	180.83
23	5.49	182.15	5.38	185.87	5.28	189.39	2.00%	1.86%	-3.83%	5.38	185.87
24	5.61	178.25	5.50	181.82	5.43	184.16	1.96%	1.27%	-3.21%	5.51	181.49
31	6.87	145.56	6.75	148.15	6.68	149.70	1.75%	1.04%	-2.77%	6.77	147.71
32	6.62	151.06	6.48	154.32	6.34	157.73	2.11%	2.16%	-4.23%	6.48	154.32
33	6.60	151.52	6.45	155.04	6.31	158.48	2.27%	2.17%	-4.39%	6.45	155.04

	Chip#1		Chip#4		Chip#5		%diff #1 to #4	%diff #4 to #5	%diff #5 to #1	Average	
Ring#	period (ns)	freq (MHz)	period (ns)	freq (MHz)	period (ns)	freq (MHz)				period (ns)	freq (MHz)
34	7.54	132.63	7.43	134.59	7.30	136.99	1.46%	1.75%	-3.18%	7.42	134.77
41	7.10	140.85	6.93	144.30	6.85	145.99	2.39%	1.15%	-3.52%	6.96	143.68
42	6.76	147.93	6.60	151.52	6.48	154.32	2.37%	1.82%	-4.14%	6.61	151.29
43	6.82	146.63	6.65	150.38	6.52	153.37	2.49%	1.95%	-4.40%	6.66	150.15
44	6.76	147.93	6.60	151.52	6.47	154.56	2.37%	1.97%	-4.29%	6.61	151.29
45	7.86	127.23	7.74	129.20	7.64	130.89	1.53%	1.29%	-2.80%	7.75	129.03

Sun Microsystems Laboratories

Subject: **Analysis of the Duchess Chip Measurements**
Date: **June 6, 2000**
From: **Jon Lexau**
Sun Lab#: **2000:0261**

References:

[1] SML #2000-0002 “The Duchess Chip,” Ivan Sutherland, 4 January 2000
[2] SML #2000-0005, “A Ring Oscillator Speed Test Proposal,” Ivan Sutherland, 7 January 2000
[3] SML #2000-0045 “Improved Wire Models for the HP GMOS10qa Process,” Jon Lexau, 27 January 2000
[4] SML #2000-0188 “Preliminary Duchess Chip Testing Results,” Jon Gainsley, 17 April 2000

Introduction

The duchess chip [1,2] was fabricated so that we could calibrate our hspice and logical effort wire models to an actual chip, instead of using the tables of data provided by MOSIS and the fab house, as I did in [3]. Jon Gainsley has measured the speeds of all of the rings on the chip and tabulated those results in [4]. In this memo, I analyze Jon’s data to derive improved wire models for the TSMC process which can be used in the design stage of future chips.

This memo only presents the mathematical analysis and raw results for the duchess chip. This analysis should prove useful for future versions of the duchess chip. I am planning another memo which will make specific recommendations for new simulation wire models based on the results presented here.

The table below presents a summary of some of the interesting figures derived herein.

case	cap/L (fF/μm)	% gate
isolated M1	0.109	5.56
isolated M2	0.071	3.61
isolated M3	0.060	3.07
isolated M4	0.070	3.54

case	cap/L (fF/μm)	% gate
fingered M1	0.161	8.17
fingered M2	0.140	7.10
fingered M3	0.138	6.99
fingered M4	0.208	10.55

fingered/crossed M1	0.175	8.87
fingered/crossed M2	0.153	7.76
fingered/crossed M3	0.149	7.58
fingered/crossed M4	0.232	11.77

poly	0.154	7.81

Analysis

Jon Gainsley has measured a large amount of data from the duchess chip. The question is how to convert this into a reasonable set of wire models. Part of the problem is that from past experience, we do not really expect the simulated performance to exactly match the behavior of the chip. So, I cannot rely on using direct simulation in my analysis.

A convenient starting point is to look at the three basic rings with 1, 2, and 3 inverter loads only. Jon Gainsley's measurements from [4] are reproduced in the table below.

ring id	description	load	period (ns)
ring00	next inverter	1	4.55
ring01	2 inverters	2	6.18
ring02	3 inverters	3	7.82

Table 1: Base Rings (no wire)

Although we say these rings have no wire load, there is actually a 36 μm metal1 wire which connects adjacent stages. Normally, I would consider a wire this short to be negligible, but the inverter sizes here are so small (N = 2μm, P = 4μm) that I worry that this wire represents a significant fraction of the total load on each stage. In fact, it turns out to be about a quarter of the total stage load for ring00. However, I believe that I have performed my analysis in a way where this extra wire is factored out of the results.

Let us find the best-fit straight line through the three points in Table 1 so that we can find the delay per inverter load. The result is

$$period = 2.913 + 1.633 load$$

This fit is nearly perfect. For the subsequent analysis, it will be useful to invert this equation, or

$$load = 0.612 period - 1.782$$

This equation allows us to express the wire load of a ring stage as an equivalent inverter load. In Tables 3 - 6, the equation above is used to generate the data in the load column. For simulation purposes, I have made an additional test ring which has a *load* parameter which is used to set the size of an extra inverter load (plus Miller killer inverters) on each stage of the ring. This circuit will be used later to confirm the predictions made by the analysis to follow.

My first thought to find the appropriate wire load capacitances was to simulate this new test ring with the load predicted from the measured period and then, by trial and error, adjust the capacitance parameter in the wire model until the two simulated periods were equal. I did this for many of the rings, but it is very time consuming and it seemed like there should be a better way. I discussed this with Ivan and some of his suggestions led me to the approach described below.

We need to have two sets of simulated data; one with only inverter loads, and one with only metal wire loads. That will allow us to relate *simulated* inverter loads to *simulated* wire loads. We also have the *measured* inverter loads given by the formula above. By equating the *simulated* and *measured* inverter loads, we can express the *simulated* wire load in terms of the *measured* ring period.

The two test circuits I chose to simulate are:

1. A ring like ring21[1] where the capacitance of the metal wire is artificially set to an appropriate range of values. The wire length is set to 100 µm. The extra 36 µm of metal is *not* included in this circuit.
2. The three basic rings (ring00, ring01, ring02) *without* the extra 36 µm of metal1 attached to each inverter output.

Simulations using the generic TSMC hspice parameters give quite different speed measurements than the run-specific parameters from MOSIS. The run-specific parameters give consistently faster times than the generic parameters, in some cases as much as 25%.

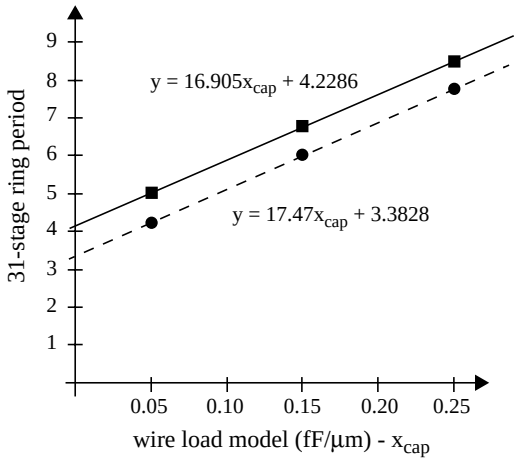
I am hoping that we only need one set of wire models which will work for any run of the TSMC process, so I show the analysis for both sets of hspice parameters. Fortunately, in the end, we find that there is very little difference in the predicted wire model despite the fairly large disparity in the predicted ring periods.

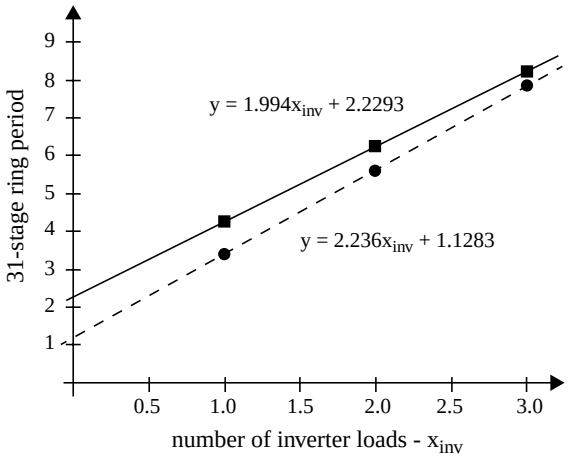
wire load (fF/µm)	period (ns)	
	generic	run specific
0.05	5.075	4.251
0.15	6.762	6.014
0.25	8.456	7.745

inverter load	period (ns)	
	generic	run specific
1 (ring00)	4.232	3.375
2 (ring01)	6.200	5.579
3 (ring02)	8.220	7.847

Table 2: Simulated Wire Load and Base Ring Parameters

Next, I did a linear curve fit on each of these sets of data. Each of these equations is graphed below. The generic data is shown with boxes for simulated data points and a solid line. The MOSIS run-specific data is marked with circles and a dashed line.





1.the function of each of the rings is detailed in [2]

What we really want is an expression for x_{cap}, the simulated wire capacitance load, in terms of x_{inv}, the simulated inverter load. This is easy to obtain by equating the *y*'s in the above equations. Doing this for both sets of data (left column is generic, right is run-specific), we find:

$$16.905x_{cap} + 4.2236 = 1.994x_{inv} + 2.2293$$
$$16.905x_{cap} = 1.994x_{inv} - 1.9943$$
$$x_{cap} = 0.118x_{inv} - 0.118$$

$$17.47x_{cap} + 3.3828 = 2.236x_{inv} + 1.1283$$
$$17.47x_{cap} = 2.236x_{inv} - 2.2545$$
$$x_{cap} = 0.128x_{inv} - 0.129$$

As we can see the two final expressions are quite similar. From this point on, I will use the generic result because this is what we do most of our simulation with. This expression can be rewritten as:

$$x_{cap} = 0.118(x_{inv} - 1)$$

Note that the x_{inv} term is the same as what I called *load* in the equations on page 2. Making the appropriate substitution yields:

$$x_{cap} = 0.118[(0.612\,period - 1.782) - 1]$$

$$x_{cap} = 0.0722\,period - 0.328$$

We have now expressed the wire capacitance to be used for simulation in terms of the period which is measured from the duchess chip, as desired.

Results

The 5 tables below record the results of applying the above equation to each of the measured rings on the duchess chip. The third column is the measured period, taken directly from [4]. The fourth column uses the equation on page two to express the additional wire load in terms of fractional inverter loads. Note that the wire load is really (*load* - 1) because there is one real inverter loading each stage in addition to the wire we are trying to measure. The fifth column is the simulated period using the generic TSMC hspice parameters. I have also simulated some of the rings with the MOSIS run-specific parameters and found that the predicted speeds were slightly faster than the measured periods. The final column gives the wire capacitance per unit length for the specific case using the final formula from the previous section. All wires are of minimum width for that layer. Most of these predictions have been double-checked with additional hspice simulations.

ring id	description	period (ns)	load	sim period	C/L (fF/μm)
ring00	next inverter	4.55	1	4.888	n/a
ring21	100 μm M1	6.06	1.927	6.712	0.109
ring22	100 μm M2	5.53	1.602	6.072	0.071
ring23	100 μm M3	5.38	1.511	5.921	0.060
ring24	100 μm M4	5.51	1.590	6.037	0.070

Table 3: For Isolated Metal Wire Loads

ring id	description	period (ns)	load	sim period	C/L (fF/µm)
ring00	next inverter	4.55	1	4.888	n/a
ring31	100 µm M1	6.77	2.361	7.572	0.161
ring32	100 µm M2	6.48	2.184	7.223	0.140
ring33	100 µm M3	6.45	2.165	7.183	0.138
ring34	100 µm M4	7.42	2.759	8.386	0.208

Table 4: For Fingered Metal Wire Loads

ring id	description	period (ns)	load	sim period	C/L (fF/µm)
ring00	next inverter	4.55	1	4.888	n/a
ring41	100 µm M1 w/M2	6.96	2.478	7.805	0.175
ring42	100 µm M2 w/M1	6.61	2.263	7.397	0.149
ring43	100 µm M2 w/M3	6.66	2.294	7.455	0.153
ring44	100 µm M3 w/M2	6.61	2.263	7.397	0.149
ring45	100 µm M4 w/M3	7.75	2.961	8.811	0.232

Table 5: For Fingered & Crossed Metal Wire Loads

ring id	description	period (ns)	load[a]	sim period	C/L (fF/µm)
ring00	next inverter	4.55	1	4.888	n/a
ring20	50 µm poly	5.61	1.651	6.190	0.154
ring30	50 µm poly w/R	6.2	2.012	6.871	0.154

Table 6: For Polysilicon Wire Loads

a.the formula for *load* assumes a 100µm wire, so for the poly wires, we must double the C/L

For the purposes of generating logical effort wire models, we may wish to know the percent of gate load that a given wire type represents, *frac*. Because each inverter load has 6µm of gate, this can simply be expressed as

$$frac = 0.06(load - 1)$$

The *frac* value for each ring is reported in the summary table on page 1.

Conclusions

My recommendations for new hspice and logical effort wire models will be relegated to a forthcoming memo. I will point out here, however, that it appears that the wire models we have been using are on the conservative side, with the possible exception of some metal4 wires. For dense metal4 wires, we may be underestimating the capacitance.

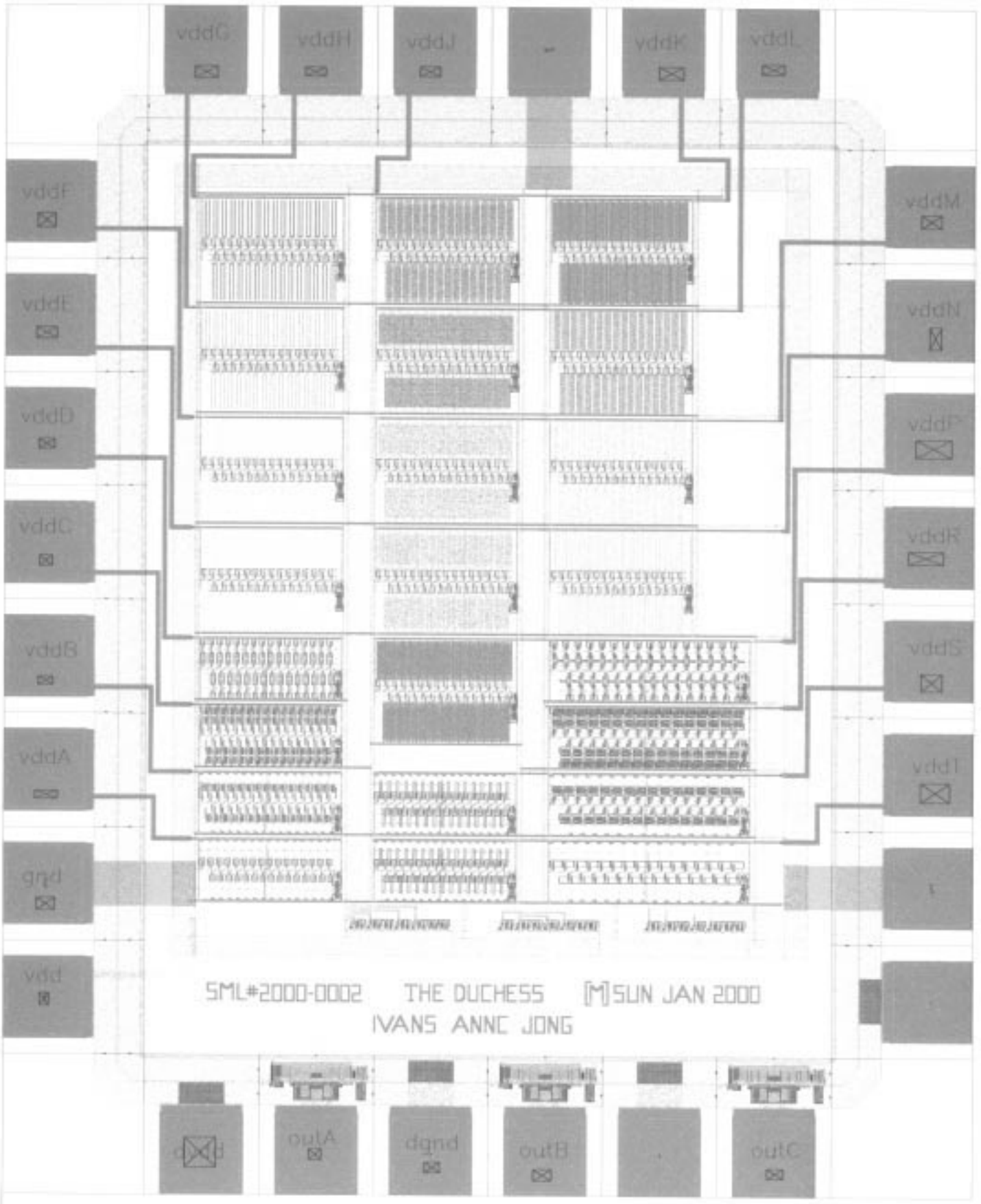
The analysis method presented here may be used on any future run of the duchess chip, simply substituting the new measured results for the data used here. We are already preparing a second run of this chip to help fill in a few gaps in the data which we have gathered.

The Duchess Chip

I. Sutherland, J. Gainsley, & A. Coulthard

SML#2000-0002

6 January 2000



Sun Microsystems Laboratories

Subject: **Rings for the DuchessII Chip**
Date: **June 6, 2000**
From: **Jon Lexau and Jon Gainsley**
Sun Lab#: **2000:0262**

References:

[1] SML #2000-0002, “The Duchess Chip,” Ivan Sutherland, Ann Coulthard, and Jon Gainsley, 4 January 2000
[2] SML #2000-0005, “A Ring Oscillator Speed Test Proposal,” Ivan Sutherland, 7 January 2000
[3] SML #2000-0247, “The DuchessII Chip,” Jon Gainsley, 23 May 2000
[4] SML #2000-0261, “Analysis of the Duchess Chip Measurements,” Jon Lexau, 6 June 2000

Introduction

We are planning to tape out a new version of the duchess chip [3] on the 12 June 2000 MOSIS run of the 0.35 µm TSMC process. The new chip will include all of the rings from the previous version [1,2], except for ring43. We have added seven new rings to either fill in gaps in our previous analysis [4] or to try out new test structures to see their effect on performance.

List of Rings

The table on page 2 lists all of the test rings which will be on the duchessII chip. The seven rings which have been added since the previous version of the chip are shown in **bold**.

Table 1: Rings for the Duchess2 Chip

test	loading	comments
ring00	next inverter	N=2 microns, P=4 microns
ring01	2 like inverters	with miller killers
ring02	3 like inverters	with miller killers
ring03	3 like inverters	no miller killers
ring10	next inverter	folded source, total N=4 microns, P=8 microns
ring11	2 like inverters	with miller killers
ring12	3 like inverters	with miller killers
ring13	3 like inverters	no miller killers
ring14	**next inverter**	**not folded, N=4 microns, P=8 microns**
ring15	**next inverter**	**not folded, N=4μ, P=8μ, limited active contacts**
ring16	**next inverter**	**not folded, N=4μ, P=8μ, extra-wide drain**
ring20	next inverter	plus 50 μ of polysilicon parallel load
ring21	next inverter	plus 100 μ of isolated metal1 load
ring22	next inverter	plus 100 μ of isolated metal2 load
ring23	next inverter	plus 100 μ of isolated metal3 load
ring24	next inverter	plus 100 μ of isolated metal4 load
ring30	next inverter	plus 50 μ of polysilicon series load
ring31	next inverter	plus 100 μ of fingered metal1 load
ring32	next inverter	plus 100 μ of fingered metal2 load
ring33	next inverter	plus 100 μ of fingered metal3 load
ring34	next inverter	plus 100 μ of fingered metal4 load, 2.4 μ c/c spacing
ring35	**next inverter**	**plus 100 μ of fingered metal4 load, 3.2 μ c/c spacing**
ring36	**next inverter**	**plus 100 μ of fingered metal4 load, 6.4 μ c/c spacing**
ring37	**next inverter**	**plus 100 μ of polysilicon series load**
ring41	next inverter	plus 100 μ of fingered metal1 load w/ metal2 cross
ring42	next inverter	plus 100 μ of fingered metal2 load w/ metal1 cross
ring44	next inverter	plus 100 μ of fingered metal3 load w/ metal4 cross
ring45	next inverter	plus 100 μ of fingered metal4 load w/ metal3 cross
ring46	**next inverter**	**plus 50 μm of polysilicon parallel load w/ metal1 cross**

Note that ring43 has been removed from this test chip.

Description of New Rings

Below, I provide a brief description of the rings which have been added for the duchessII chip to indicate what additional information they might provide.

ring14

This is to be used as a more direct comparison to ring10 in order to determine exactly how much improvement is seen by folding a transistor to reduce the source/drain area. On the previous duchess chip, we had to compare ring10 to ring 00, which should be OK, but I was concerned that the extra metal1 load (see [3]) on each stage might affect the results too much.

ring15

In his layout for the t35 chip, Ivan is fond of using only a single substrate contact for a reasonably large diffusion area in order to allow more wires to run over the transistor. We would like to see what impact, if any, this has on the performance of the transistors.

ring16

We are also interested in learning what the effect is of adding extra space, above the 1λ minimum, between the active contacts and the poly gate of a transistor, as this happens occasionally in our layouts. We have chosen to make the spacing 3λ for the inverters in ring16.

ring35, ring36

As indicated by vendor technology information, the line-to-line capacitance for metal4 is very high. I would like to be able to measure how the coupling falls off with line separation, so I have chosen two additional separations to test. Also, ring35 has the spacing set to the usual value that we use on our chips, which is twice the normal separation for metal1, metal2, and metal3 connections.

ring37

This is just one more ring in the polysilicon wire load group. I am hoping that having a second length of series connection would allow us to confirm the resistance part of our model for poly wires.

ring46

In the first duchess chip, we had only isolated polysilicon wires. This ring will correct this oversight.

Sun Microsystems Laboratories

Title: **Pinout for the DuchessII Chip**
Date: **7 June 2000**
Author: **Jonathan Gainsley**
SML #: **2000-0271**

References:

[1] SML# 2000-0247: “The DuchessII Chip (CHIP),” Gainsley, 7 June 2000
[2] SML# 2000-0262: “Rings for the DuchessII Chip,” Lexau, Gainsley, 6 June 2000

Introduction

This memo documents the pinout for the DuchessII Chip [1]. Further information about the chip can be found in [2].

The Chip Pins

The DuchessII has 29 rings which run off local vdd pins. In some cases, two rings share the same local vdd pin, as shown in Figure 1. There are 20 such local vdd pins. To measure the frequency at which the rings oscillate, a tap from each ring goes to one of four 8-way ORs. As long as only one local vdd is powered, only one signal will go to any 8-way OR. There are four output pins, one from each of the four 8-way ORs.

I used four extra pad locations for testing the pads. The input pad *ptin* connects through a passgate to an output pad *ptout*, and a bidirectional pad *ptio*. This allows *ptin* to drive both *ptout* and *ptio*, and allows *ptio* to drive *ptout* if the *ptin* is cut off by the passgate. Another input pad, *ptrd*, controls the direction of the bidirectional pad. This takes up 4 pins. Note that the passgate is opaque when *ptrd* is set such that *ptio* is in input mode.

There are also 4 clean ground pins, 2 clean vdd pins, 3 dirty ground pins, and 3 dirty vdd pins. This is a total of 12 pins for power.

20 vdd pins plus 4 output pins plus 12 power pins plus 4 pad test pins equals 40 pins. DuchessII fits nicely in a DIP40 package.

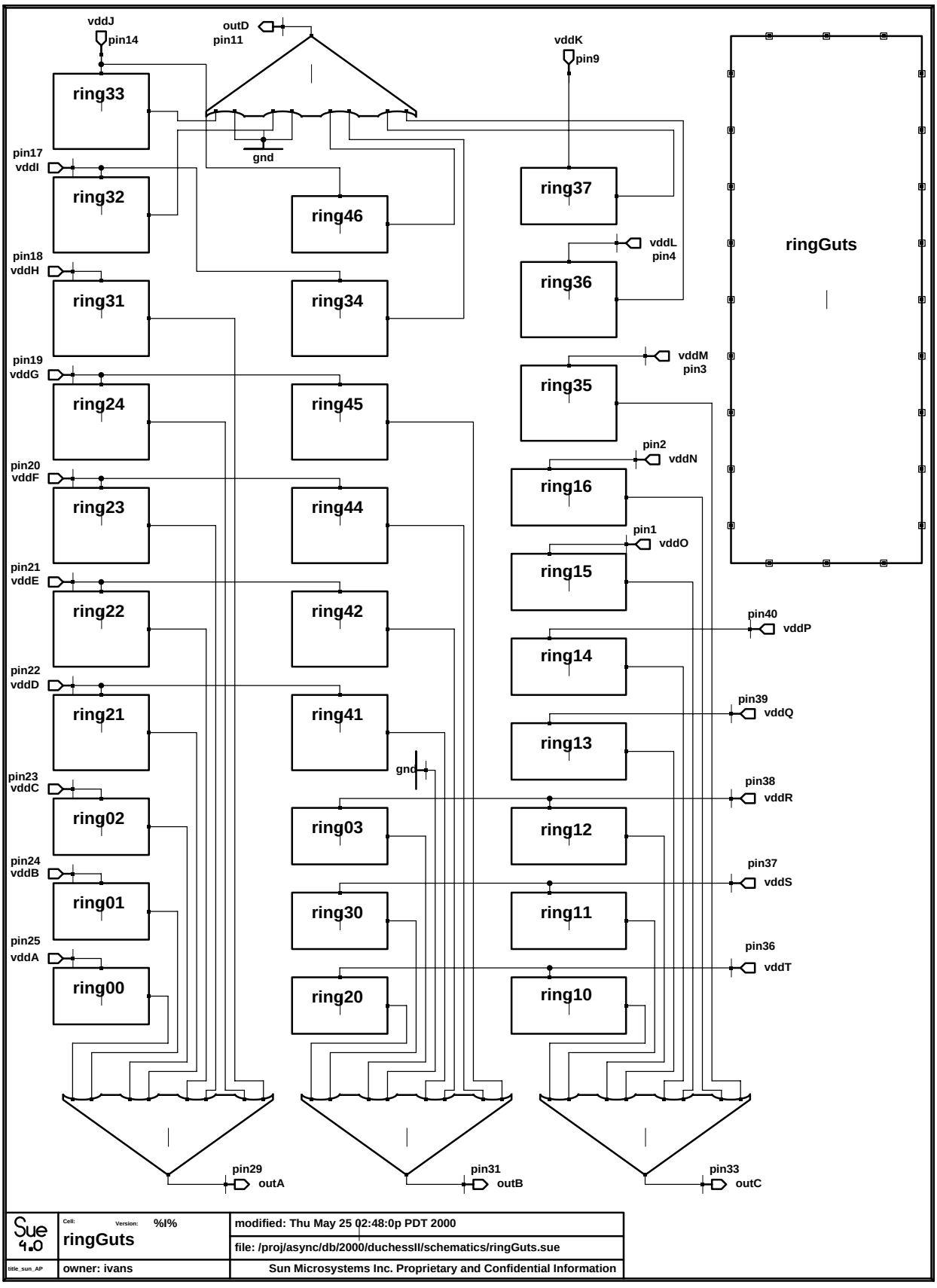
Pin Assignments

Rather than using a table, I find it easier to reference Figure 1 for the local vdd and frequency out pins.

Table 1 lists pin numbers for the power pins and the pad test pins.

Table 1: Power and Pad Test Pin Assignments

pin name	pin function	pin number(s)	pin count	pad type
vdd	clean power	13, 27	2	RAW
gnd	clean ground	5, 15, 26, 35	4	GND
dvdd	dirty power	12, 30, 34	3	DVDD
dgnd	dirty ground	10, 28, 32	3	DGND
ptin	input pad	6	1	INBUF
ptout	output pad	7	1	OUT
ptio	io pad	8	1	IO
ptrd	controls direction of ptio	16	1	INBUF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pin14
outD
pin11
vddK
pin9
ringGuts
ring33
gnd
pin17
vddI
ring32
ring46
ring37
vddL
pin4
pin18
vddH
ring31
ring34
ring36
vddM
pin3
pin19
vddG
ring24
ring45
ring35
pin2
vddN
pin20
vddF
ring23
ring44
ring16
pin1
vddO
pin21
vddE
ring22
ring42
ring15
pin40
vddP
pin22
vddD
ring21
ring41
ring14
pin39
vddQ
gnd
pin23
vddC
ring02
ring03
ring13
pin38
vddR
pin24
vddB
ring01
ring30
ring12
pin37
vddS
pin25
vddA
ring00
ring20
ring11
pin36
vddT
ring10
pin29
outA
pin31
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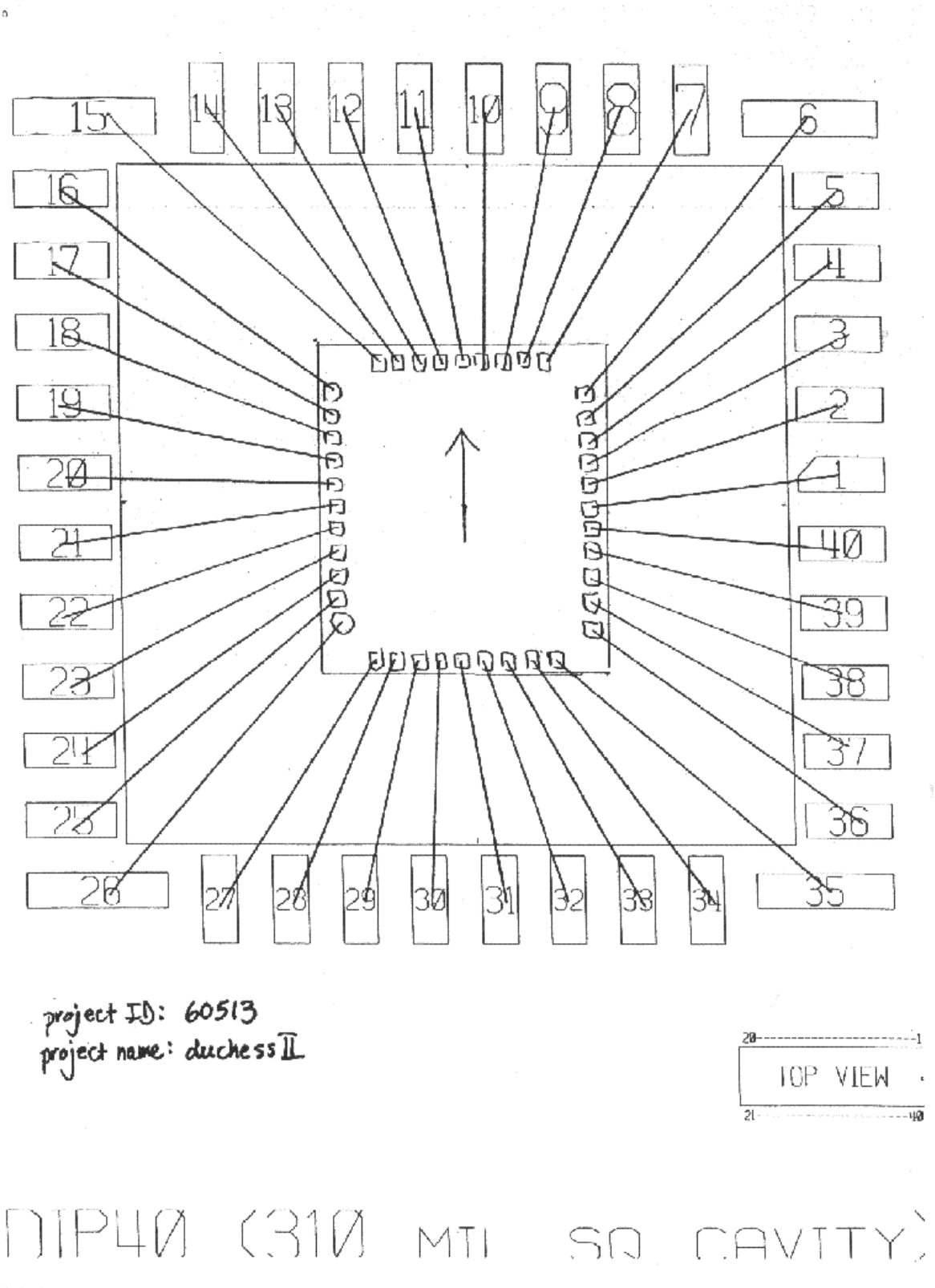
Sun Microsystems Inc. Proprietary and Confidential Information



Bonding diagram for the DuchessII Chip

Sun Microsystems Laboratories

Title: **DuchessII Ring Speeds - Just the Numbers**
Date: **18 Aug 2000**
Author: **Jonathan Gainsley**
SML #: **2000-0447**

References:

[1] SML# 2000-0262: “Rings for the DuchessII Chip,” *Lexau*, *Gainsley*, 6 Jun 2000
[2] SML# 2000-0448: “DuchessII Tied Output Bug and Workaround,” *Gainsley*, 18 Aug 2000

Introduction

This memo records the speeds of the rings on the DuchessII Chip. For a full description of the rings, see reference [1].

Methods

For most rings I used an oscilloscope to measure the periods of ring oscillations, which I then converted to frequencies. However, for rings 32, 33, 34, and 46 I used a spectrum analyzer, due to a bug in the chip. See [2] for details.

Organization

Table 1 lists the average frequency for each ring calculated from the three DuchessII chips I tested. Table 2 lists the frequencies of the rings for the three chips tested, and the standard deviation. As in [1], new rings are shown in **bold**.

Table 1: Average Ring Speeds in DuchessII

test	loading	comments	freq (MHz)
ring00	next inverter	N=2 microns, P=4 microns	210.4
ring01	2 like inverters	with miller killers	155.1
ring02	3 like inverters	with miller killers	122.5
ring03	3 like inverters	no miller killers	118.9
ring10	next inverter	folded source, total N=4 microns, P=8 microns	277.0
ring11	2 like inverters	with miller killers	192.7
ring12	3 like inverters	with miller killers	147.2
ring13	3 like inverters	no miller killers	140.4
ring14	**next inverter**	**not folded, N=4 microns, P=8 microns**	**246.3**
ring15	**next inverter**	**not folded, N=4μ, P=8μ, limited active contacts**	**274.3**
ring16	**next inverter**	**not folded, N=4μ, P=8μ, extra-wide drain**	**227.3**
ring20	next inverter	plus 50 μ of polysilicon parallel load	173.9
ring21	next inverter	plus 100 μ of isolated metal1 load	157.1
ring22	next inverter	plus 100 μ of isolated metal2 load	172.6
ring23	next inverter	plus 100 μ of isolated metal3 load	178.8
ring24	next inverter	plus 100 μ of isolated metal4 load	173.7
ring30	next inverter	plus 50 μ of polysilicon series load	156.4
ring31	next inverter	plus 100 μ of fingered metal1 load	140.9
ring32	next inverter	plus 100 μ of fingered metal2 load	150.8
ring33	next inverter	plus 100 μ of fingered metal3 load	153.8
ring34	next inverter	plus 100 μ of fingered metal4 load, 2.4 μ c/c spacing	127.4
ring35	**next inverter**	**plus 100 μ of fingered metal4 load, 3.2 μ c/c spacing**	144.0
ring36	**next inverter**	**plus 100 μ of fingered metal4 load, 6.4 μ c/c spacing**	167.5
ring37	**next inverter**	**plus 100 μ of polysilicon series load**	120.1
ring41	next inverter	plus 100 μ of fingered metal1 load w/ metal2 cross	135.8
ring42	next inverter	plus 100 μ of fingered metal2 load w/ metal1 cross	143.7
ring44	next inverter	plus 100 μ of fingered metal3 load w/ metal4 cross	146.4
ring45	next inverter	plus 100 μ of fingered metal4 load w/ metal3 cross	122.7
ring46	**next inverter**	**plus 50 μm of polysilicon parallel load w/ metal1 cross**	**167.8**

Table 2: Sampled Chip Speeds

test	Chip#1 Freq. (MHz)	Chip#2 Freq. (MHz)	Chip#3 Freq. (MHz)	One Stdev (MHz)
ring00	207.38	213.68	210.26	3.15
ring01	153.44	157.65	154.25	2.23
ring02	121.07	124.69	121.65	1.94
ring03	117.92	120.19	118.48	1.18
ring10	273.97	281.06	275.86	3.67
ring11	190.15	196.54	191.39	3.39
ring12	145.62	149.99	145.99	2.42
ring13	138.89	143.53	138.89	2.68
ring14	**243.31**	**251.13**	**244.5**	**4.21**
ring15	**270.86**	**280.35**	**271.74**	**5.24**
ring16	**224.72**	**231.48**	**225.58**	**3.68**
ring20	172.03	176.34	173.28	2.22
ring21	155.84	158.73	156.67	1.49
ring22	170.74	175.01	172	2.19
ring23	176.77	181.82	177.65	2.7
ring24	171.56	176.77	172.83	2.72
ring30	155.45	158.15	155.45	1.56
ring31	138.89	143.2	140.51	2.18
ring32	147.5	152.2	150.1	2.35
ring33	151.6	156.3	152.5	2.49
ring34	125.6	129.4	126.4	2
ring35	**142.19**	**146.69**	**143.2**	**2.36**
ring36	**165.1**	**170.74**	**166.67**	**2.91**
ring37	**119.05**	**121.95**	**119.33**	**1.6**
ring41	134.54	137.31	135.45	1.41
ring42	141.84	145.29	143.88	1.73
ring44	144.93	148.52	145.62	1.91
ring45	120.88	125	122.25	2.1
ring46	**165.5**	**170.5**	**166.5**	**2.65**

Sun Microsystems Laboratories

Title: **DuchessII Tied Output Bug and Workaround**
Date: **16 Aug 2000**
Author: **Jonathan Gainsley**
SML #: **2000-0448**

References:

[1] SML# 2000-0262: "Rings for the DuchessII Chip," *Lexau, Gainsley*, 6 Jun 2000
[2] SML# 2000-0271: "Pinout for the DuchessII Chip," *Gainsley*, 7 Jun 2000

Introduction

There is a bug in the DuchessII chip where two ring oscillators are powered by the same local VDD, and their outputs go to the same 8-way OR. Because their outputs go to the same 8-way OR, one cannot observe and measure either frequency alone. The chip output is then the "OR" of the two ring oscillator outputs. This happens for two different pairs of rings.

Tied Outputs

By mistake I routed several ring oscillator outputs to the same 8-way OR that should have been routed to separate 8-way ORs. This is glaringly obvious in Figure 1 of [2]. Rings 32 and 34 are powered by local *VDDI*, and have outputs that get OR'd and come out on *outD*. The same occurs for rings 33 and 46, powered by *VDDJ*, and going to the same 8-way OR.

Problem

If both ring outputs were square waves, it would probably be easy to measure two distinct periods off the resulting OR'd signal on an oscilloscope. Unfortunately, either the signals internal to the chip are not perfect square waves, or the output pads are too slow to faithfully reproduce the resulting output. My guess is probably both. The resulting output signal is a messy but periodic signal from which it is difficult to make accurate measurements for the two unknown periods.

Solution

Part A: Looking at a ring pair output on the oscilloscope

Using an oscilloscope, I measured what appeared to be the period of the higher frequency output imposed on the lower frequency output. I did this for both pairs of rings. At this point, I was not sure that this was a real output frequency, and not just a result of the OR of the two signals. I did this for both pairs of tied together rings.

Part B: Looking at the ring pair output on a spectrum analyzer

I then ran the output to a spectrum analyzer, where I looked for the frequency peaks. Of course there were several peaks due to different harmonics, but two peaks stood out with a greater

magnitude than the rest. Interestingly, they appeared to be of about the same magnitude. The frequency of one of the peaks closely matched the period measurement I took in Part A. This affirmed my belief that the two large peaks represented the two output frequencies of the rings.

Part C: Deducing the ring to frequency matching

I now had two frequency measurements for two rings, and needed to match which frequency came from which ring. I noted that on the Duchess chip, rings 32 and 33 had very similar speeds. Because rings 32 and 33 did not change from Duchess to DuchessII, I conjectured that rings 32 and 33 on DuchessII should be about the same speed. In addition, for all the other rings, speeds on DuchessII are very similar to speeds on the original Duchess chip. So rings 32 and 33 on DuchessII should have about the same speed as rings 32 and 33 on the Duchess chip.

The ring pair of rings 32 and 34 had speeds of 150 MHz and 126 MHz. The ring pair of rings 33 and 46 had speeds of 153 MHz and 167 MHz. Rings 32 and 33 on the original Duchess chip had speeds of about 150 MHz. I concluded then that ring 32 must have a speed of 150 MHz, and ring 33 a speed of 153 MHz.

If this is true, then ring 46 has a speed of 167 MHz. Ring 46 is 50um of parallel polysilicon load with metal1 crossing. Ring 20 is 50um of parallel polysilicon load with no metal crossing, and runs at 174 MHz. So it is expected that ring 46 should be slower than ring 20, which is the case.

Ring 34 then must run at 126 MHz. Ring 34 has a metal 4 load with 2.4um center to center spacing. Rings 35 and 36 also have metal 4 loads, with 3.2um and 6.4um center to center spacing, respectively. They run at 144 MHz and 168 MHz, respectively. It is expected that ring 34 run slower than rings 35 and 36, which is the case.

Conclusion

I cannot be 100% sure that I have found the correct frequencies for each ring in the tied ring pairs. I am, however, 99% sure that I have. Comparisons to the original Duchess chip agree with my conclusion. Comparisons to other rings on DuchessII, and the resulting expected frequencies for the unknown rings, also agree with my conclusion. The final test will be the full-blown numerical analysis by Jon Lexau to follow at a later date.

Sun Microsystems Laboratories

Subject: **Analysis of the DuchessII Chip Measurements**
Date: **August 28, 2000**
From: **Jon Lexau**
Sun Lab#: **2000-0472**

References:

[1] SML #2000-0247 “The DuchessII Chip (Chip),” Jon Gainsley, 7 June 2000
[2] SML #2000-0261 “Analysis of the Duchess Chip Measurements,” Jon Lexau 6 June 2000
[3] SML #2000-0262 “Rings for the DuchessII Chip,” Jon Lexau and Jon Gainsley, 6 June 2000
[4] SML #2000-0316 “Suggested Wire Models for the TSMC 0.35 um Process,” Jon Lexau, 5 July 2000
[5] SML #2000-0447 “DuchessII Ring Speeds - Just the Numbers,” Jon Gainsley, 18 August 2000

Introduction

The duchessII chip [1,3] was fabricated in order to confirm the results from the previous duchess chip, as well as add new data from several additional rings. Jon Gainsley has measured the speeds of all of the rings on the new chip and tabulated those results in [5]. In this memo, I repeat my analysis as in [2], using this new data. The short and sweet conclusion from this analysis is that there is no need to change the wire models that we are currently using [4]. New insight from some of the added rings may allow us to reduce the capacitance for the metal4 wire model.

The table below presents a summary of some of the interesting figures derived herein.

case	cap/L (fF/μm)	% gate
isolated M1	0.112	5.70
isolated M2	0.072	3.67
isolated M3	0.058	2.96
isolated M4	0.072	3.67

case	cap/L (fF/μm)	% gate
fingered M1	0.162	8.27
fingered M2	0.130	6.62
fingered M3	0.121	6.16
fingered M4[a]	0.151	7.70

fingered/crossed M1	0.181	9.21
fingered/crossed M2	0.152	7.78
fingered/crossed M3	0.143	7.32
fingered/crossed M4	0.234	11.95

poly	0.138	7.06
poly crossed M1	0.167	8.54

a.for wires with double the normal separation (3.2 μm)

Analysis

A detailed description of the data analysis method was presented in [2]. I will not repeat the justification for each step here, but instead simply refer to the prior work as needed. I will also borrow some intermediate results from the previous memo which do not depend on process parameters.

We again begin by considering the three basic rings with 1, 2, and 3 inverter loads only. Jon Gainsley's measurements from [5] are reproduced in the table below.

ring id	description	load	period (ns)
ring00	next inverter	1	4.75
ring01	2 inverters	2	6.45
ring02	3 inverters	3	8.17

Table 1: Base Rings (no wire)

Let us find the best-fit straight line through the three points in Table 1 so that we can find the delay per inverter load. The result is

$$period = 1.71 load + 3.037$$

This fit is nearly perfect. For the subsequent analysis, it will be useful to invert this equation, or

$$load = 0.585 period - 1.776$$

This equation allows us to express the wire load of a ring stage as an equivalent inverter load. The equation above is used to generate the data in the *load* column of Tables 2 - 5 below.

In [2], I went to great length to determine the relationship between x_{cap}, the wire capacitance load, in terms of x_{inv}, the inverter load. Here I will simply present the final result; please refer to [2] for all the gory details. This expression can be rewritten as:

$$x_{cap} = 0.118(x_{inv} - 1)$$

Here, the x_{inv} term is the same as what I called *load* in the equations above. Making the appropriate substitution yields:

$$x_{cap} = 0.118[(0.585 period - 1.776) - 1]$$

$$x_{cap} = 0.069 period - 0.328$$

This equation expresses the wire capacitance to be used for simulation in terms of the period which is measured from the duchess chip.

Basic Results

The four tables below record the results of applying the above equation to each of the measured rings on the duchess chip. The third column is the measured period, taken directly from [5]. The fourth column uses the equation on page 2 to express the additional wire load in terms of fractional inverter loads. Note that

the wire load is really (*load* - 1) because there is one real inverter loading each stage in addition to the wire we are trying to measure. The final column gives the wire capacitance per unit length for the specific case using the final formula from the previous section. All wires are of minimum width for that layer.

ring id	description	period (ns)	load	C/L (fF/μm)
ring00	next inverter	4.55	1	n/a
ring21	100 μm M1	6.37	1.950	0.112
ring22	100 μm M2	5.79	1.611	0.072
ring23	100 μm M3	5.59	1.494	0.058
ring24	100 μm M4	5.79	1.611	0.072

Table 2: For Isolated Metal Wire Loads

ring id	description	period (ns)	load	C/L (fF/μm)
ring00	next inverter	4.75	1	n/a
ring31	100 μm M1	7.1	2.378	0.162
ring32	100 μm M2	6.63	2.103	0.130
ring33	100 μm M3	6.50	2.027	0.121
ring34	100 μm M4	7.85	2.815	0.214
ring35	100 μm M4 (3.2 sep)	6.94	2.284	0.151
ring36	100 μm M4 (6.4 sep)	5.97	1.717	0.084

Table 3: For Fingered Metal Wire Loads

ring id	description	period (ns)	load	C/L (fF/μm)
ring00	next inverter	4.75	1	n/a
ring41	100 μm M1 w/M2	7.37	2.536	0.181
ring42	100 μm M2 w/M1	6.96	2.296	0.152
ring44	100 μm M3 w/M2	6.83	2.220	0.143
ring45	100 μm M4 w/M3	8.15	2.992	0.234

Table 4: For Fingered & Crossed Metal Wire Loads

ring id	description	period (ns)	load[a]	C/L (fF/μm)
ring00	next inverter	4.75	1	n/a
ring20	50 μm parallel poly	5.75	1.588	0.138
ring30	50 μm series poly	6.40	”	”
ring37	100 μm series poly	8.33	”	”
ring46	50 μm poly w/M1	5.96	1.712	0.167

Table 5: For Polysilicon Wire Loads

a.the formula for *load* assumes a 100μm wire, so for the poly wires, we must double the C/L for rings 20, 30, and 46

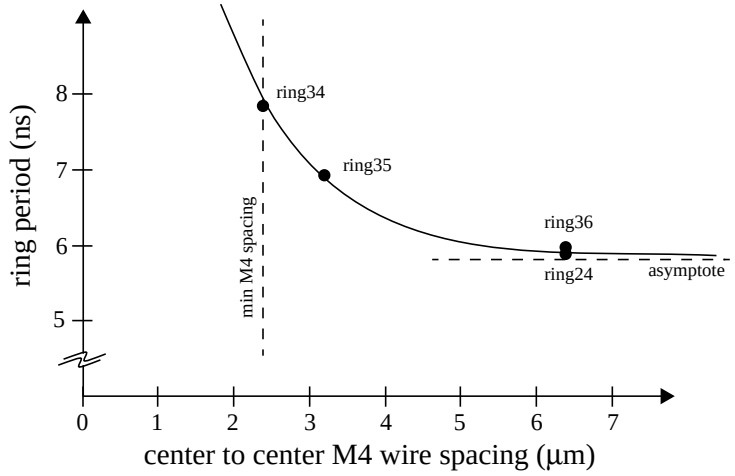
For the purposes of generating logical effort wire models, we may wish to know the percent of gate load that a given wire type represents, *frac*. Because each inverter load has 6μm of gate, this can simply be expressed as

$$frac = 0.06(load - 1)$$

The *frac* value for each ring is reported in the summary table on page 1.

New Metal4 Wire Results

We added rings 34 and 35 to the duchessII test suite in order to generate a curve of speed vs wire separation for metal4. Separation affects the speed of all metal layers, but metal4 is especially bad because this metal layer is significantly thicker than the others. Rings 24 and 36 have the same metal4 pitch - their periods are different because the wire’s surrounding environment is slightly different in each case.



From this graph, we can see that any separation greater than about 6.0μm is essentially the same as infinite separation. More importantly, we can also find that a separation of around 3.5μm gives a ring period of the same order as for M2 or M3 (cf rings 32 and 33). This means that for separations greater than this, we can safely use the M1-M3 capacitance model for M4 wires, instead of the very pessimistic model that we are

using now. For many of our chips, we have used a minimum metal4 separation of 3.2µm, which is exactly double the spacing used for other metal layers, and it appears that this may be a good practice.

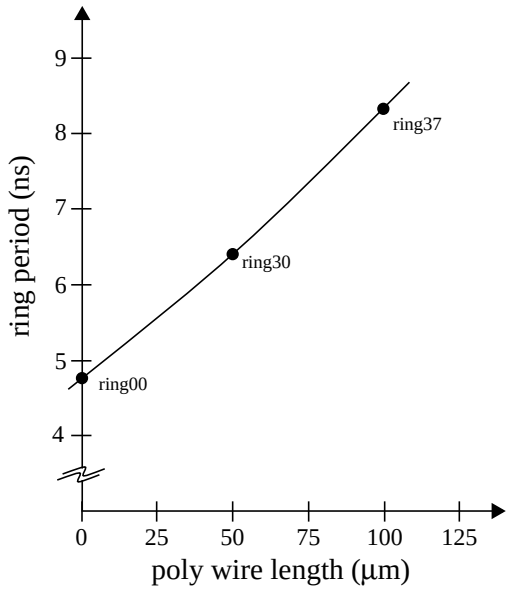
In case it is needed later, the curve that I used to fit the line in the graph above is

$$y = 5.85 + 14.9801e^{-0.8164x}$$

New Polysilicon Wire Results

On the first duchess chip, there was no polysilicon wire ring with crossed metal over it. The duchessII chip corrects this oversight with ring46. Fortunately, we find that the capacitance increase is not too great.

The other poly wire addition to duchessII was ring37, which has twice the poly wire length of ring30. This was added to try to get a handle on ring speed vs wire load when the resistance per unit length is large. The three data points that we have are plotted on the graph below.



Intuition (and hspice simulation) indicates that this curve should not really be linear, as it looks in the graph. The problem is that we are seeing just a small section of the curve. To really see the proper shape, we would need to have a couple more poly rings with, say, 200 and 500 µm wire loads. I don't really think we want to have such long poly wires, so I would not recommend building such rings, except perhaps for purely academic purposes.

Conclusions

The analysis of duchessII shows that our current wire models [4] are still correct. We now have enough data to fine tune the model for metal4 for typical instead of worst-case wire separation, if desired. Also, we can see that the relationship between delay and poly wire length is roughly linear for the range of wires that we are likely to see on any of our test chips.

Sun Microsystems Laboratories

Subject: **Analyzing the Inverter-Only Rings on DuchessII**
Date: **September 8, 2000**
From: **Jon Lexau**
Sun Lab#: **2000-0497**

References:

[1] SML #2000-0002 “The Duchess Chip (Chip),” Ivan Sutherland, 4 January 2000
[2] SML #2000-0247 “The DuchessII Chip (Chip),” Jon Gainsley, 7 June 2000
[3] SML #2000-0262 “Rings for the DuchessII Chip,” Jon Lexau and Jon Gainsley, 6 June 2000
[4] SML #2000-0316 “Suggested Wire Models for the TSMC 0.35 μm Process,” Jon Lexau, 5 July 2000
[5] SML #2000-0447 “DuchessII Ring Speeds - Just the Numbers,” Jon Gainsley, 18 August 2000
[6] SML #2000-0472 “Analysis of the DuchessII Chip Measurements,” Jon Lexau, 28 August 2000

Introduction

We have fabricated the duchess family of chips [1,2] primarily to calibrate the wire loading models that we use for hspice simulation. These models are presented in [4,6]. There are also a number of rings on these chips which do not have any wire loading so that we can study some basic inverter properties. In this memo, I attempt to draw some useful conclusions from the data the Jon Gainsley has gathered and reported in [5].

Result Summary

Here is a quick summary of the results. Note that in this memo, the drain node of a transistor refers to its output node, as opposed to the source, or power-connected node.

1. The miller killer inverters we added to most of the rings have only a small impact on performance, contrary to our expectations. The performance difference is on the order of 3-4%.
2. We are able to extract very good information about inverter performance vs drain area.
3. Folding a transistor in half to create a shared drain improves performance by about 12%, primarily due to the reduced drain area.
4. Using fewer drain contacts improved inverter speed by 11.2%, again due to the reduction in area. No comment is made here about the effects on reliability, current handling, etc.
5. Longer source and drain regions (3x normal length) resulted in 8.4% slower operation.

Raw Data

The table below records the raw data which were gathered by Jon Gainsley and reported in [5]. I have grouped the rings accorded to the size of the inverter transistors and how they are laid out. The complete list of test rings is given in [3].

inv size	ring id	stage load	period (ns)
N=2µ:P=4µ non-folded inverters	ring00	next inverter	4.75
	ring01	2 inverters (next inv plus one)	6.45
	ring02	3 inverters (next inv plus two)	8.17
	ring03	3 inverters, no miller killer	8.41
N=4µ:P=8µ folded inverters	ring10	next inverter	3.61
	ring11	2 inverters	5.19
	ring12	3 inverters	6.79
	ring13	3 inverters, no miller killer	7.12
N=4µ:P=8µ non-folded inverters	ring14	next inverter	4.06
	ring15	next inverter, few active contacts	3.65
	ring16	next inverter, extra-wide drain	4.40

Table 1: Measured Results from [5]

Conclusions

In the following sections, I will comment briefly on each of the inverter ring tests performed.

Miller Killers

In both versions of the duchess chip, we have built the same ring with and without “miller killer” inverter loads. Surprisingly, we do not see as much slowdown as might be expected when the miller killer inverters are removed in rings 03 and 13. The performance loss is on the order of 3-4%. I do not have an explanation for this.

Transistor Folding

In an ideal world, we would expect the periods of rings 00 - 03, using 2µ:4µ inverters, to exactly match those of rings 10 - 13, with 4µ:8µ inverters. The reason that they do not is because of the fairly substantial piece of wire between adjacent stages of the ring, at least compared to the inverter sizes we are using. I have commented on this in [2], and performed my wire model analysis in a way that factors this out. One of the reasons for adding rings 14 - 16, which also use 4µ:8µ inverters, on the duchessII chip was to allow a direct comparison of the impact of transistor folding, which was not possible with the first duchess chip.

On this chip, we can compare rings 10 and 14 directly as the total inverter sizes are the same; only the layouts differ. We see that a 12.5% performance improvement is gained by folding the transistors, which significantly reduces the area of the drain region.

Transistor Modifications

DuchessII contains two final inverter tests to test what can happen with some common gate layout variations.

In ring15, there is only 1 contact for each source or drain region. In ring14, for example, there are 3 contacts for each n-type transistor and 6 contacts for each p-type. We see that performance improves by about 11.2%, but much, if not all, of this difference is due to the fact that the area of the source/drain regions is significantly reduced when there are fewer contacts. We do not currently know how reducing the number of contacts affects other factors such as long-term reliability, current handling capability, etc.

In ring16, the length of both the source and drain region of every transistor was artificially increased by 0.4 μm, or 2λ. Remember that the minimum allowable length is 0.2 μm, or 1λ. Such an increase in length often occurs when two transistors of different widths share a common source or drain because of the poly to active spacing rules. We see a performance drop of about 8.4% in this case, but this particular test probably represents an upper bound on the length increase that we might typically see in a real design.

We would like to see if we can make some statement about the effect that drain area and perimeter have on the inverter performance. The table below gives the drain area and perimeter for four of the test rings, each with 4μ:8μ total inverter size. I have sorted them in order of increasing period, which also happens to be increasing drain area. The layouts for rings 14 - 16 are nearly identical, except for the shape of the drain regions, which is perfect for this test. I am including ring10, the folded inverter ring, in the table to see how well it fits with the others.

ring	drain area			drain perimeter			period (ns)
	N (μm^2)	P (μm^2)	total (μm^2)	N (μm)	P (μm)	total (μm)	
ring10	2.4	4.8	7.2	2.4	2.4	4.8	3.61
ring15	2.9	5.3	8.2	6.2	10.2	16.4	3.65
ring14	4.4	8.8	13.2	6.2	10.2	16.4	4.06
ring16	6.0	12.0	18.0	7.0	11.0	18.0	4.40

Scale drawings of the 4 μm NMOS transistor in the inverter for each ring are shown in Figure 2 on page 63. In each case, the layout for the 8 μm PMOS transistor is similar. For these inverter rings on duchessII, the primary performance determiner is the shape of the drain region, as this sets the output node capacitance. In ring16, it might have been better to leave the source side of the transistor at the minimum length and only increase the drain side. The main effect of the longer source region is to increase the resistance to the power supply. Fortunately, the resistivity of the active regions is fairly low; better than poly by a factor of 2 or more.

Figure 1 on page 62 graphs ring period vs total drain area for these four rings. I have chosen to drawn a “best-fit” straight line through the two points for rings 14 and 15, as they have exactly the same drain perimeter. The perimeter for ring16 is about 10% more than rings 14 and 15, and so it should be a bit slower than the best-fit line, which it is. As mentioned above, this ring also has extra source resistance which may also slow it slightly. However, because the perimeter is so much smaller for ring10, I would expect that point to be somewhat below the line, but it is not. I believe that this is because the polysilicon wire connecting to the gate of the inverter is longer in ring10 than in rings 14 - 16. This is because the inverter folding requires connections to more individual transistors.

Fortunately, using the wire model analysis in [6], we can compensate for this. The additional per-stage wire length in ring10 is 5.0 μm over the other rings. Using the best-fit curve for poly wires from [6], we can find that this corresponds to an extra 136.1 ps of delay in the ring. Thus we can estimate that, with shorter poly wires, ring10 would have a period of 3.61 - 0.136 = 3.47 ns. This point, labelled ring10-adj, is also plotted in Figure 1 and we can see that it is well below the line through the other three points, as we expect.

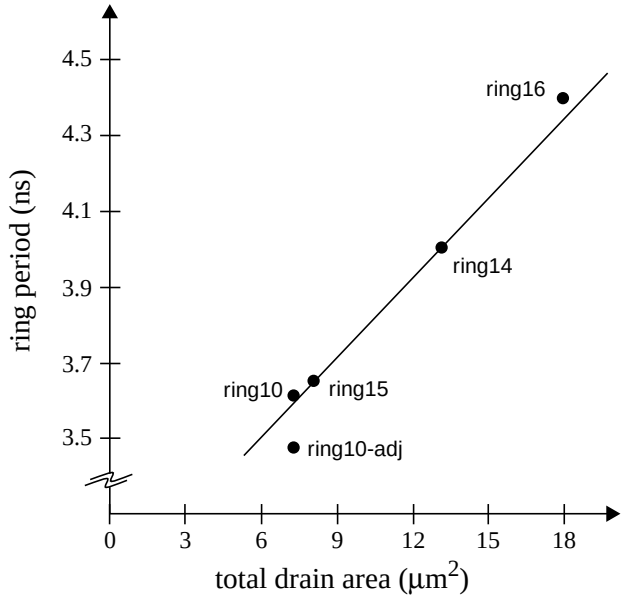
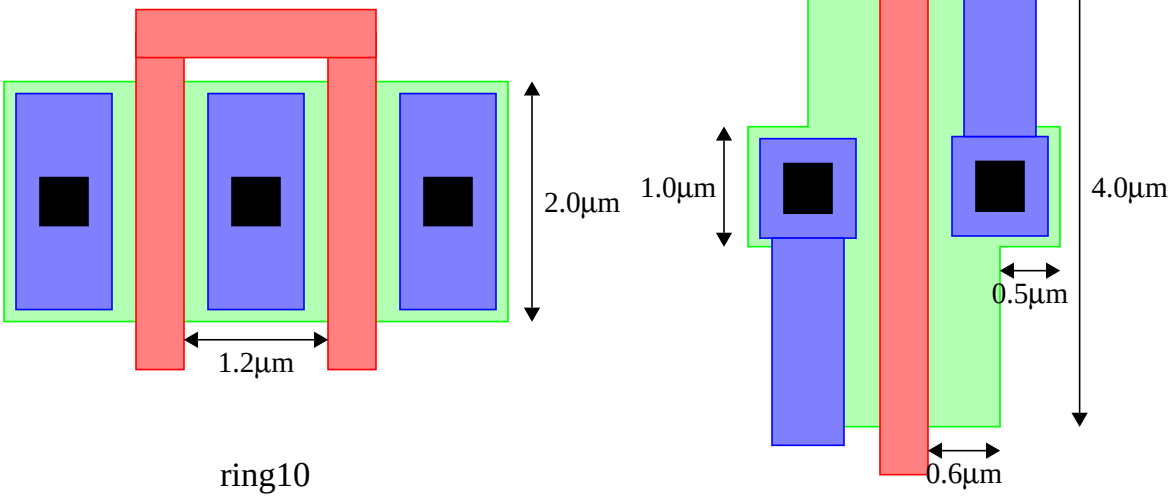


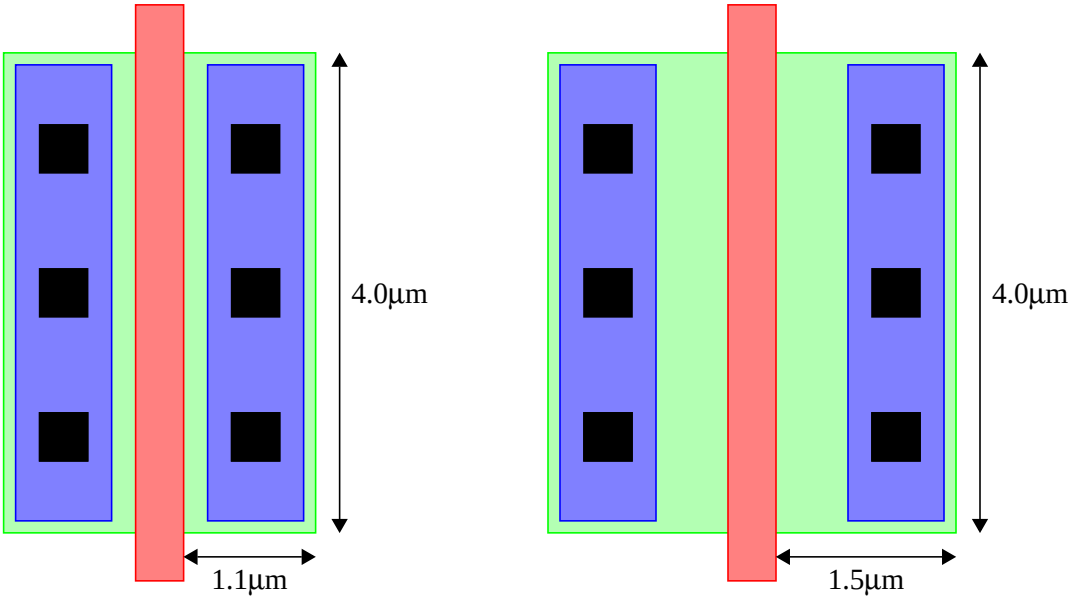
FIGURE 1. Ring Period vs Total Drain Area

A suggestion for the next duchess chip would be to artificially increase the poly routing in rings 14 - 16 to match that of ring10 so that we can verify this prediction. The increase is fairly modest and would probably be easier than trying to reduce the routing in ring10. It would be very nice if we could find a set of rings which would allow us to separate the effects of drain area from drain perimeter. Thus far, we have not determined the best layouts to do this.



ring10

ring15



ring14

ring16

FIGURE 2. Scale Layouts for the 4µm NMOS Transistors

Sun Microsystems Laboratories

Title: **The DuchessII Chip (CHIP)**
Date: **23 May 2000**
Author: **Jonathan Gainsley**
SML #: **2000-0247**

References:

[1] SML# 2000-0002: "The Duchess Chip," *Sutherland, Gainsley, Coulthard*, 6 Jan 2000
[2] SML# 2000-0005: "A Ring Oscillator Speed Test Proposal," *Sutherland*, 7 Jan 2000
[3] SML# 2000-0261: "Analysis of the Duchess Chip Measurements", *Lexau*, 6 June 2000
[4] SML# 2000-0262: "Rings for the DuchessII Chip," *Lexau, Gainsley*, 6 June 2000

Introduction

This memo documents the existence of the DuchessII Chip. The DuchessII chip follows in the footsteps of the original Duchess Chip [1], originally proposed by Ivan [2]. The Duchess Chip consists of ring oscillators of various loading to experimentally measure the effects of different types of loading on transistor speed. These experimental results are then used to verify the accuracy of our spice wire models. Jon Lexau has taken the results of testing the Duchess Chip and documented this analysis in [3].

The DuchessII

The DuchessII adds a few more rings the number of rings in Duchess, as Jon and I have come up with a number of new rings that should provide us with even more information on ring loading. Reference [4] documents the new rings.

Sun Microsystems Laboratories

Title: **DuchessIII - Changes from DuchessII**
Date: **30 Jan 2001**
Author: **Jonathan Gainsley**
SML #: **2001-0092**

References:

[1] SML# 2000-0247: “The DuchessII Chip (CHIP),” Gainsley, 23 May 2000
[2] SML# 2001-0076: “DuchessIII - The Chip,” Gainsley, Sutherland, Richards, 22 Jan 2001
[3] SML# 2000-0262: “Rings for the DuchessII Chip,” Lexau, Gainsley, 6 Jun 2000

Introduction

This memo documents the changes made to DuchessII chip [1] to upgrade it to the DuchessIII [2] chip. The rings on the DuchessII chip are described in [3].

Changes

A) Bug fix: VddI no longer powers rings 32 and 34. It now only controls ring 32. VddM now powers both rings 35 and 34. This is because the outputs of rings 32 and 34 go to the same OR tree, so the rings must be able to run separately.

B) Ivan and Bill Richards, at Bill’s request, added probe pads to be able to test transistors of different sizes.

C) DRC rules: The layout conforms to the MOSIS 4 metal layer, 1 poly layer submicron (SUBM_4M) DRC ruleset. The only exception is the glass cut design rules, which are tighter than the suggested MOSIS rules, and tighter than the DRC ruleset we had set up in Cadence. Bill and I are not sure where the latter dimensions came from, but we suspect it conforms to an older HP process. In any case, they are well within the 0.35u TSMC process ruleset, and I doubt there should be a problem, especially because it applies only to the probe pads, and not the bonding pads.

I asked Bill R. about different rules for the FermiFET process, and he did not mention any.

Sun Microsystems Laboratories

Title: **DuchessIII - The Chip**
Date: **22 Jan 2001**
Author: **Jonathan Gainsley, Ivan Sutherland, Bill Richards**
SML #: **2001-0076**

References:

[1] SML# 2000-0247: “The DuchessII Chip (CHIP),” Gainsley, 23 May 2000
[2] SML# 2001-0077: “The Duchess Release,” Sutherland, 22 Jan 2001
[3] SML# 2001-0092: “DuchessIII - Changes from DuchessII,” Gainsley, 30 Jan 2001

Introduction

The DuchessIII chip is the DuchessII chip [1] with two changes [3]. The first change is a bug fix. The second is the addition of some probe pads put together by Ivan and Bill Richards to test transistors.

The DuchessIII chip was released [2] to be manufactured by the Thunderbird group in the FermiFET process, which we hope will yield much greater speeds at the same feature size due to changes in the basic transistor design. Bill Richards is a part of this group and has been our main liaison. His email is richards@tbird.com.

Figure 1 is a plot of the DuchessIII chip.

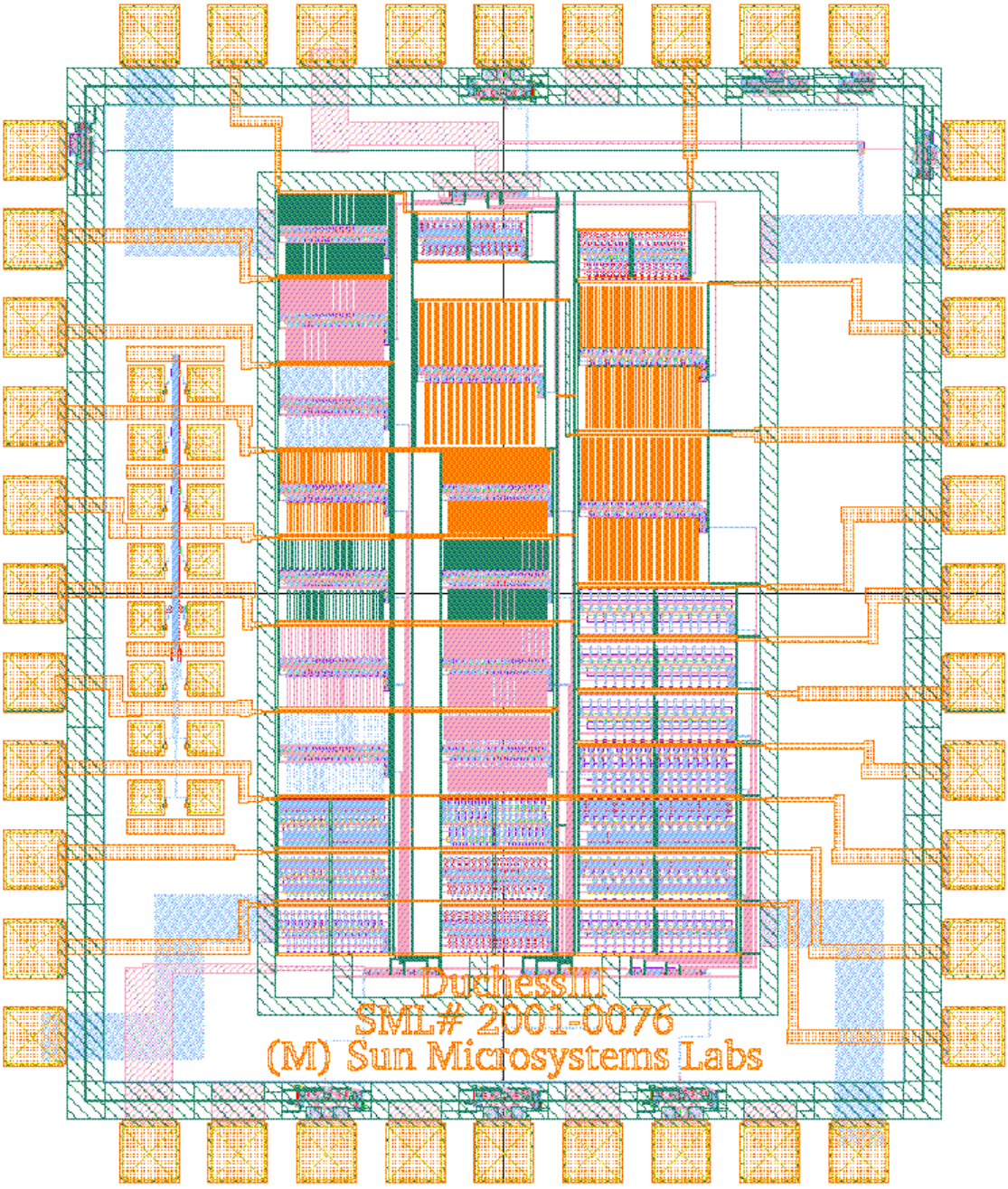


Figure 1: Plot of the DuchessIII Chip

Appendix

Appendix A

Schematics

2000−0013 Schematics for the Duchess Chip
Gainsley, 10 January 2000

Sun Microsystems Laboratories

Title: **Schematics for the Duchess Chip**
Date: **10 Jan 2000**
Author: **Jonathan Gainsley**
SML #: **2000-0013**

References:

[1] SML# 2000-0002: “The Duchess Chip,” Sutherland, Coulthard, Gainsley, 4 Jan 2000
[2] SML# 2000-0005: “A Ring Oscillator Speed Test Proposal,” *Ivan Sutherland*, 5 Jan 2000

Introduction

This memo archives the schematics for the Duchess Chip [1]. Refer to [2] for a description of the chip. The schematics were created using Sue4 by Ivan Sutherland.

Organization

This memo is organized by the different types of components of the chip. Schematics are archived in:

/proj/async/db/2000/duchess_2000_0002/schematics/

At the end of the memo are the schematics contained within the pad library directory,

/proj/async/db/2000/duchess_2000_0002/schematics/suelib_pads/

Top Level Schematics - pages 3-4

Duchess.sue
ringGuts.sue

Or Gate Schematics - pages 5-7

or8.sue
orGate.sue
orLoad.sue

Ring Schematics - pages 8-32

ring00.sue	ring01.sue	ring02.sue	ring03.sue	(pages 8-11)
ring10.sue	ring11.sue	ring12.sue	ring13.sue	(pages 12-15)
ring20.sue	ring21.sue	ring22.sue	ring23.sue	ring24.sue (pages 16-20)

ring30.sue	ring31.sue	ring32.sue	ring33.sue	ring34.sue	(pages 21-25)
ring41.sue	ring42.sue	ring43.sue	ring44.sue	ring45.sue	(pages 26-30)
ringXX.sue					

Inverter Schematics - pages 32-40

inv.sue				
inv00.sue	inv01.sue	inv02.sue	inv03.sue	(pages 33-36)
inv10.sue	inv11.sue	inv12.sue	inv13.sue	(pages 37-40)

Wire Load Schematics - pages 41-56

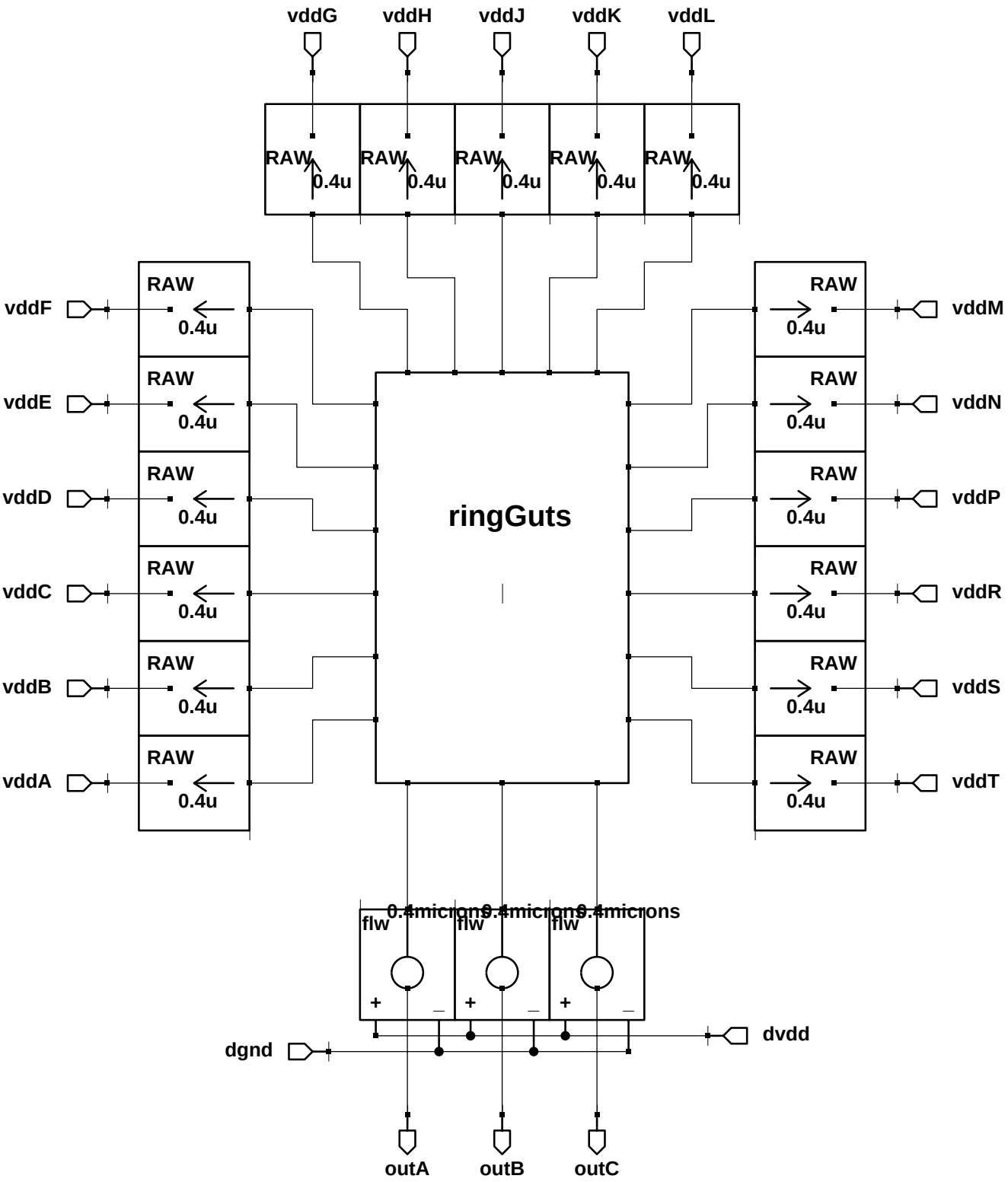
polyWire.sue					
wire.sue					
wire0.sue					
wire21.sue	wire22.sue	wire23.sue	wire24.sue	(pages 44-47)	
wire31.sue	wire32.sue	wire33.sue	wire34.sue	(pages 48-53)	
wire41.sue	wire42.sue	wire43.sue	wire44.sue	wire45.sue	(pages 54-56)

Ring Output Driver - page 57

driver.sue

Pad Library Schematics - pages 58-59

pad_flwout.ps
pad_raw.ps



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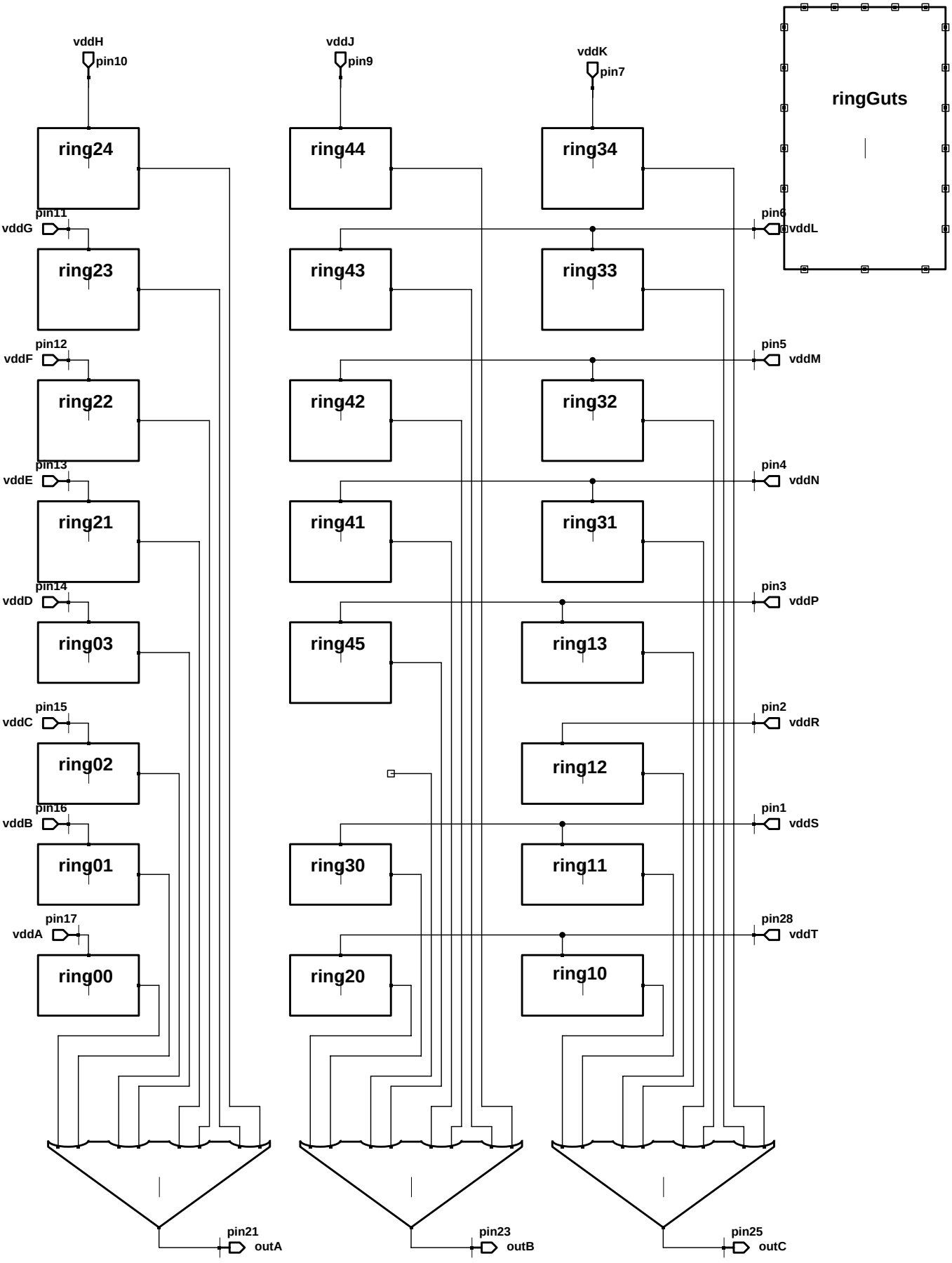

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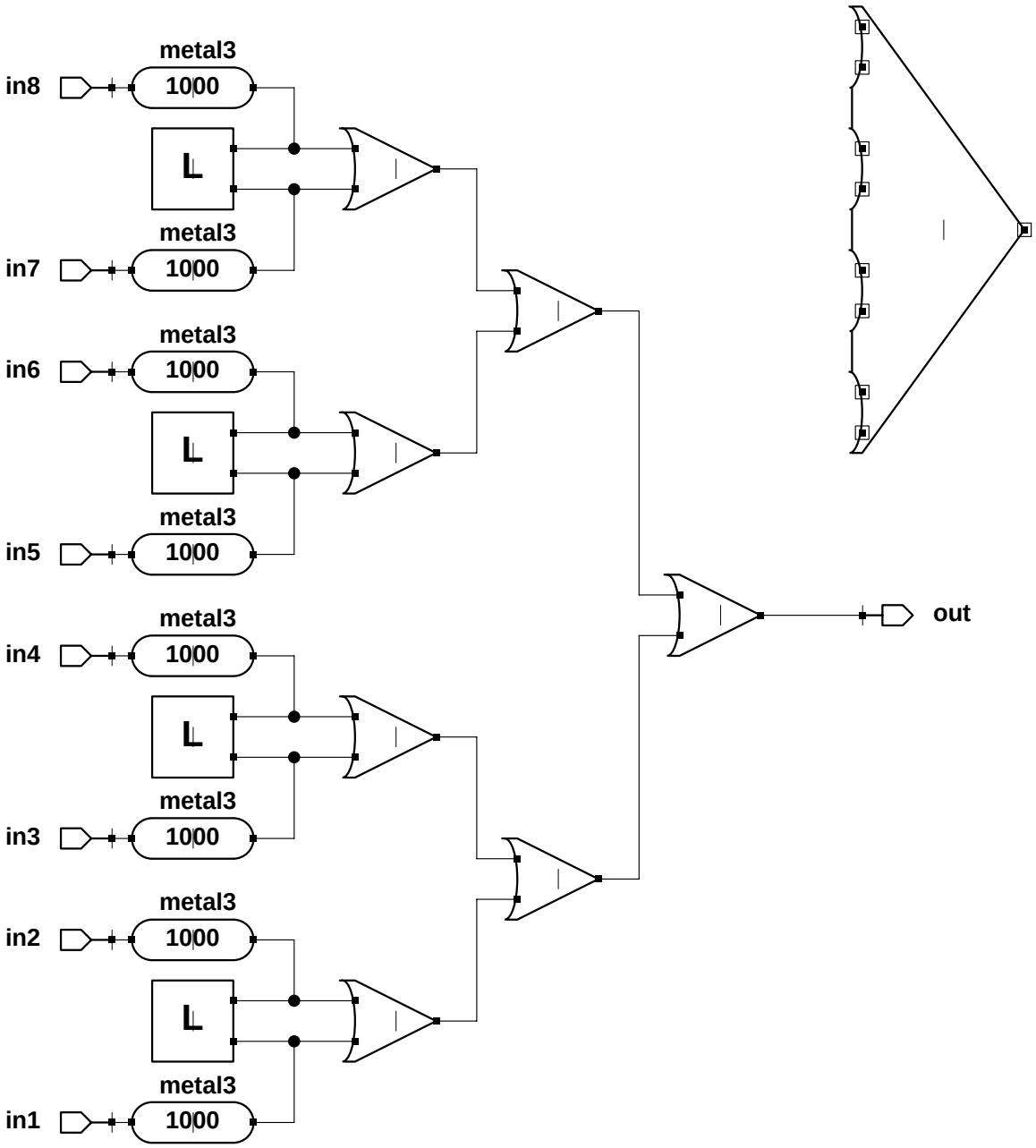

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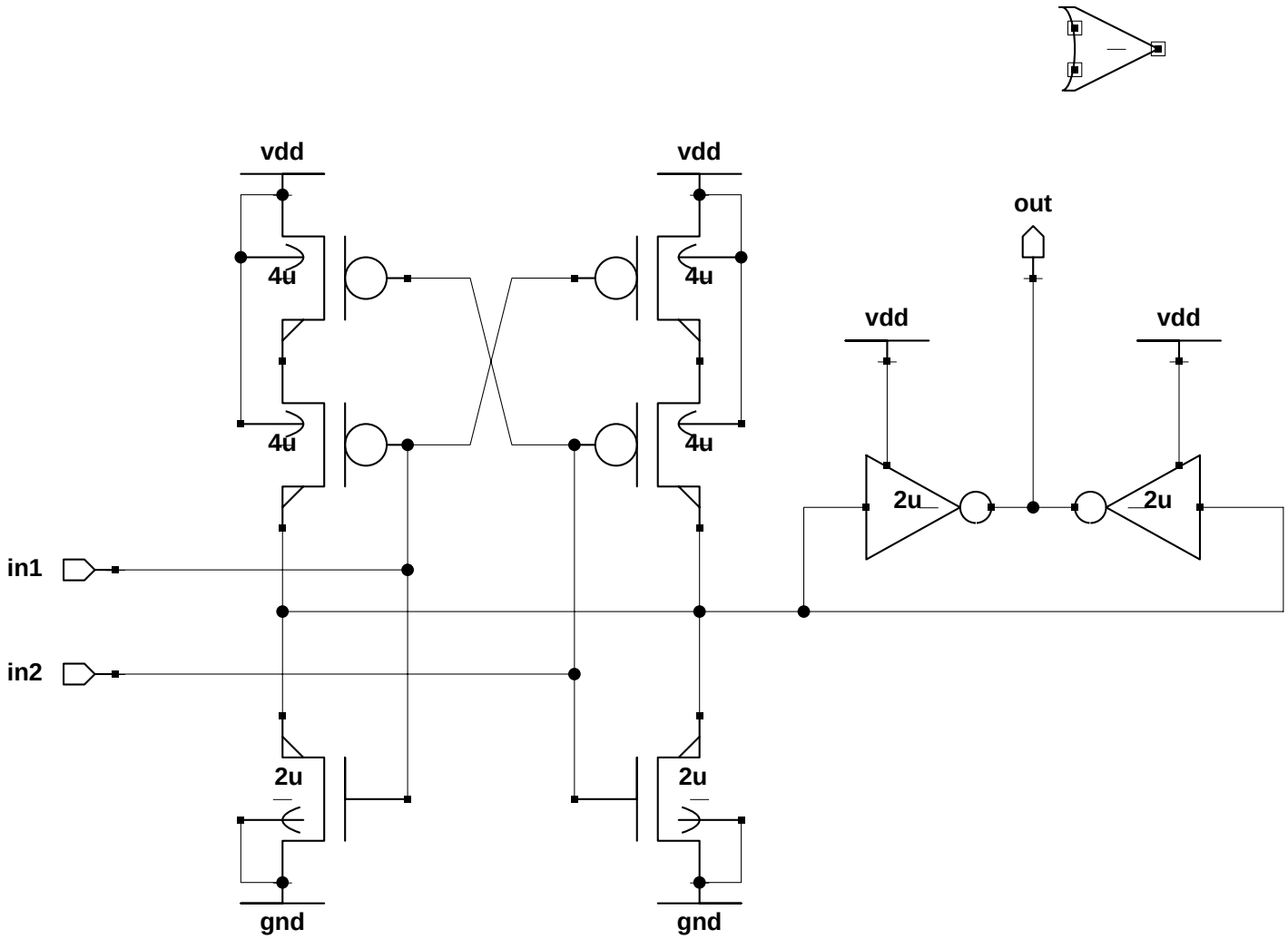

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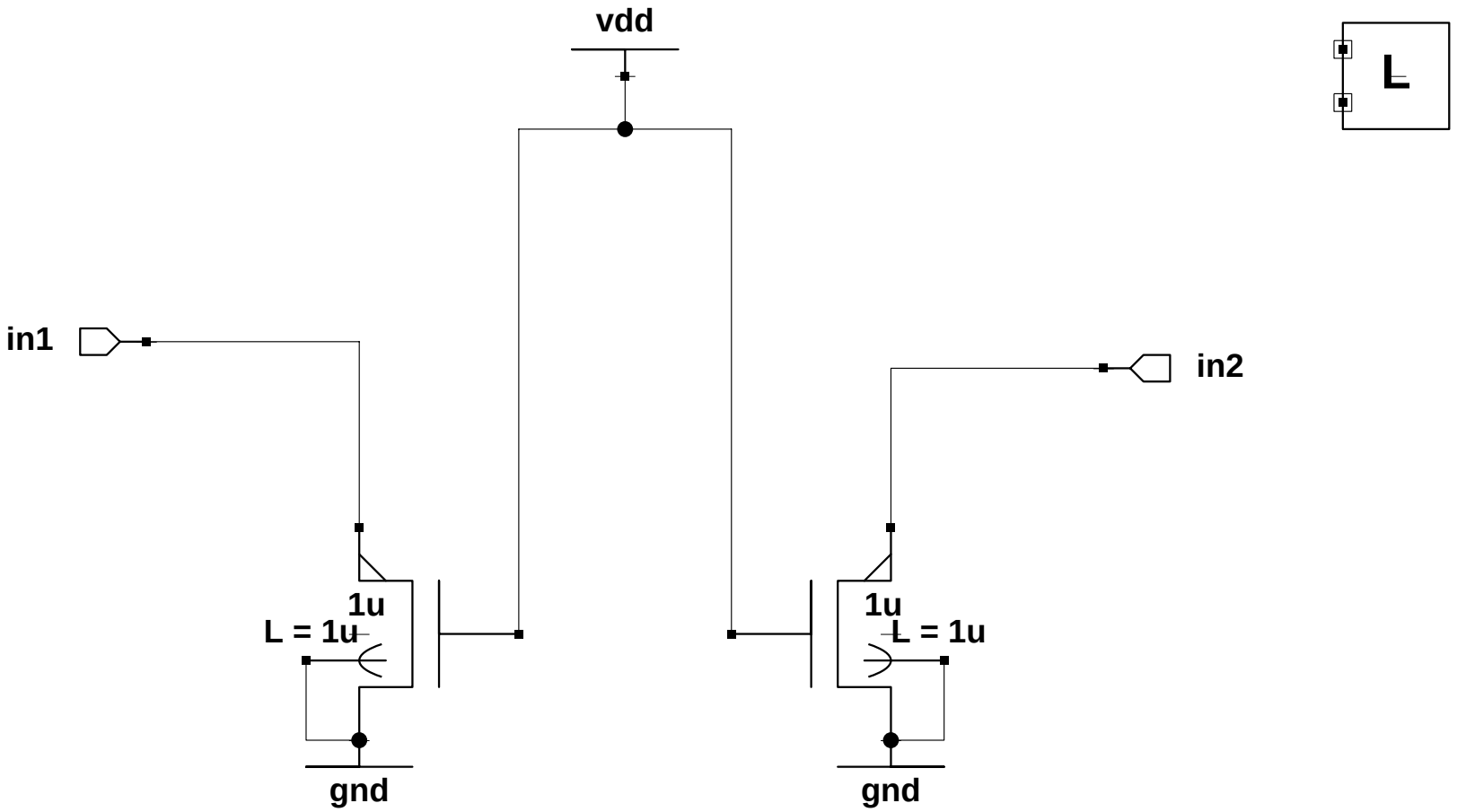

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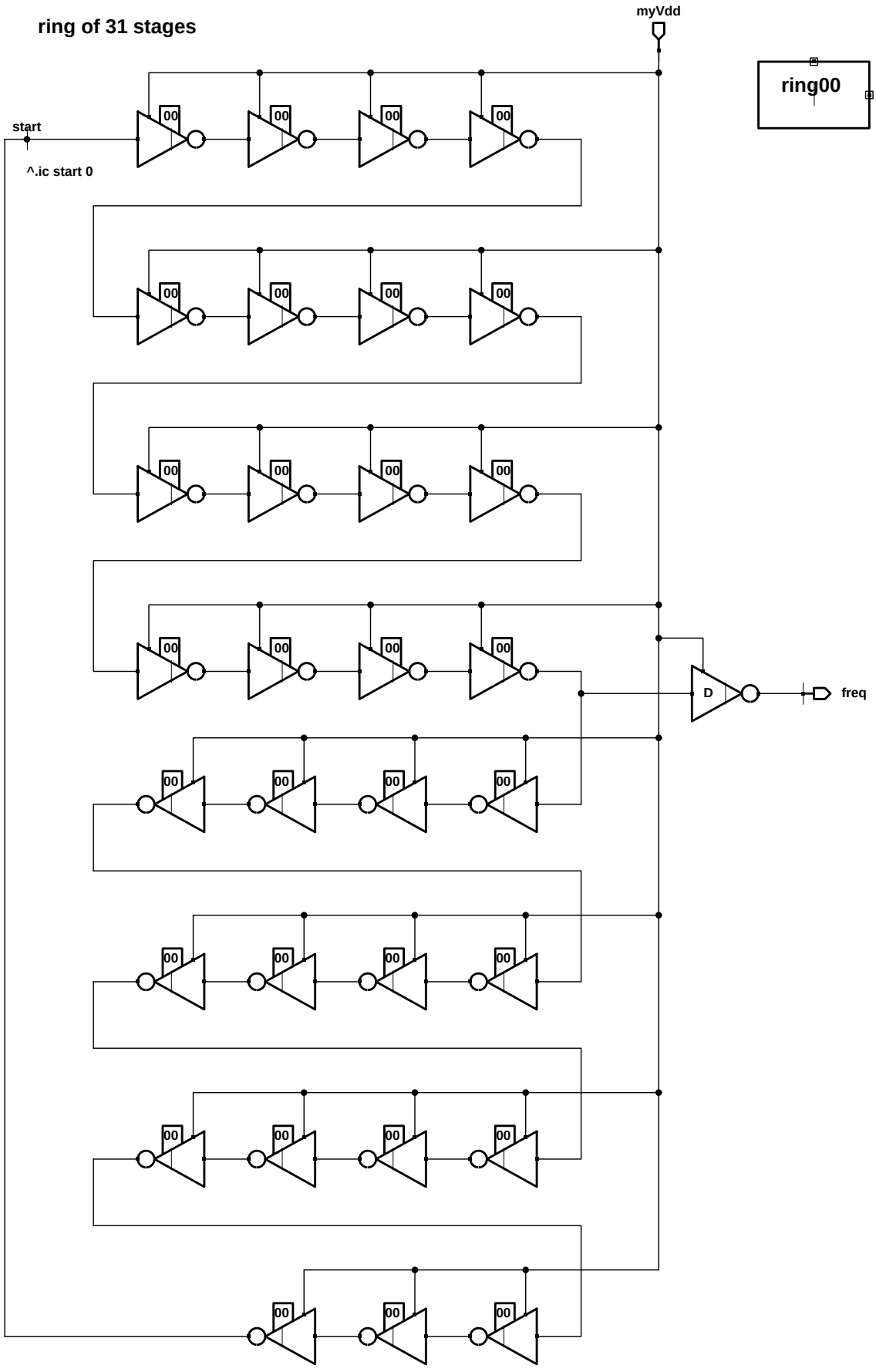

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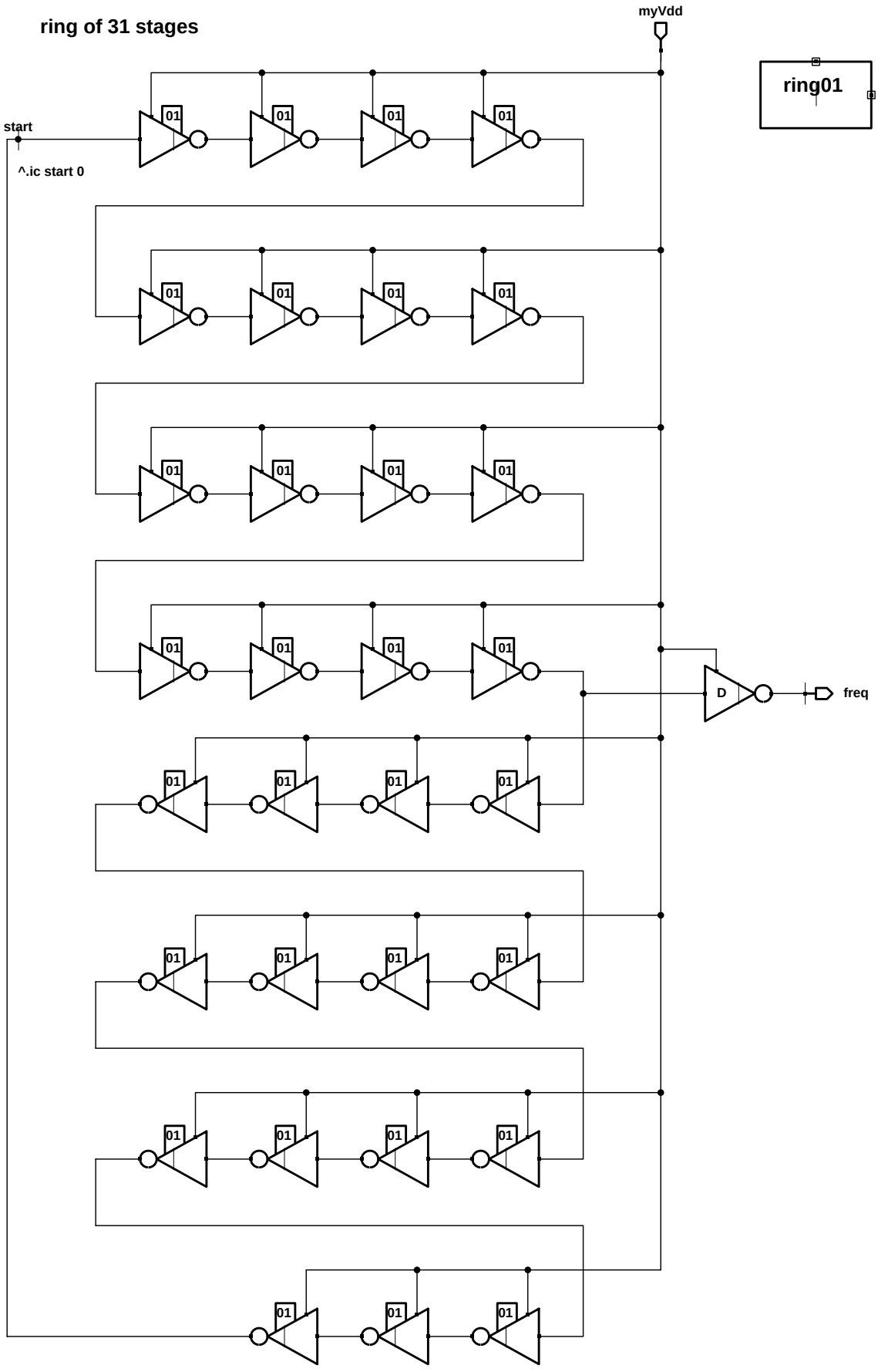

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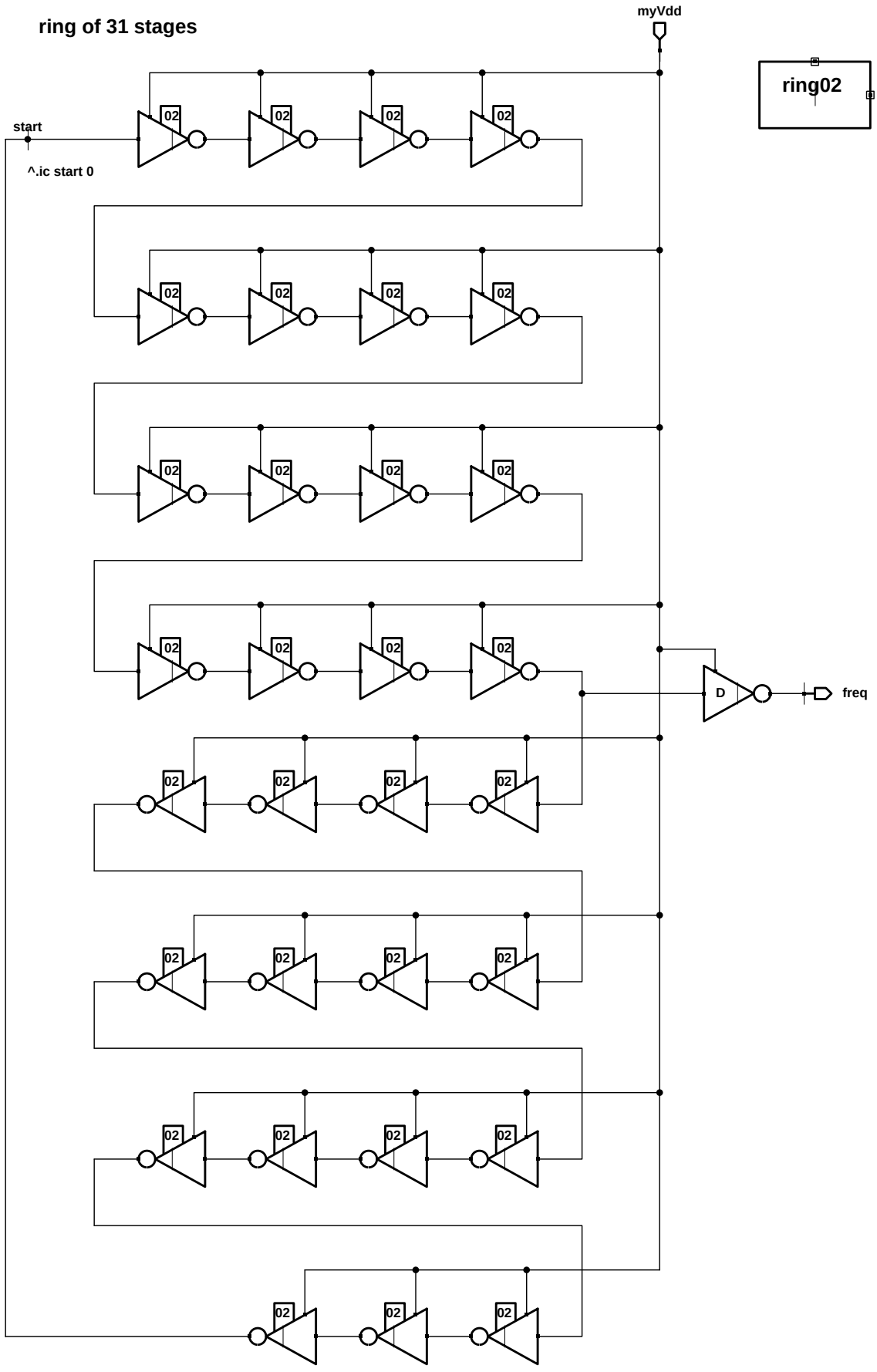

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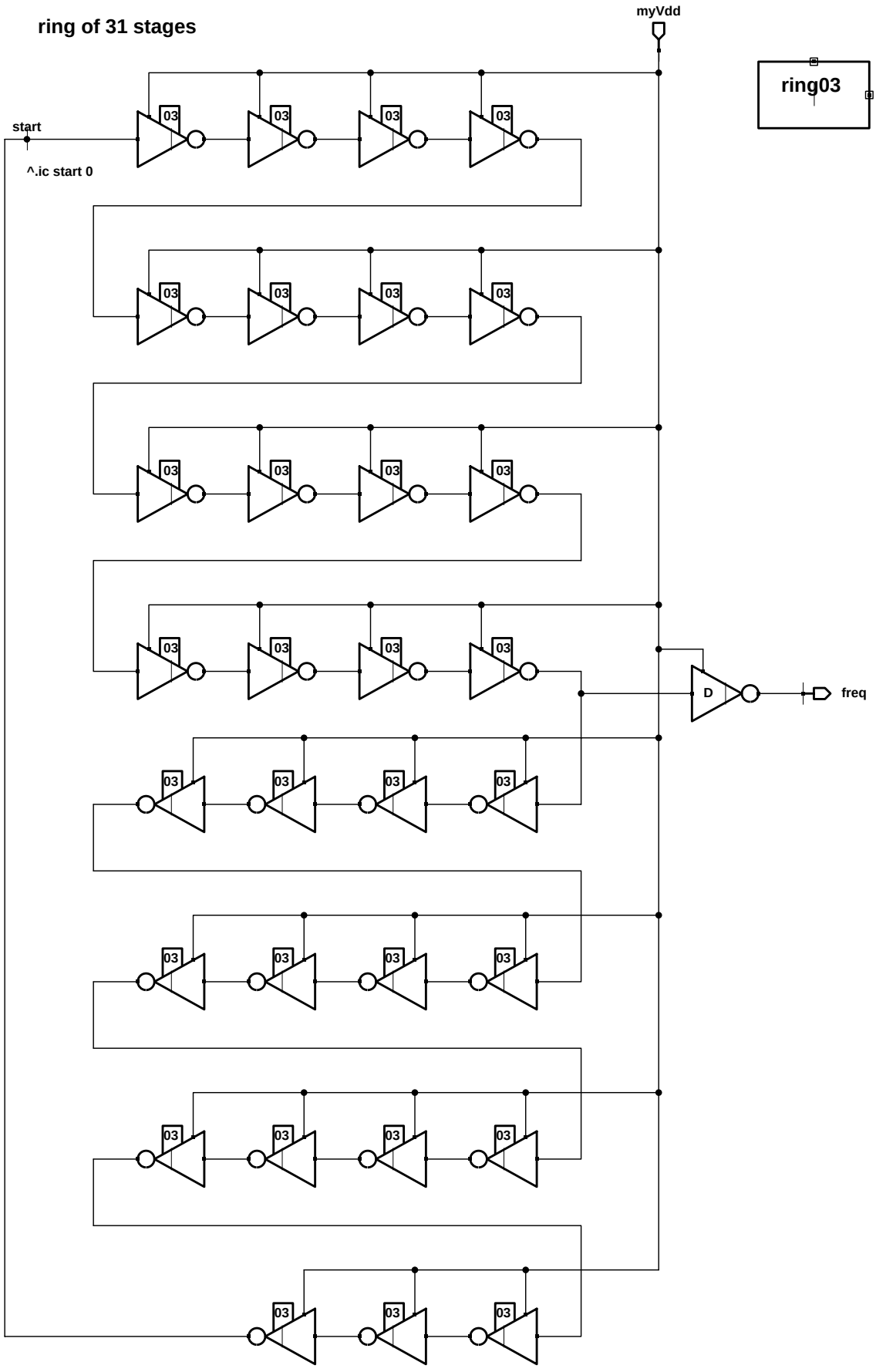

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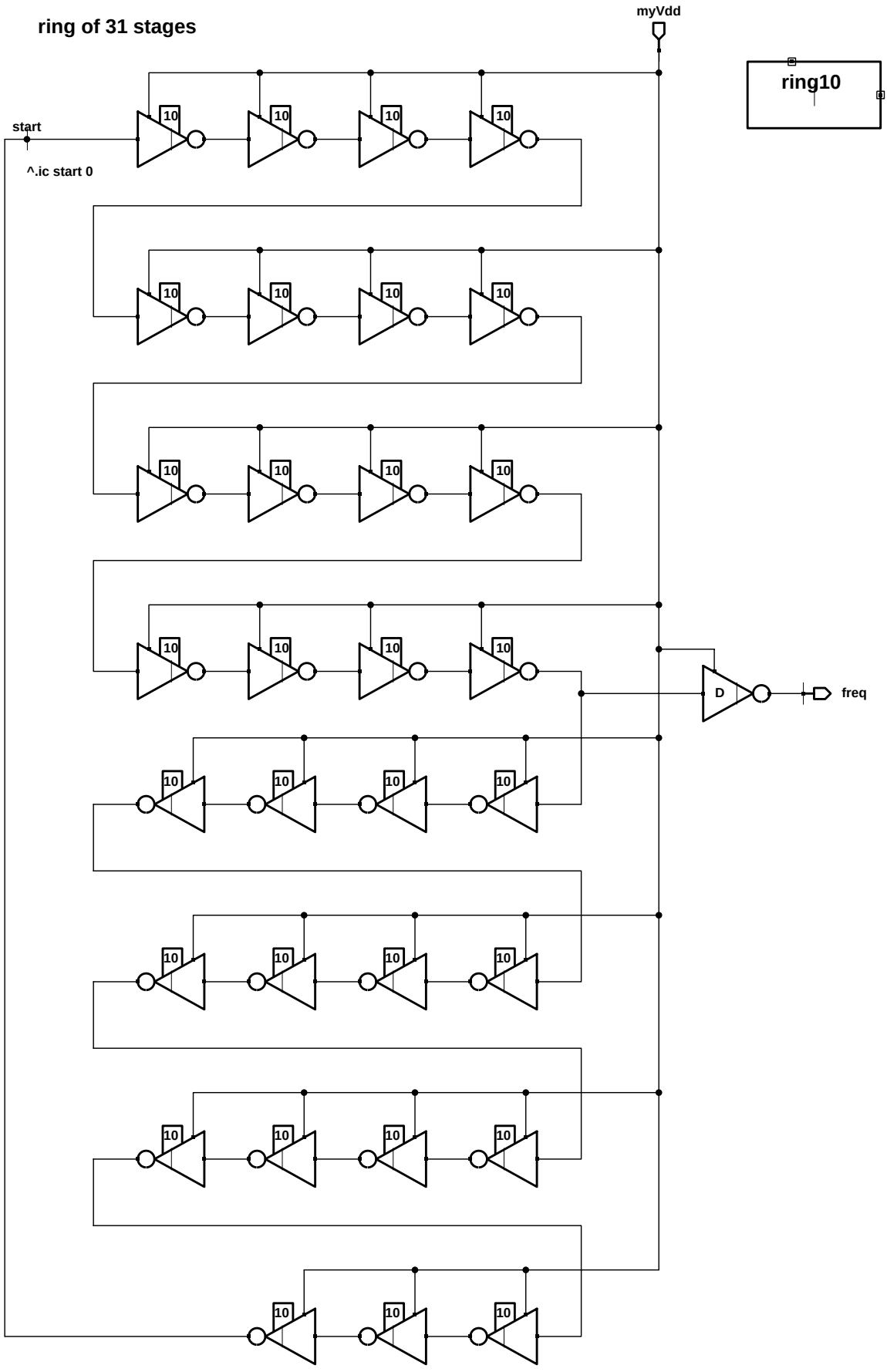

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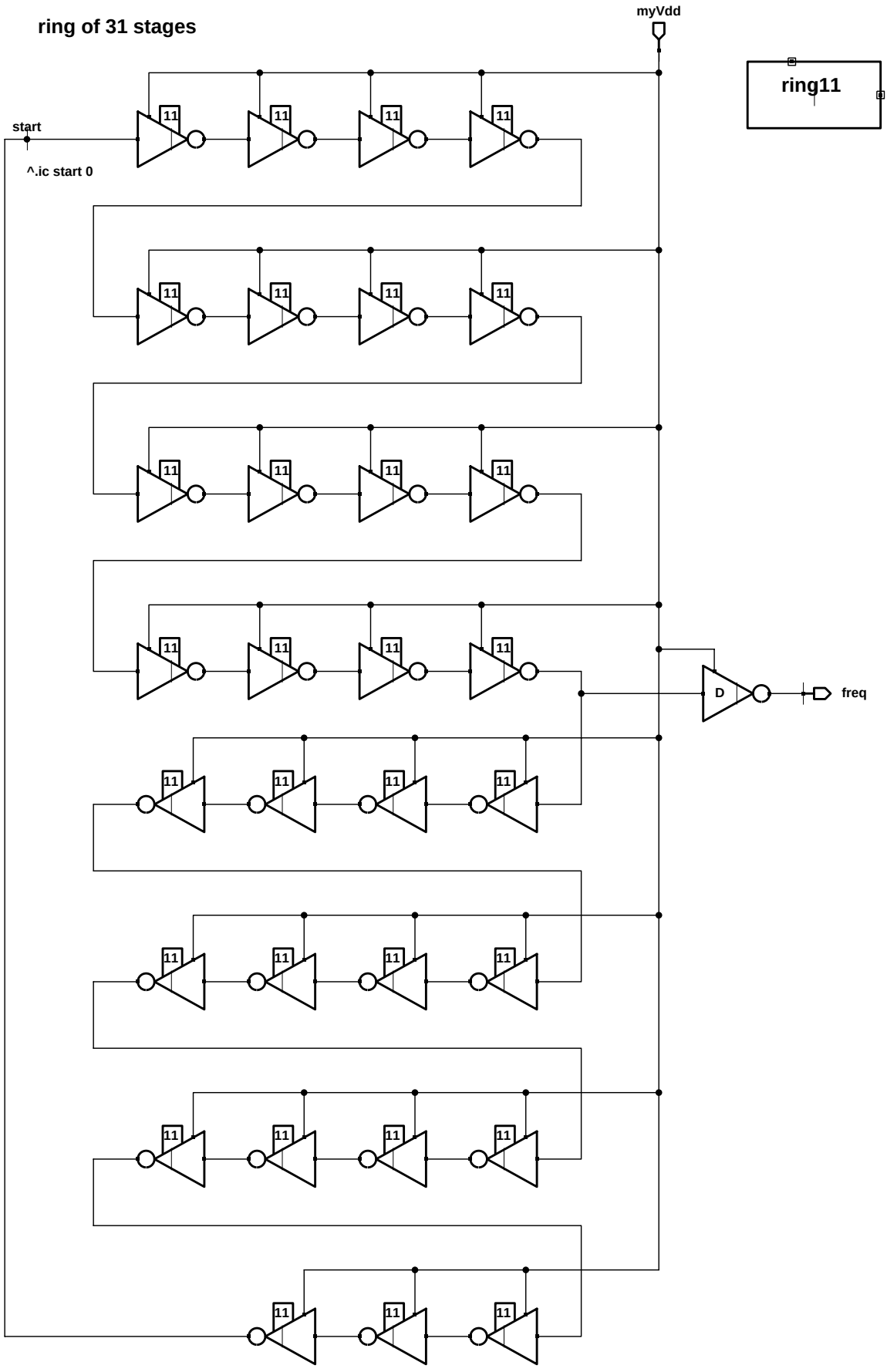

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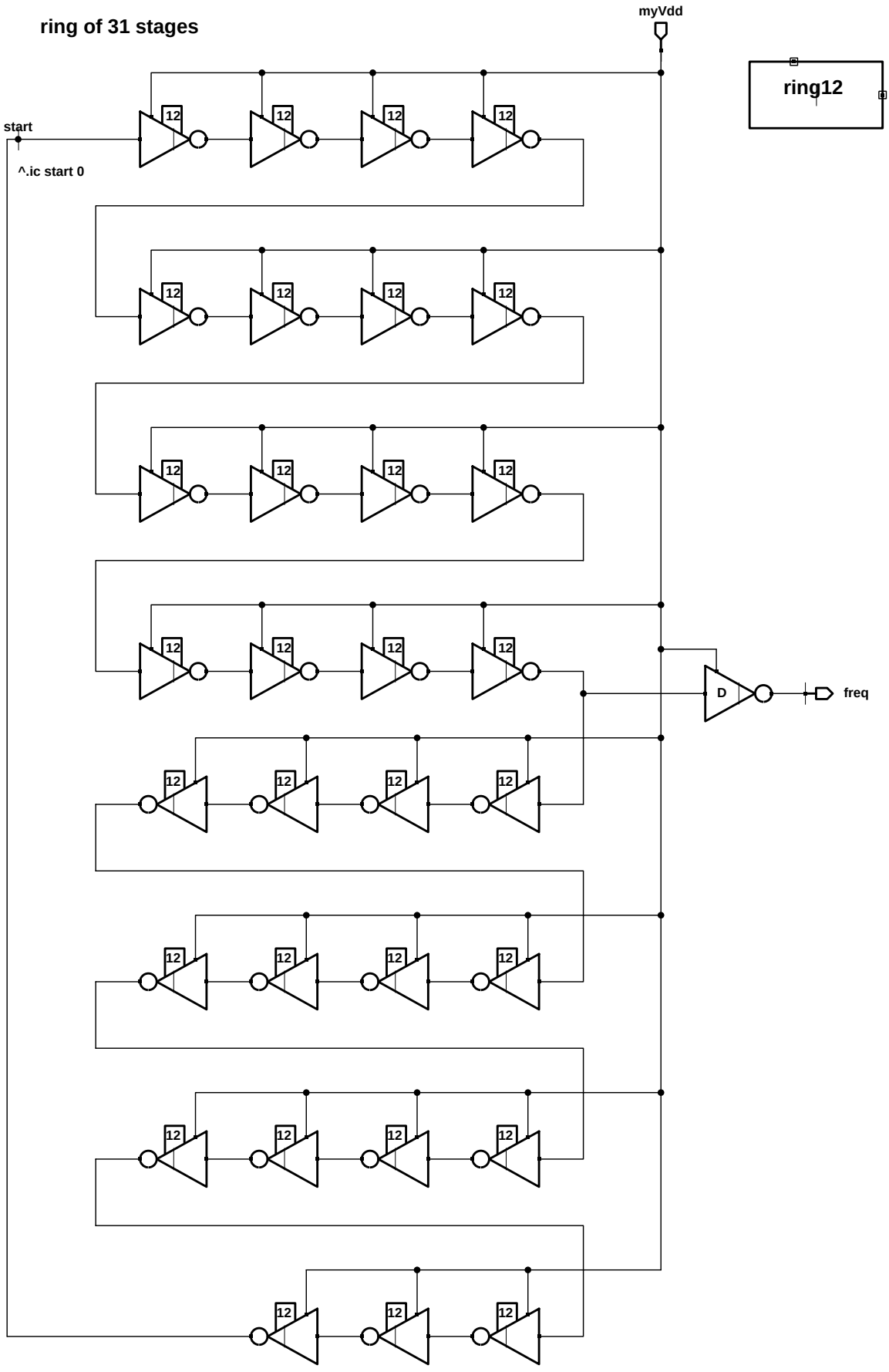

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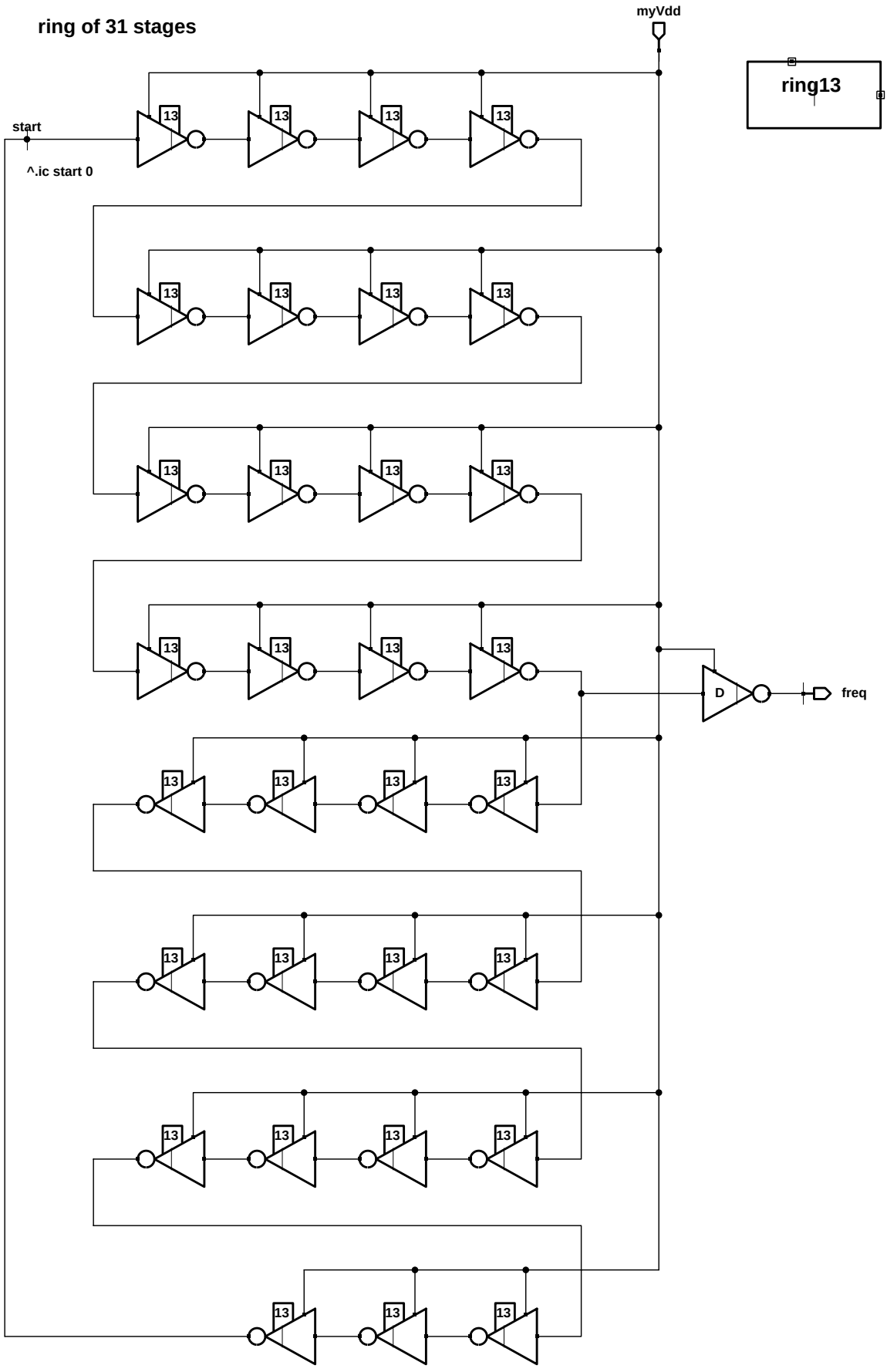

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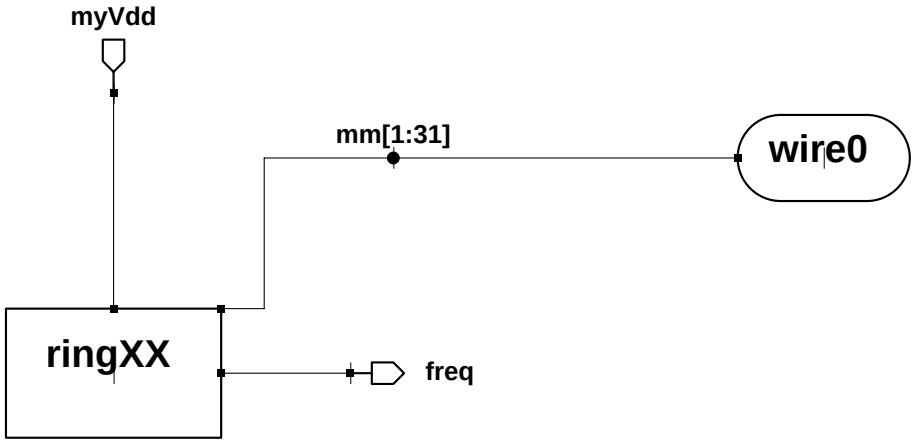
ring20

this has 50 micron poly wire loads



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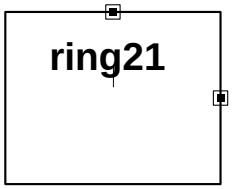
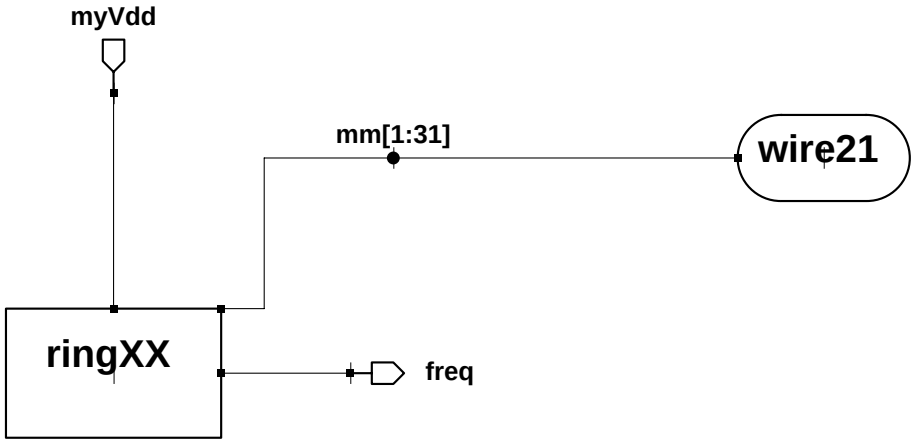


this has 100 micron metal 1 wire loads



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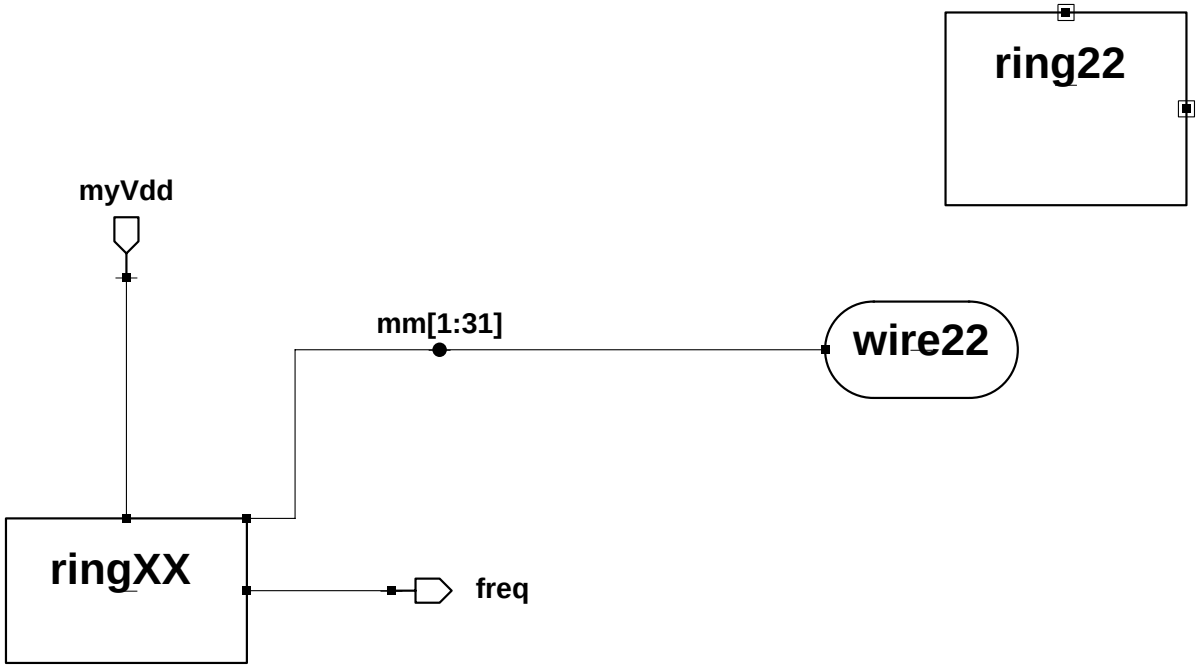
this has 100 micron wire loads



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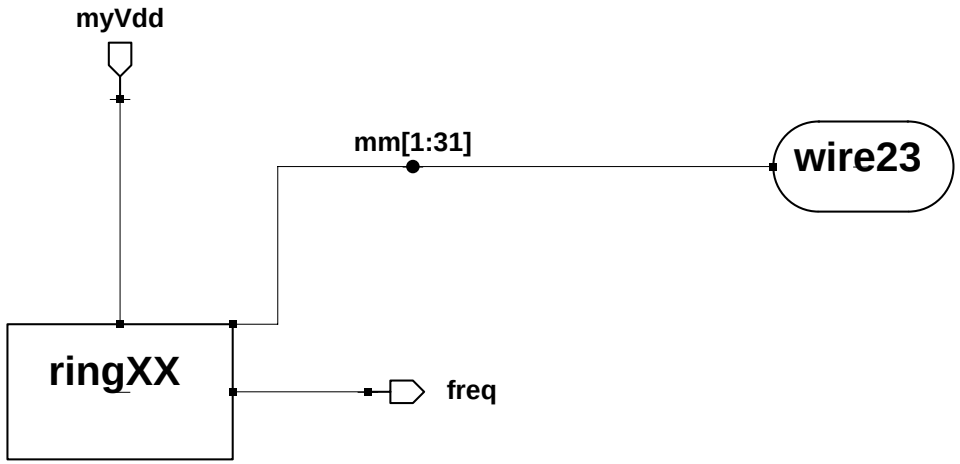
this has 100 micron wire loads

ring23



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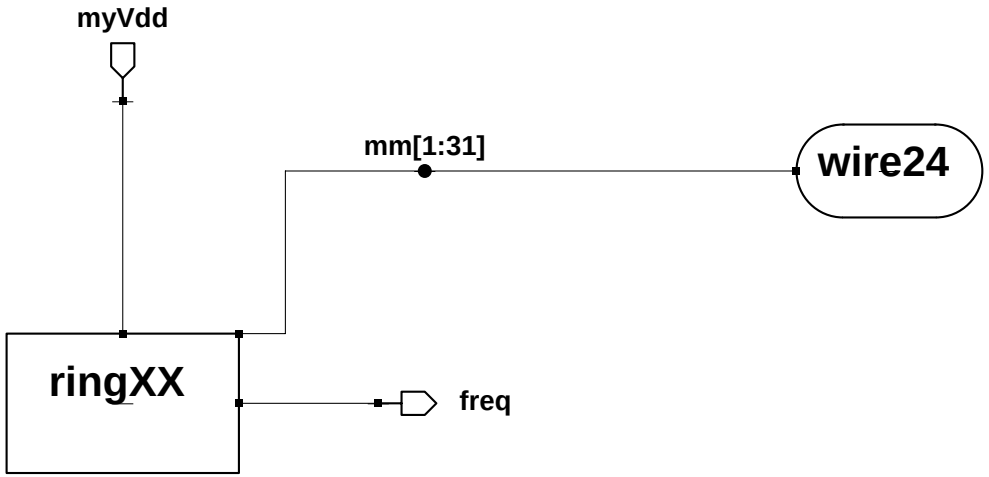
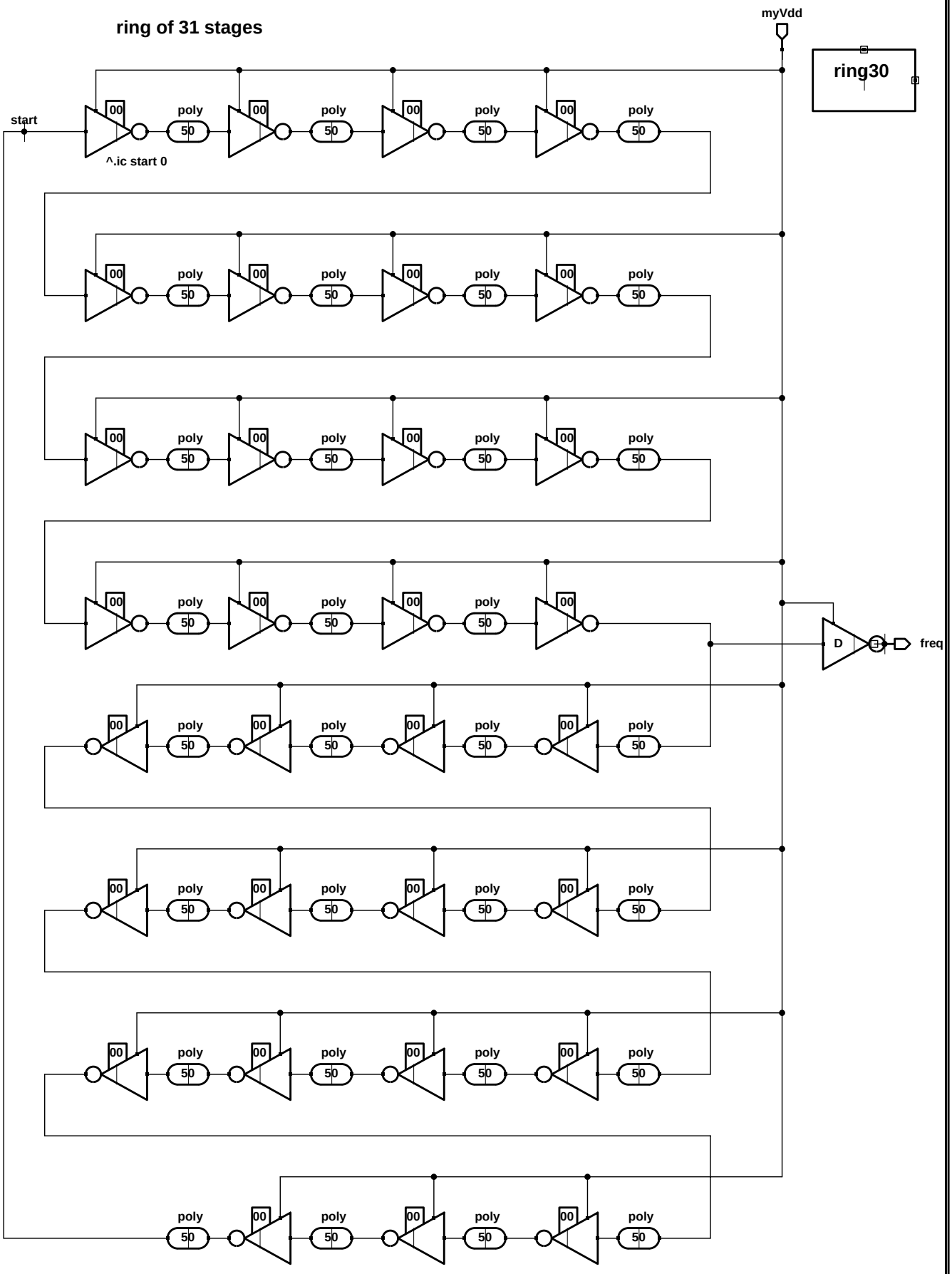
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

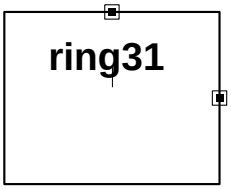
this has 100 micron wire loads



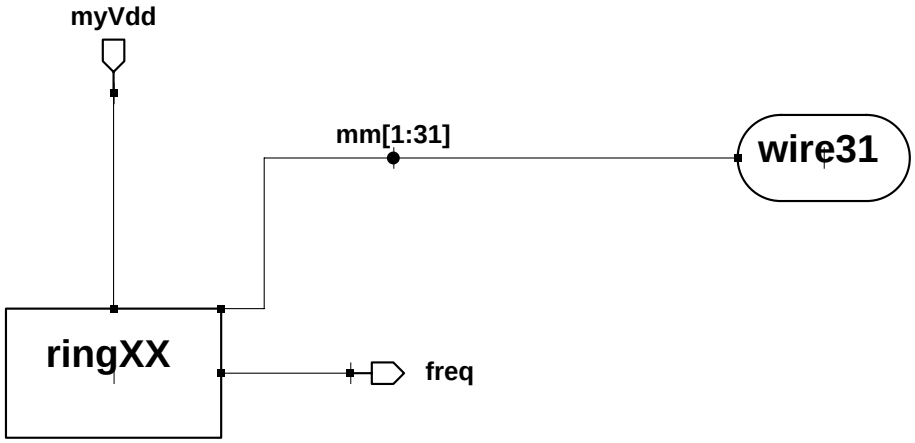
Sue 4.0	Cell: Version: %I% **ring24**	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/ring24.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



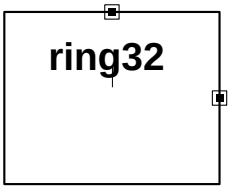
Sue 4.0	Cell: ring30 Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/ring30.sue
title_sun_AP	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



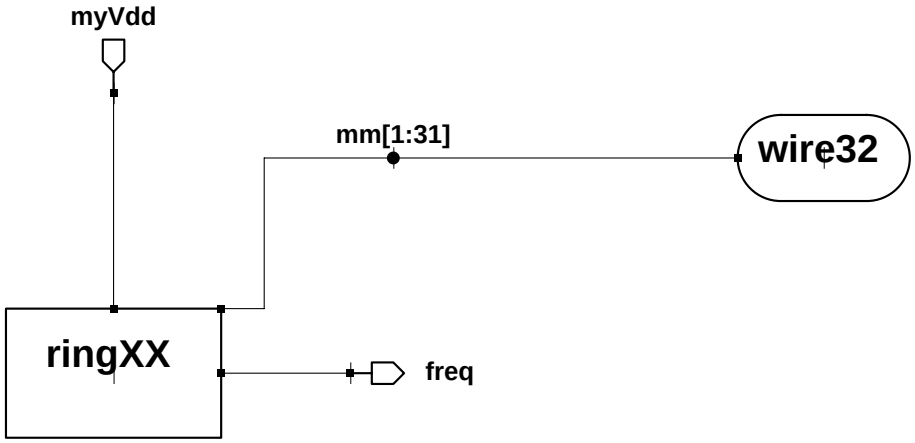
this has 100 micron metal wire loads with extra grounds



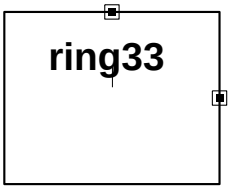
Sue 4.0	Cell: Version: %I% **ring31**	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/ring31.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



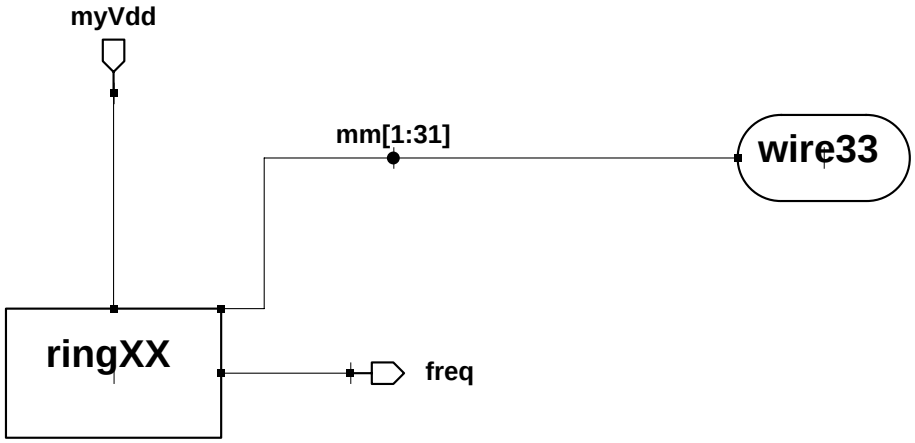
this has 100 micron metal wire loads with extra grounds



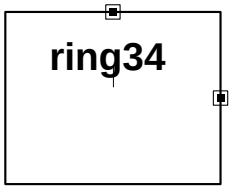
Sue 4.0	Cell: Version: %I% **ring32**	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/ring32.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



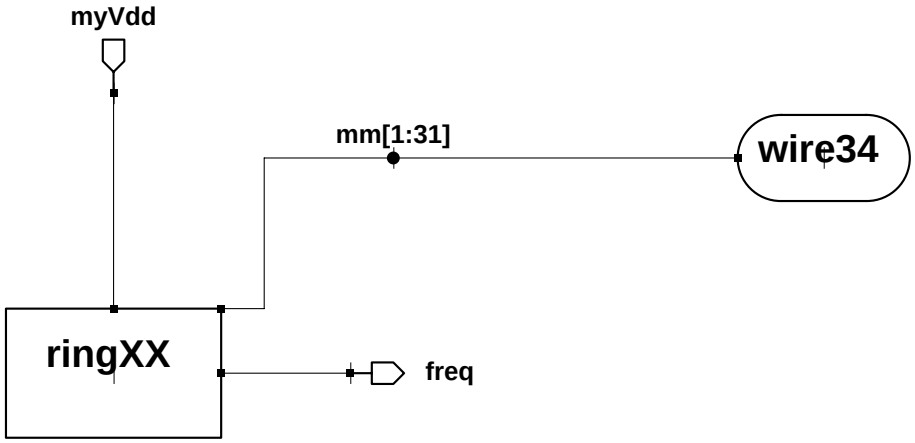
this has 100 micron metal wire loads with extra grounds



Sue 4.0	Cell: ring33 Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/ring33.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron metal wire loads with extra grounds



Sue 4.0	Cell: Version: %I% **ring34**	modified: Fri Jan 07 01:47:0p PST 2000
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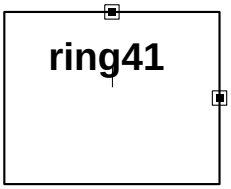
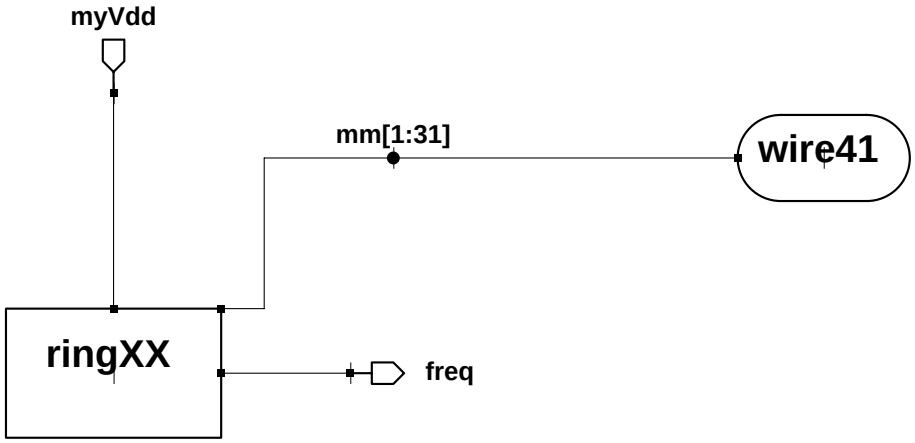
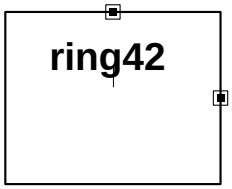
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



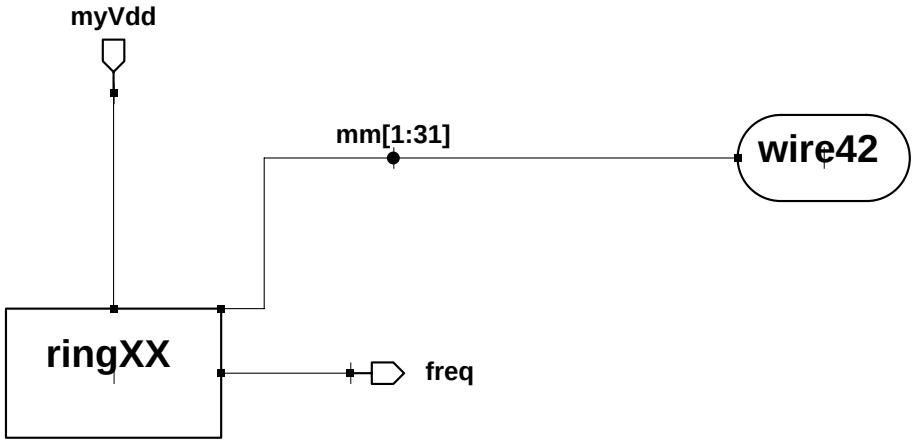
this has 100 micron metal wire loads with surround and cross



Sue 4.0	Cell: Version: %I% **ring41**	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/ring41.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron metal wire loads with surround and cross



Sue 4.0	Cell: Version: %I% **ring42**	modified: Fri Jan 07 01:47:0p PST 2000
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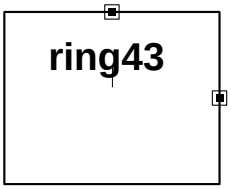
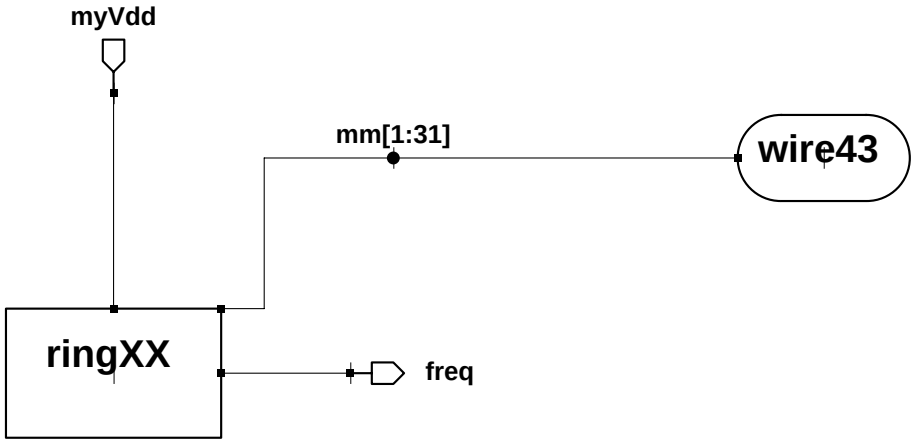
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron metal wire loads with surround and cross



Sue 4.0	Cell: Version: %I% **ring43**	modified: Fri Jan 07 01:47:0p PST 2000
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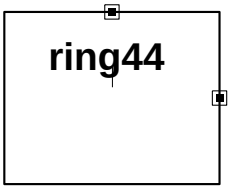
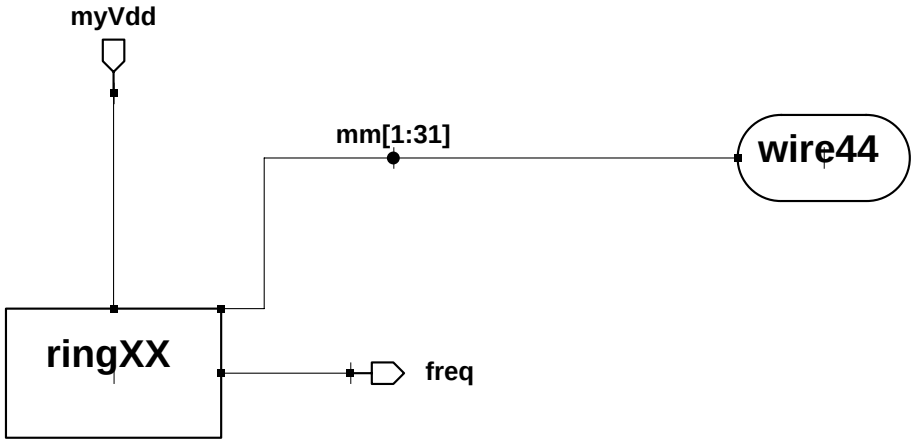
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron metal wire loads with surround and cross



Sue 4.0	Cell: Version: %I% **ring44**	modified: Fri Jan 07 01:47:0p PST 2000
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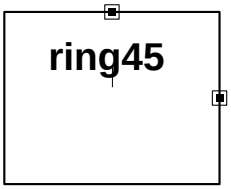
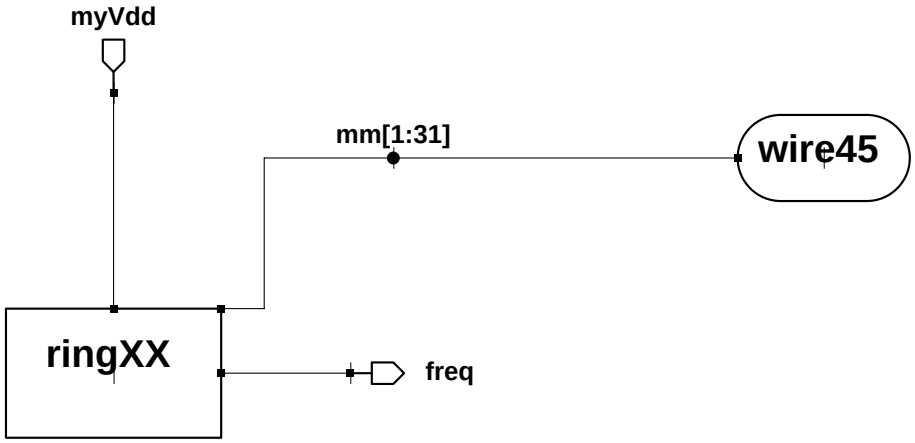
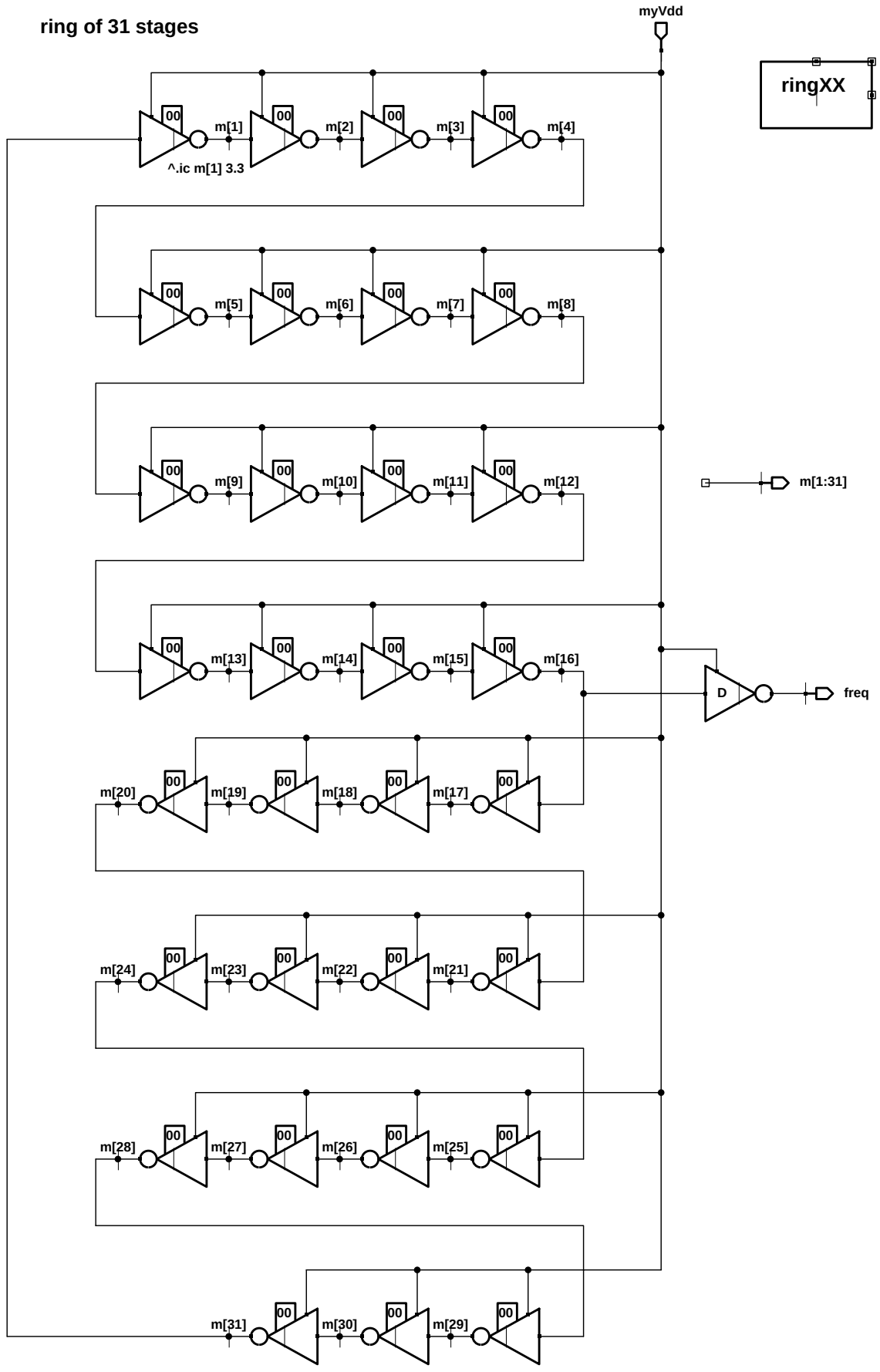
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



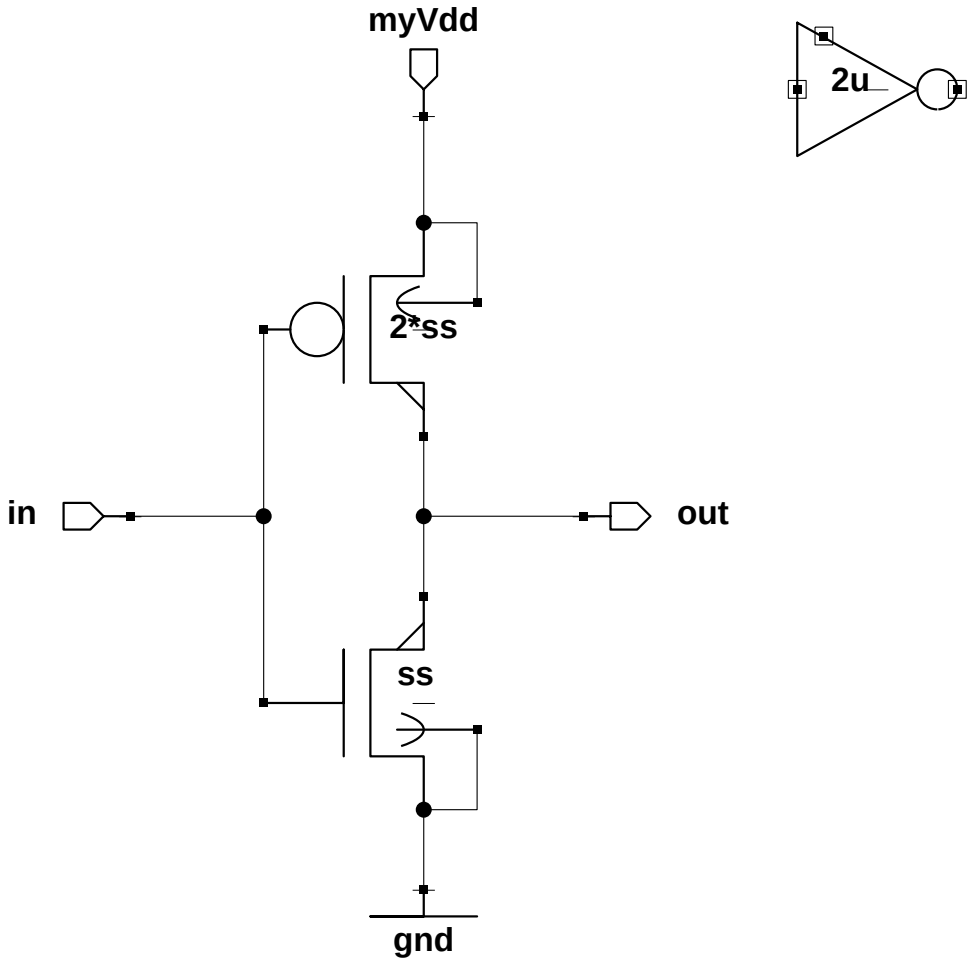
this has 100 micron metal wire loads with surround and cross



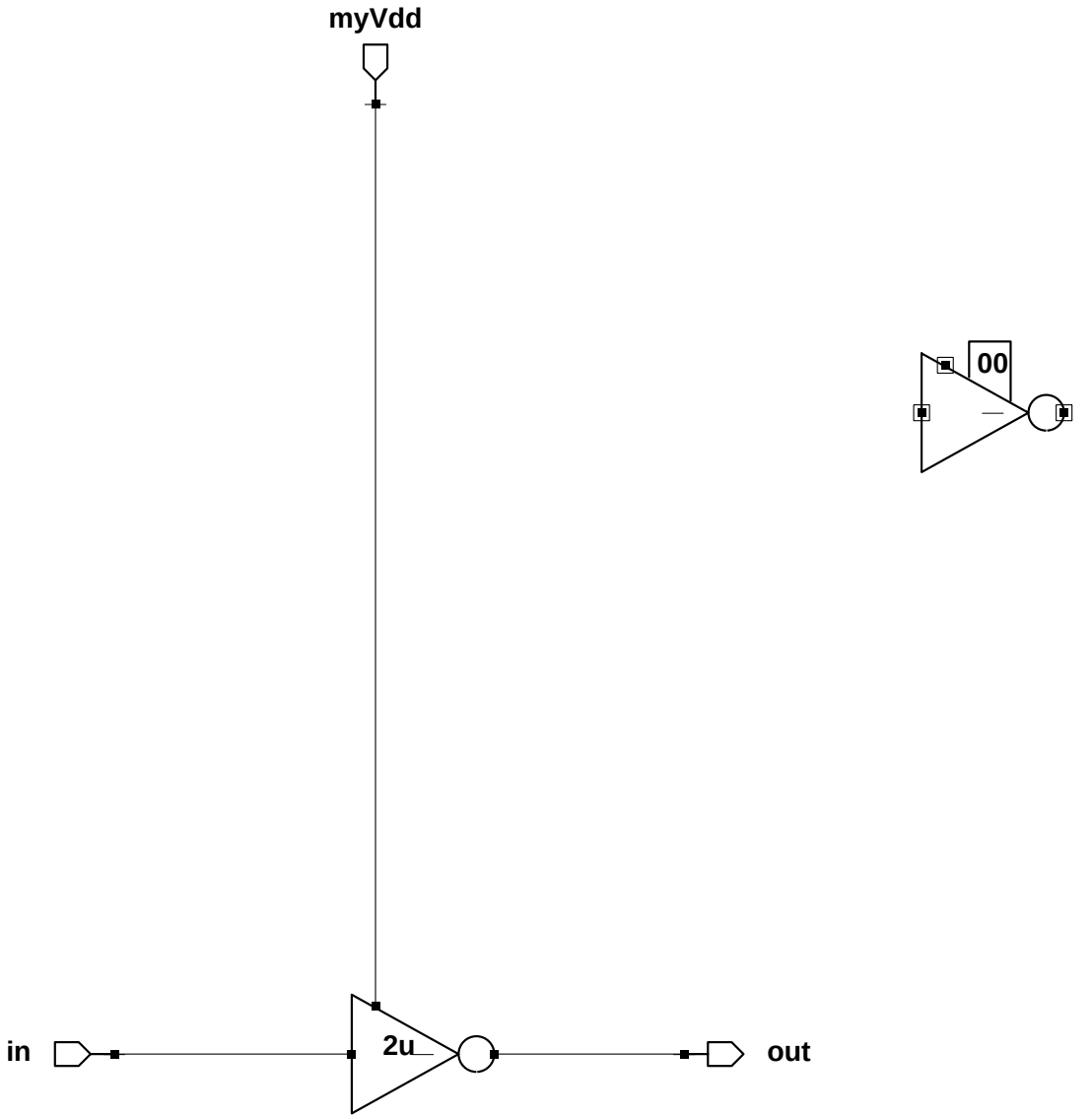
Sue 4.0	Cell: Version: %I% **ring45**	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/ring45.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



Sue 4.0	Cell: ringXX Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/ringXX.sue
title_sun_AP	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



Sue 4.0	Cell: **inv** Version: **%I%**	**modified: Fri Jan 07 01:47:0p PST 2000**
		file: /proj/async/db/2000/duchess_2000_0002/schematics/inv.sue
title_bar_sun	**owner: ivans**	**Sun Microsystems Inc. Proprietary and Confidential Information**



Sue 4.0	Cell: **inv00** Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
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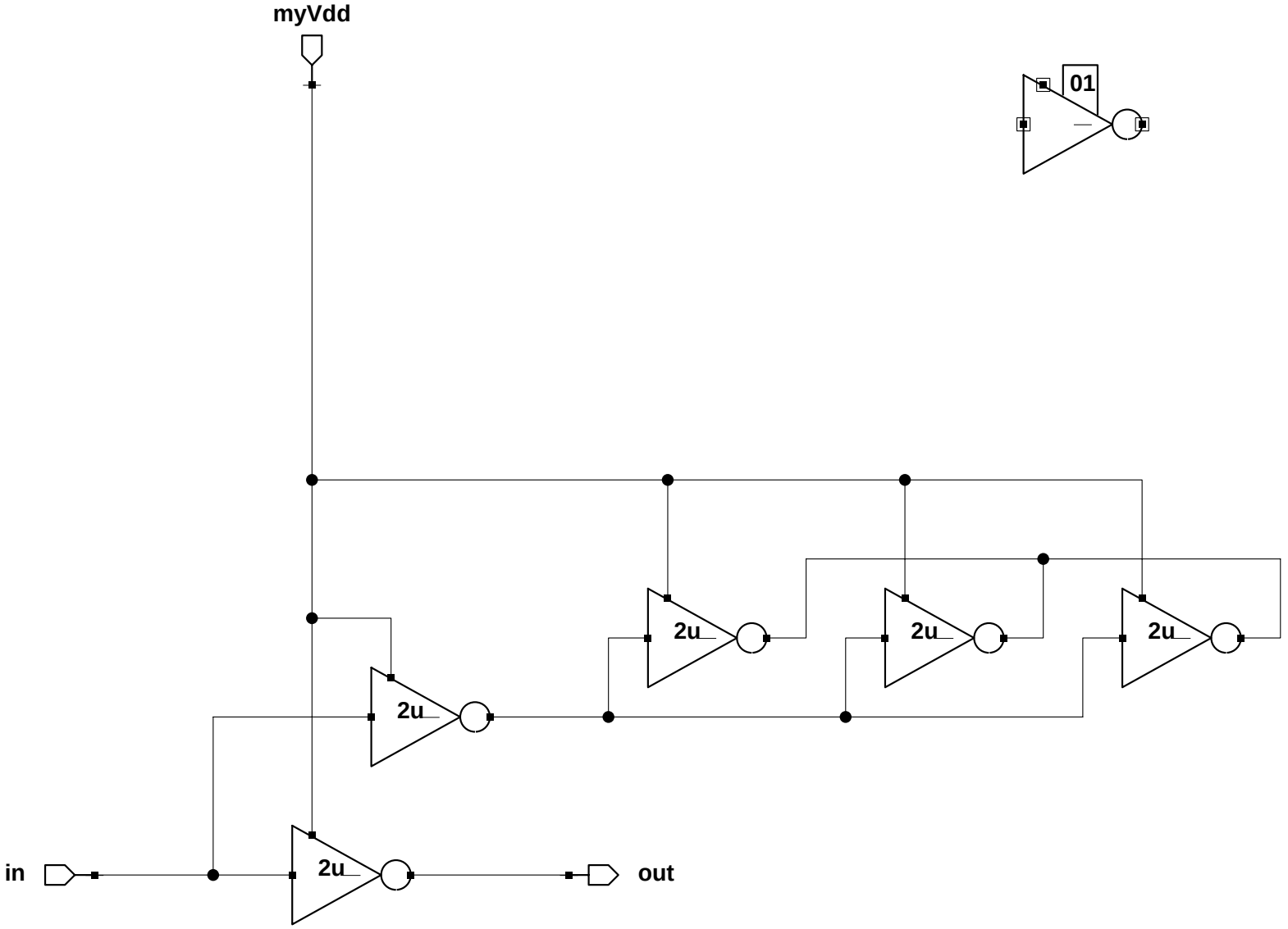
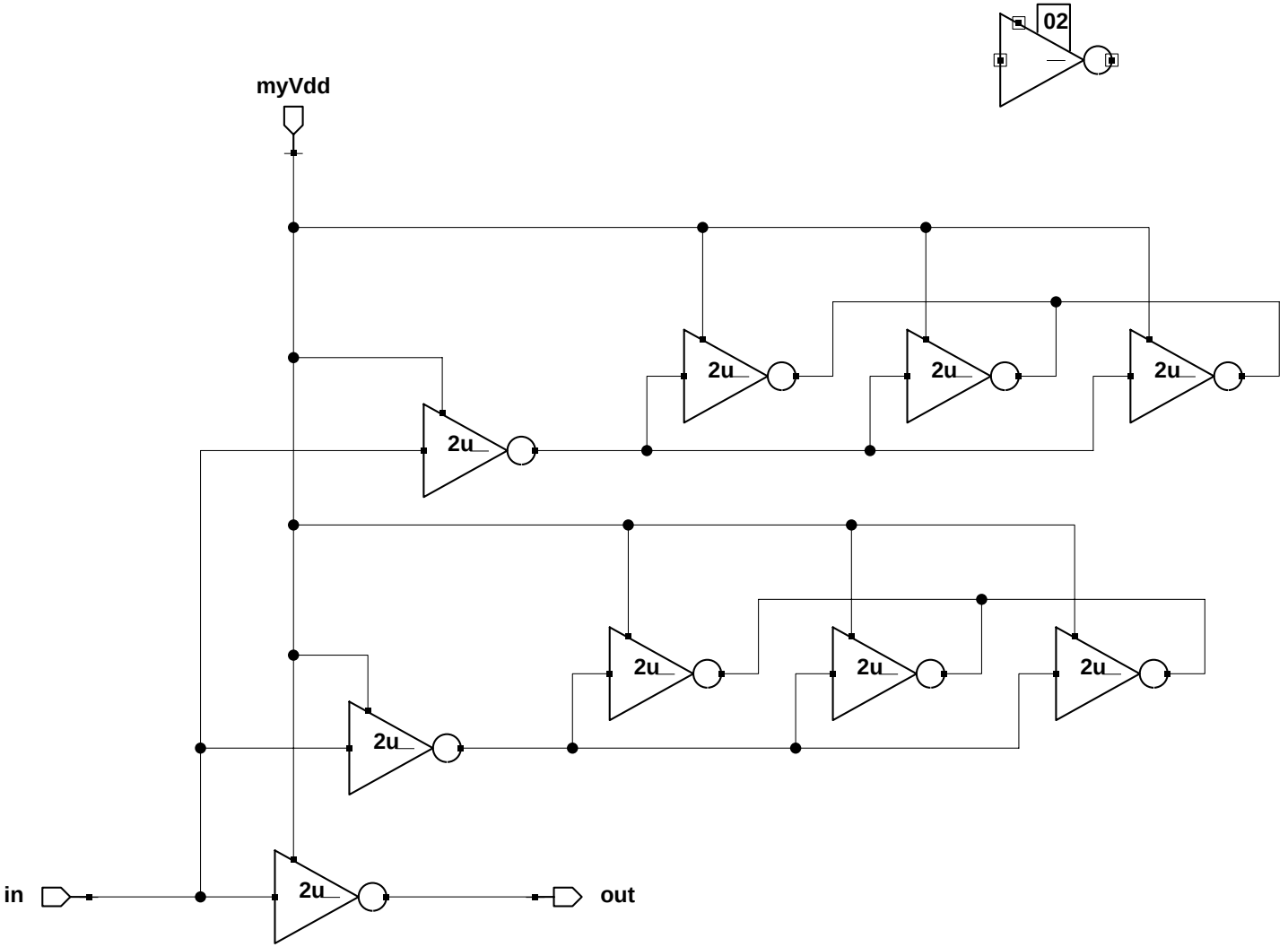
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



Sue 4.0	Cell: **inv01** Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/inv01.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



Sue 4.0	Cell: Version: %I% **inv02**	modified: Fri Jan 07 01:47:0p PST 2000
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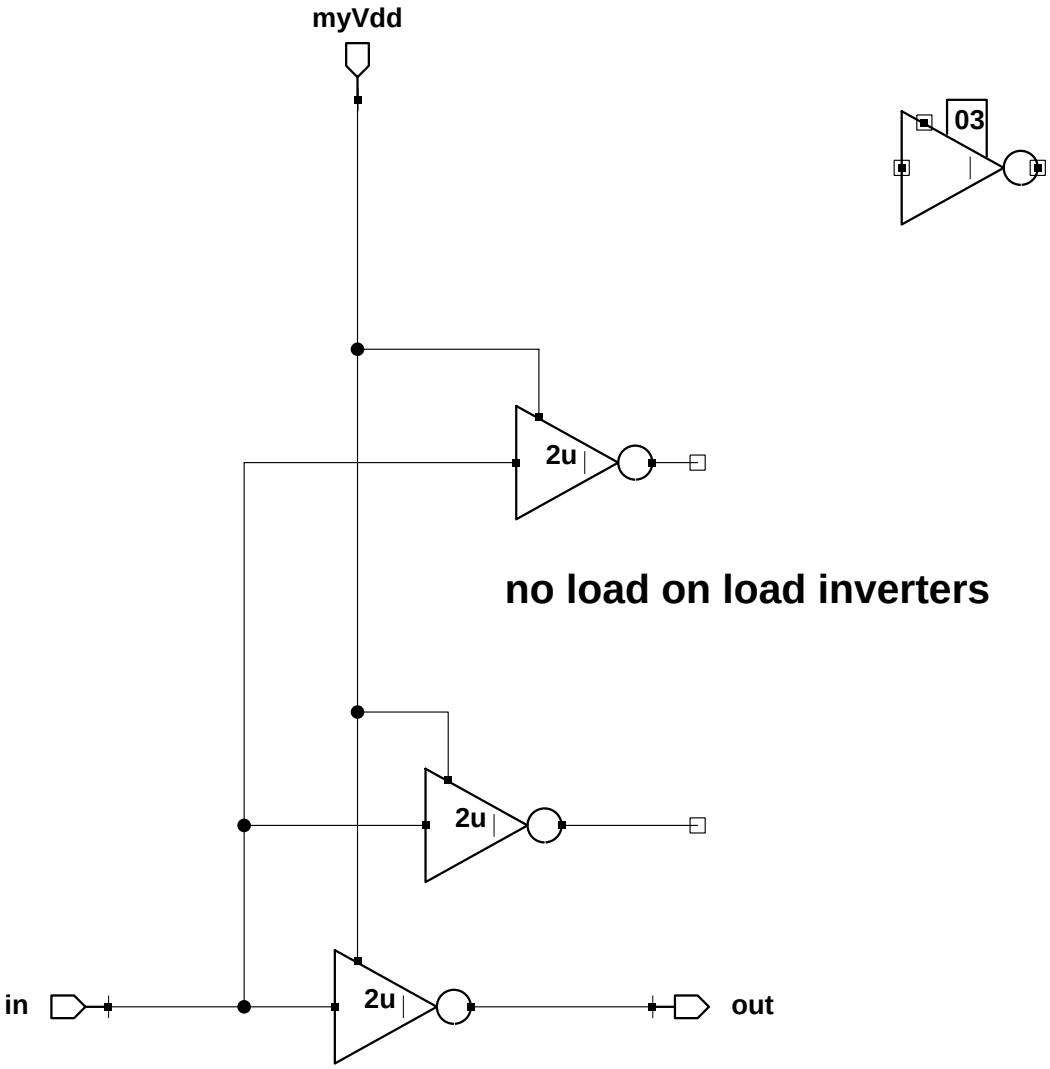
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



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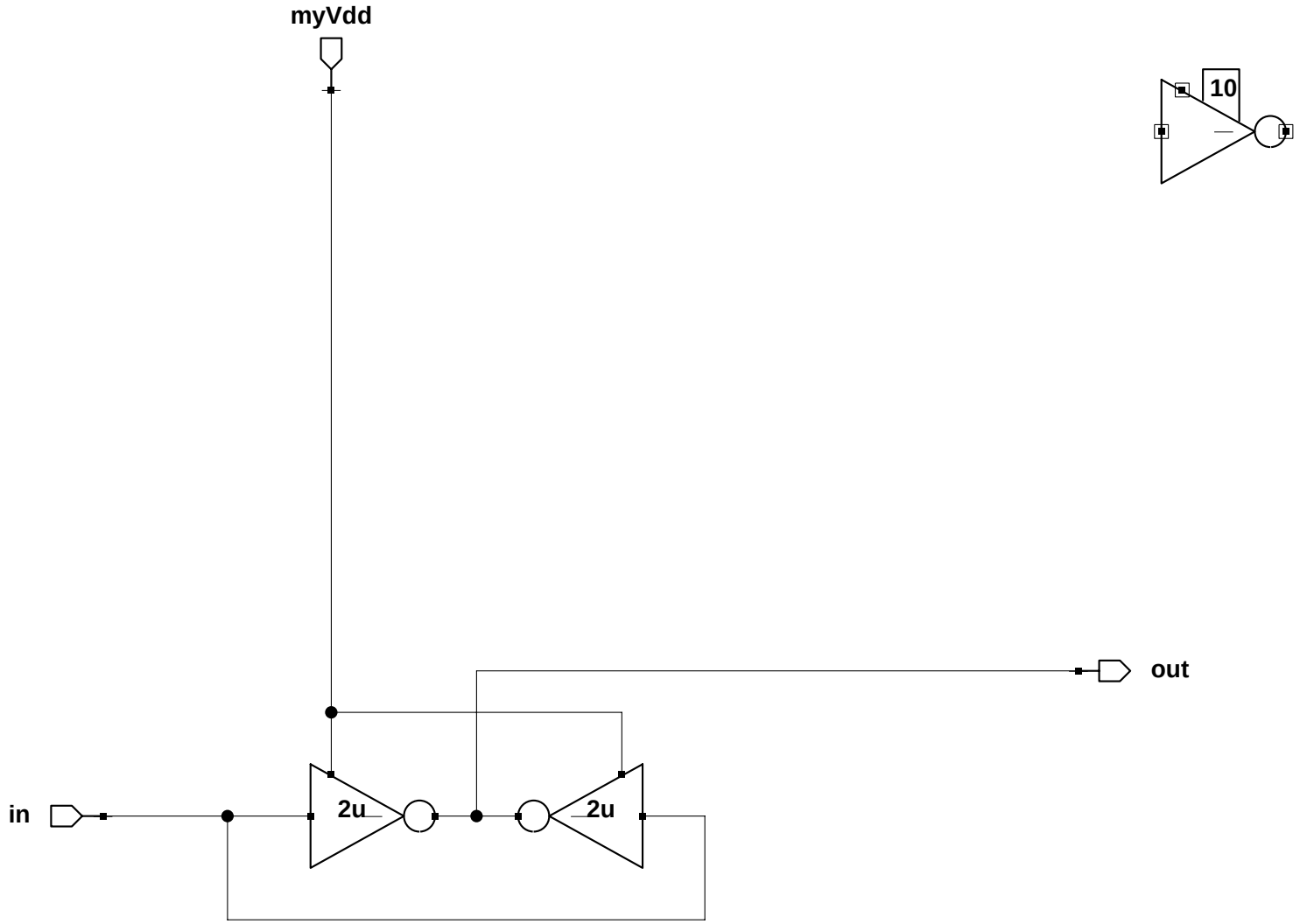
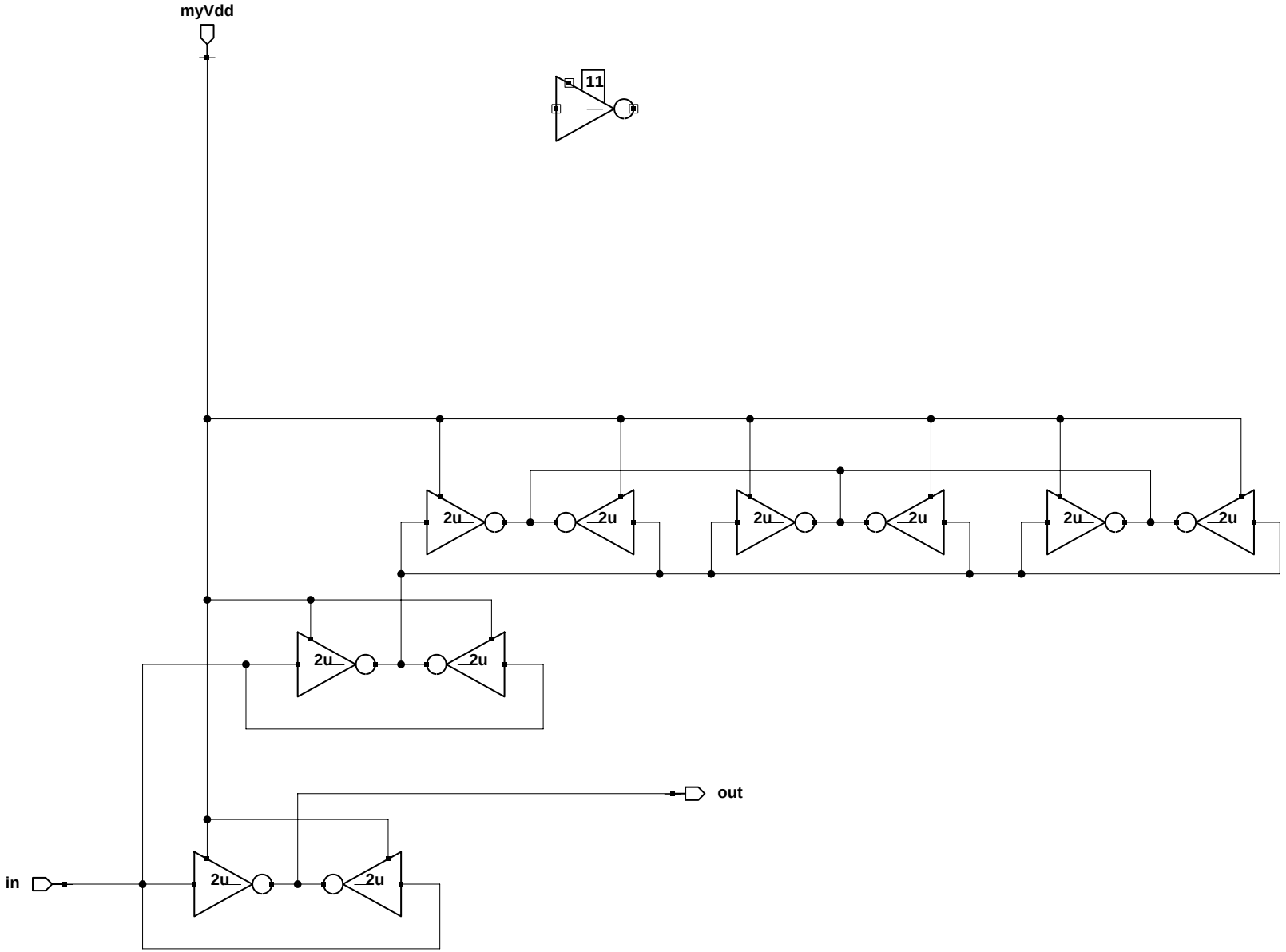
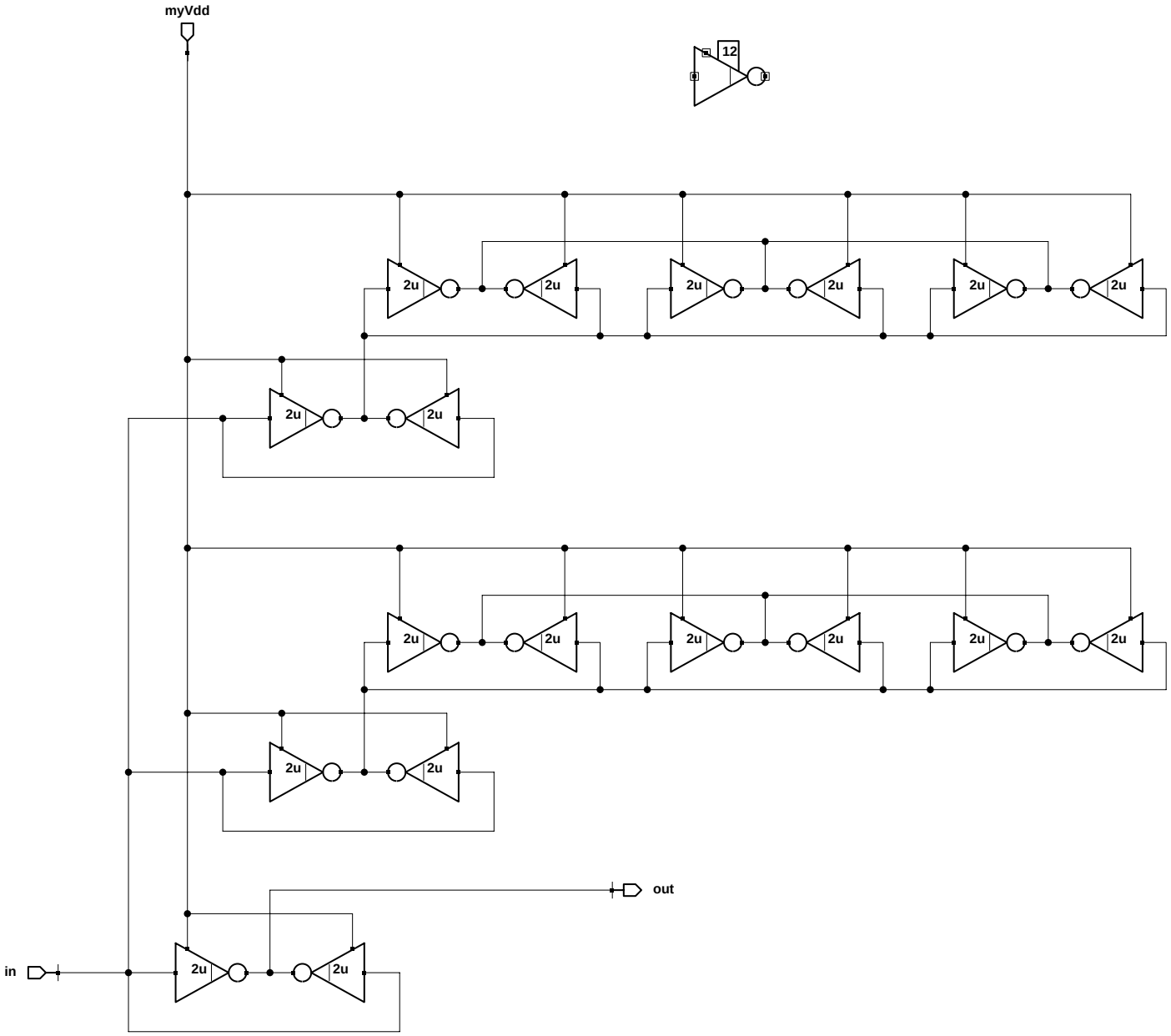
		file: /proj/async/db/2000/duchess_2000_0002/schematics/inv03.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



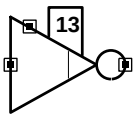
Sue 4.0	Cell: **inv10** Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/inv10.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

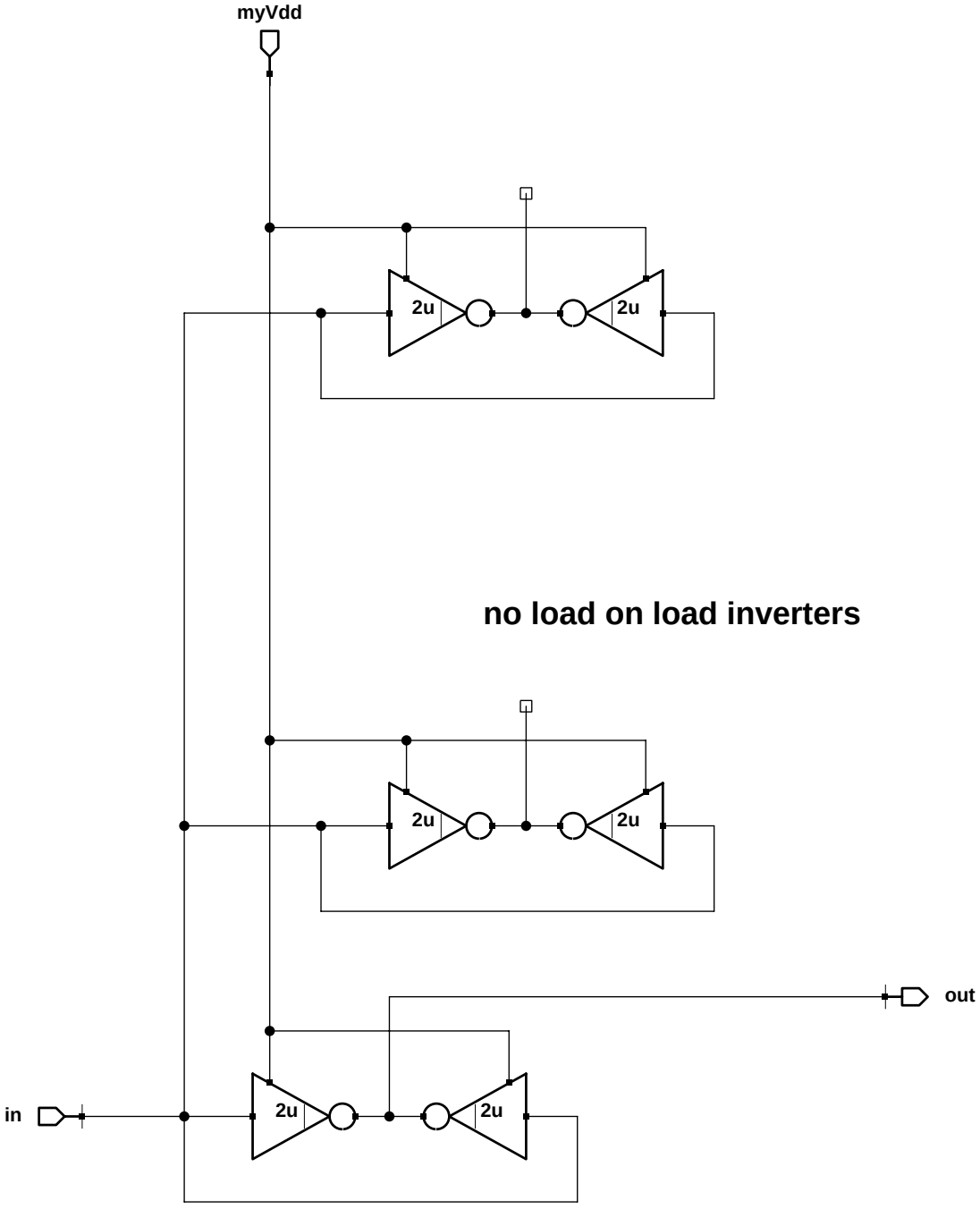


Sue 4.0	Cell: Version: %I% **inv11**	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/inv11.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



Sue 4.0	Cell: inv12 Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/inv12.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information





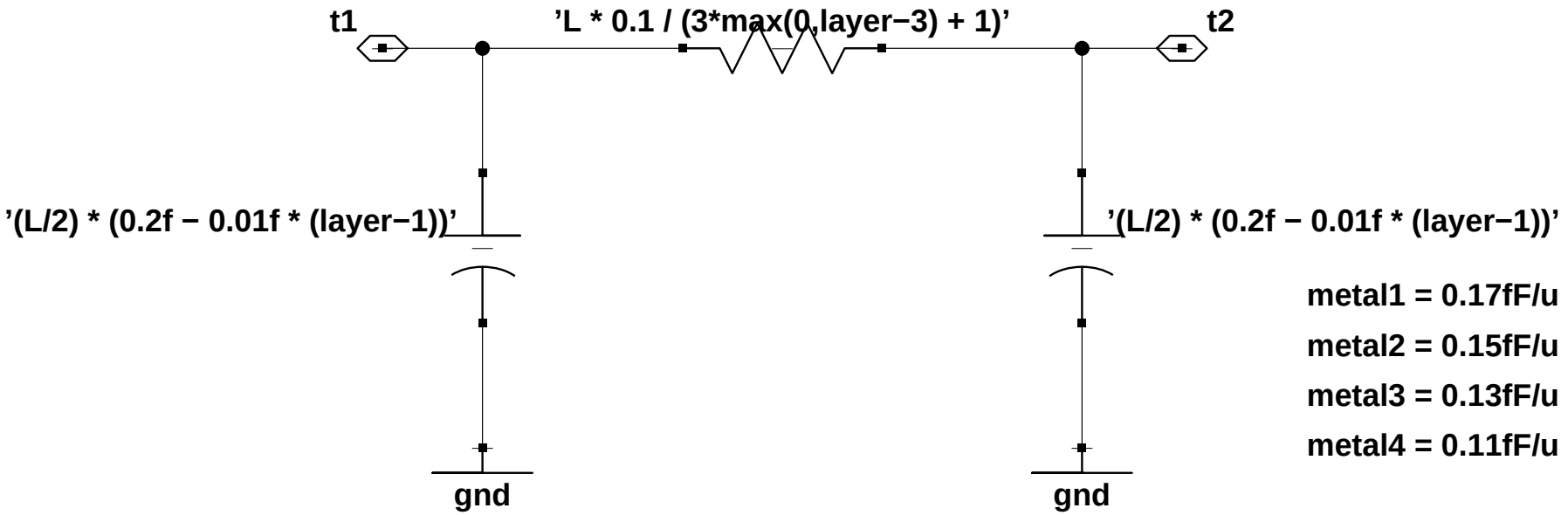
Sue 4.0	Cell: Version: %I% **inv13**	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/inv13.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

poly

100

paramaterized wire model for the HP GMOS10qa process

denominator is 1 for metal1,2,3 and 4 for metal4



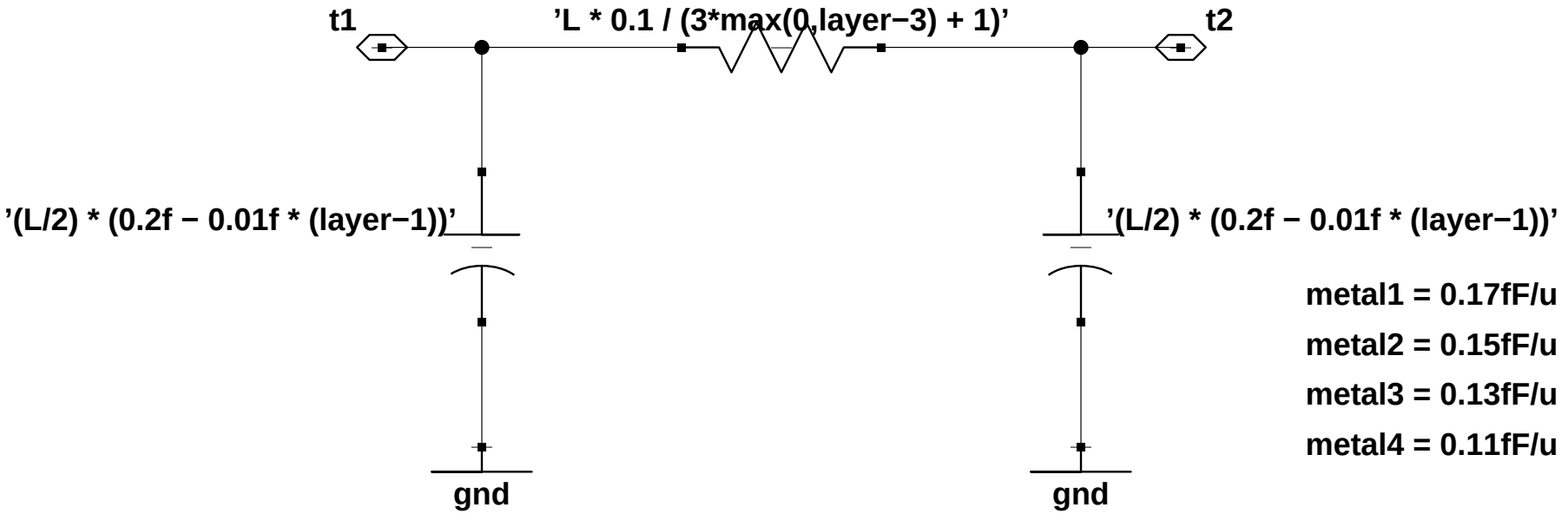
owner: Ian W. Jones	modified: Fri Jan 07 01:47:0p PST 2000
cell: polyWire	file: /proj/async/db/2000/duchess_2000_0002/schematics/polyWire.su

metal1

100

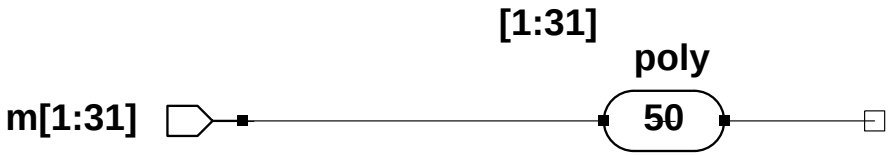
paramaterized wire model for the HP GMOS10qa process

denominator is 1 for metal1,2,3 and 4 for metal4



owner: Ian W. Jones	modified: Fri Jan 07 01:47:0p PST 2000
cell: wire	file: /proj/async/db/2000/duchess_2000_0002/schematics/wire.sue

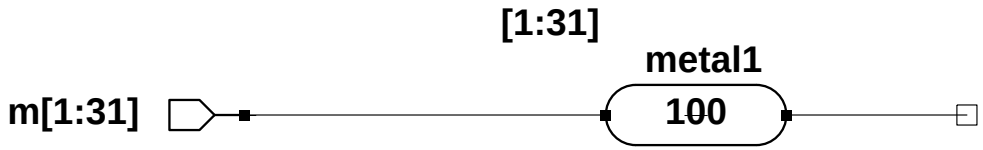
there are 31 pieces of poly wire each 50 microns long



this is poly, in spite of saying metal1

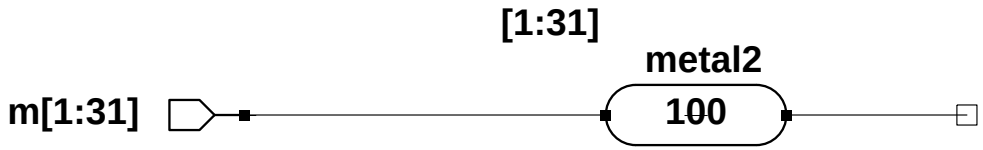
Sue 4.0	Cell: wire0 Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/wire0.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long



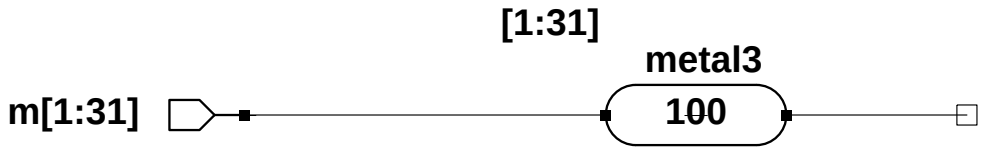
Sue 4.0	Cell: wire21 Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/wire21.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long



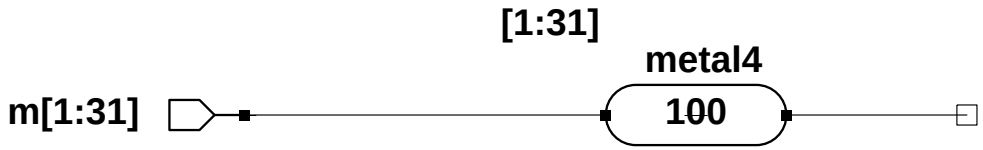
Sue 4.0	Cell: Version: %I% **wire22**	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/wire22.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long



Sue 4.0	Cell: wire23 Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/wire23.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

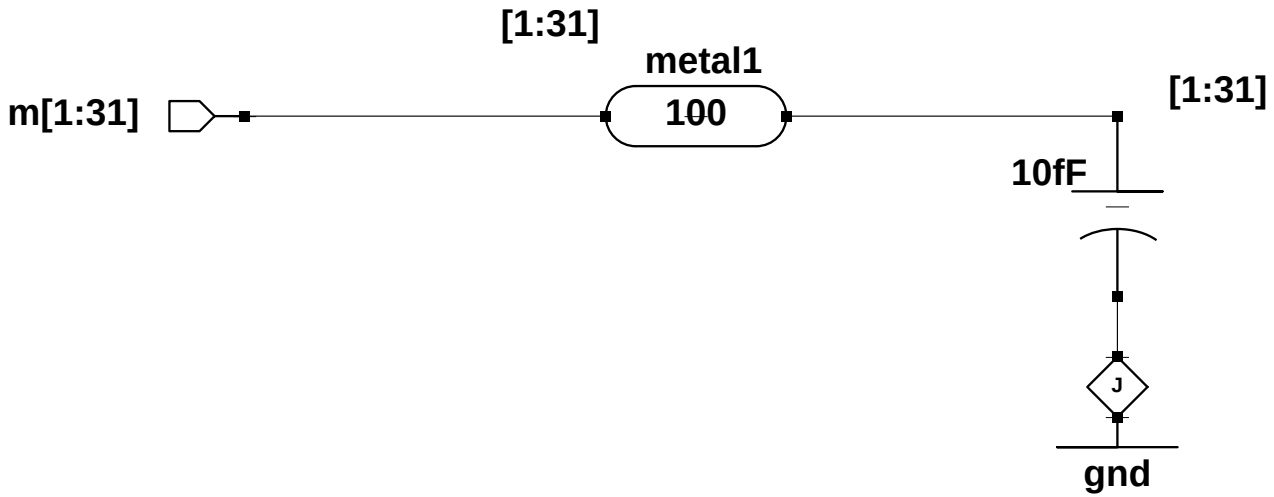
there are 31 pieces of wire each 100 microns long



Sue 4.0	Cell: wire24 Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/wire24.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

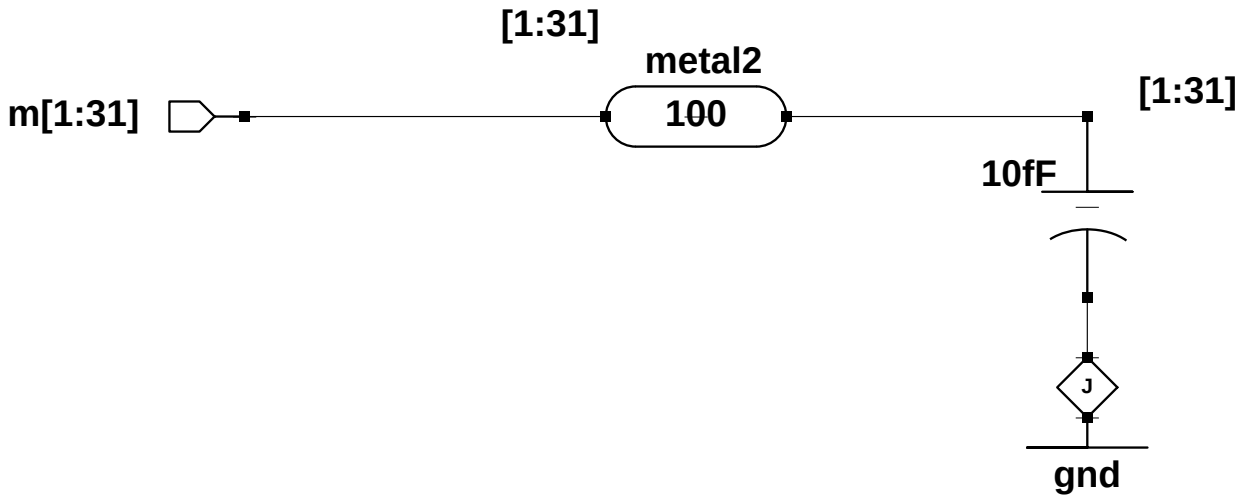
each is flanked by matching wire on both sides



Sue 4.0	Cell: Version: %I% **wire31**	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/wire31.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

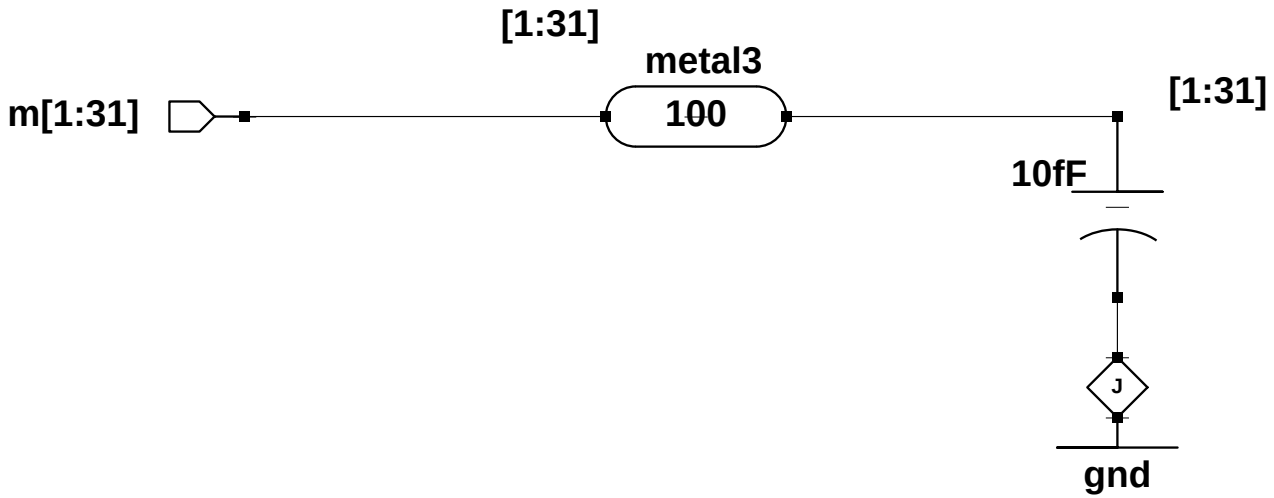
each is flanked by matching wire on both sides



Sue 4.0	Cell: wire32 Version: %I%	modified: Fri Jan 07 01:47:0p PST 2000
		file: /proj/async/db/2000/duchess_2000_0002/schematics/wire32.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides



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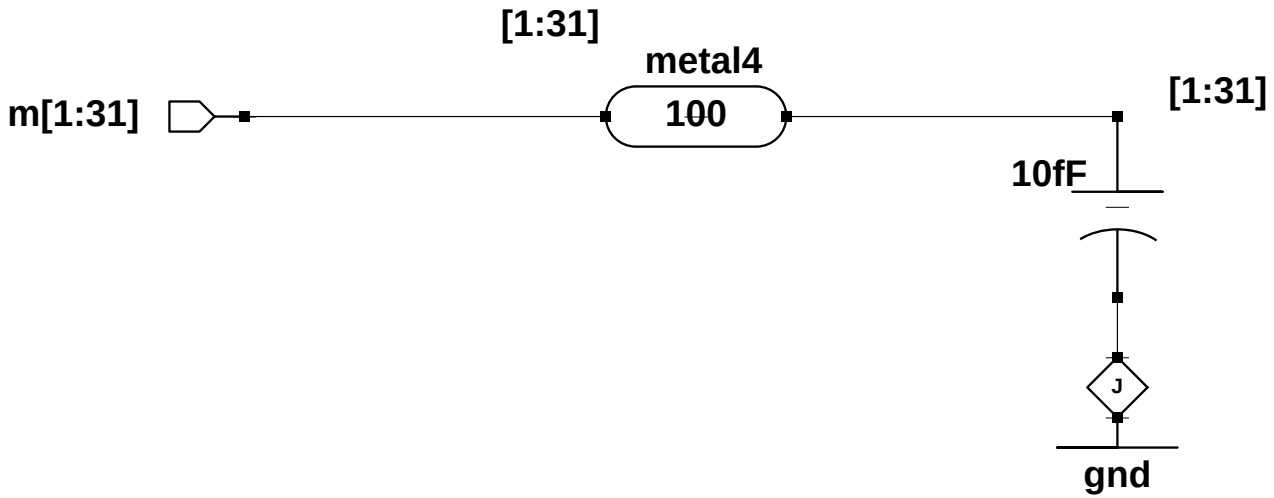
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides



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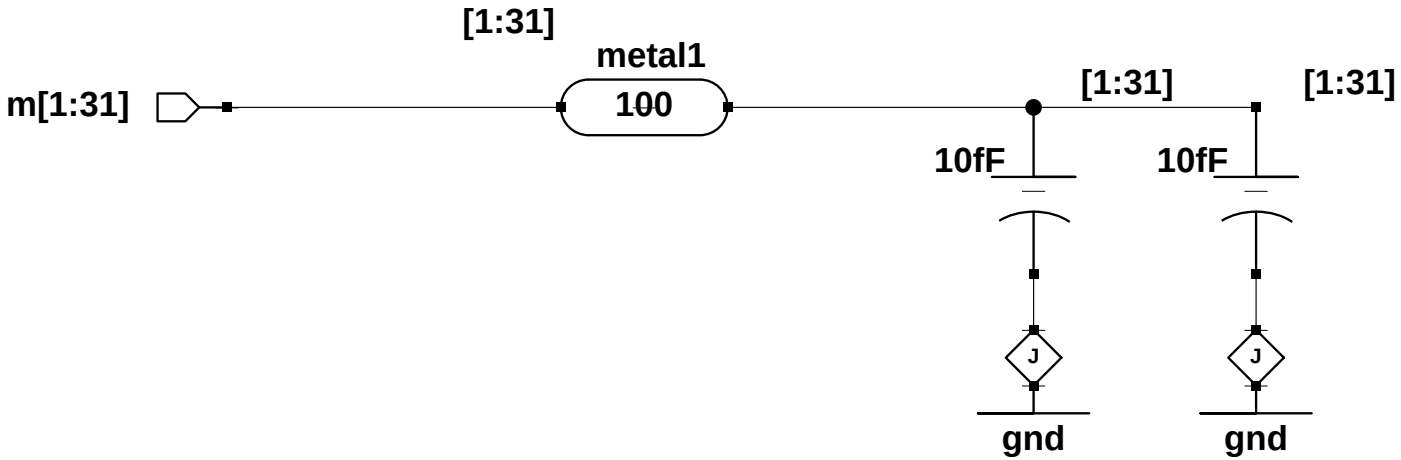
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



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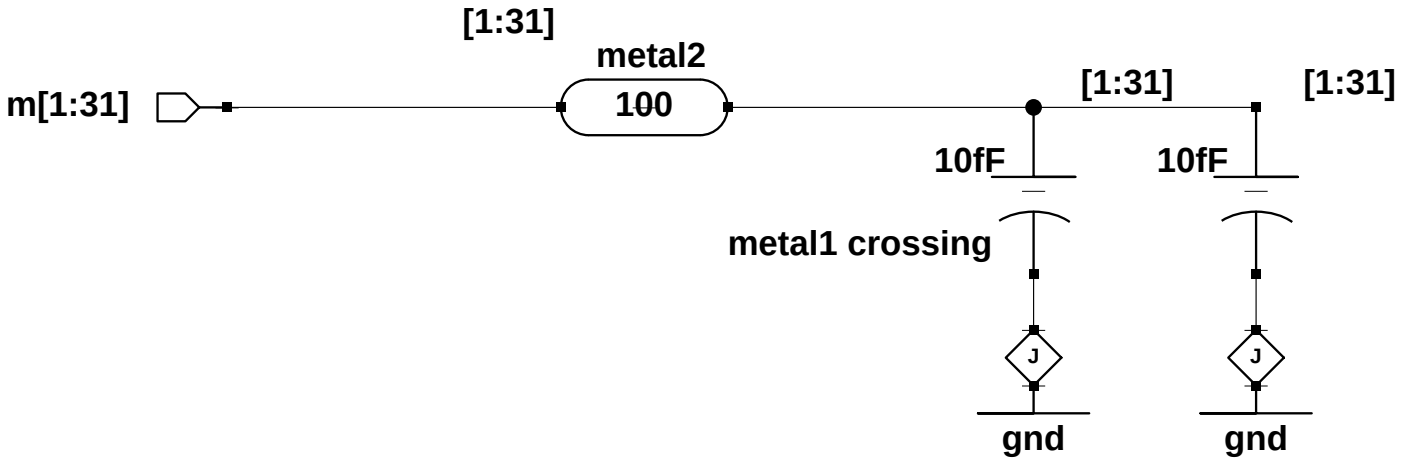
there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



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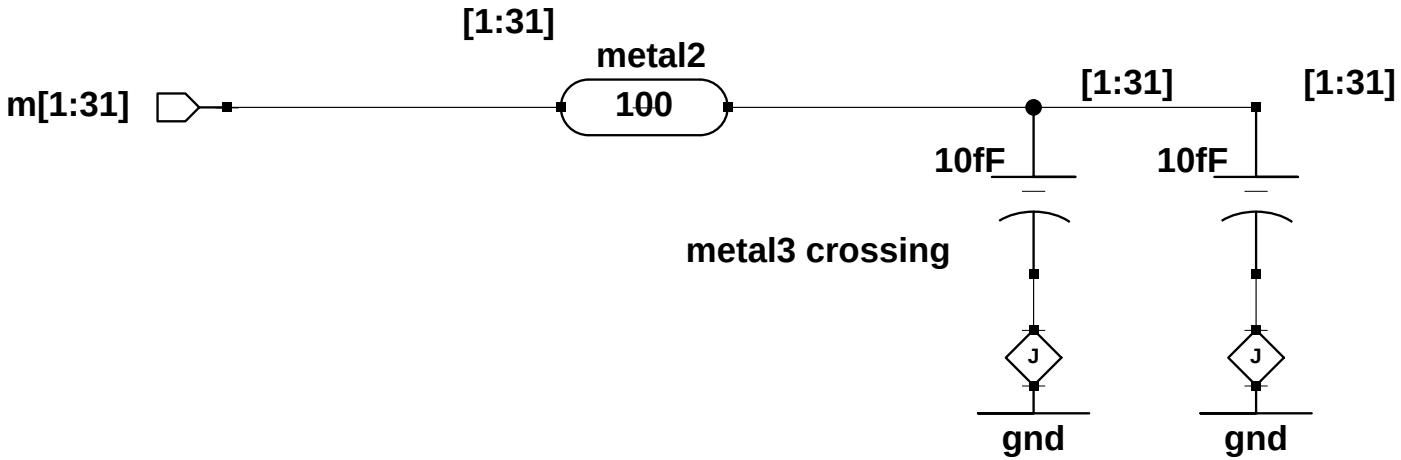
there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



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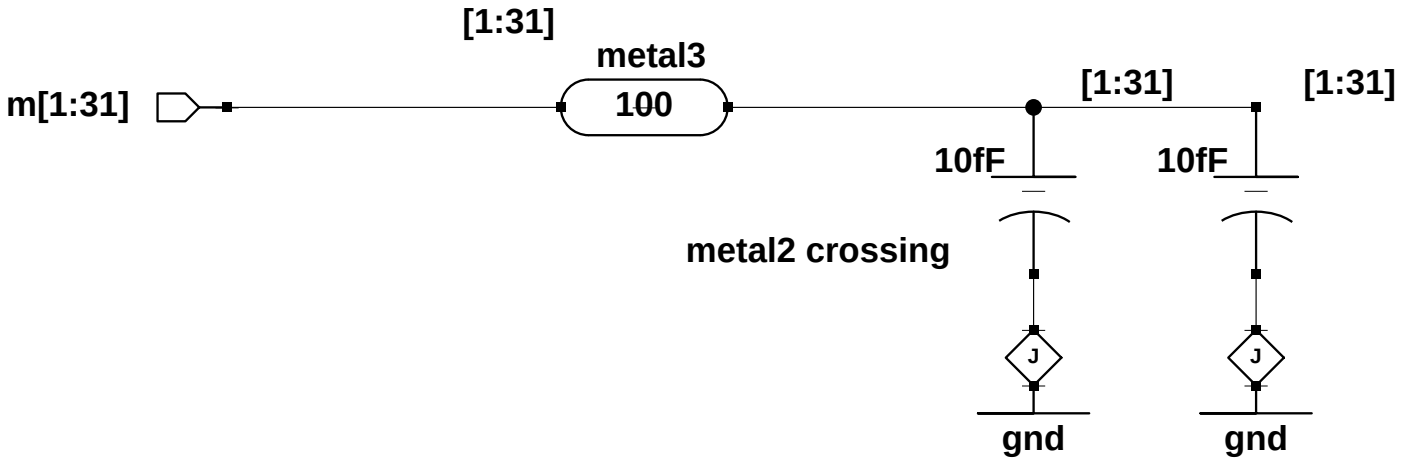
there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



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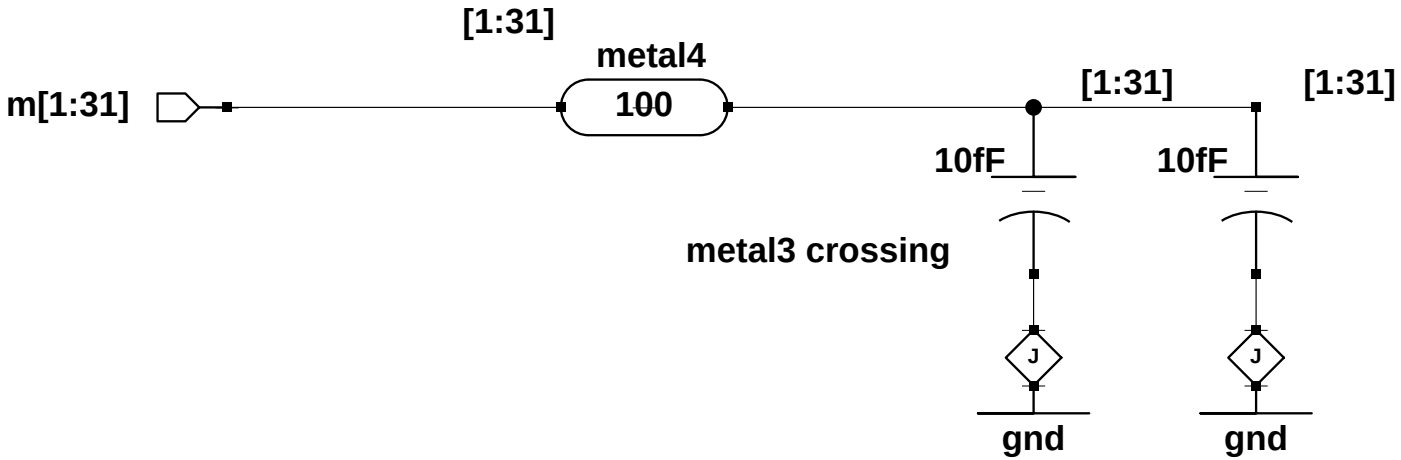
there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



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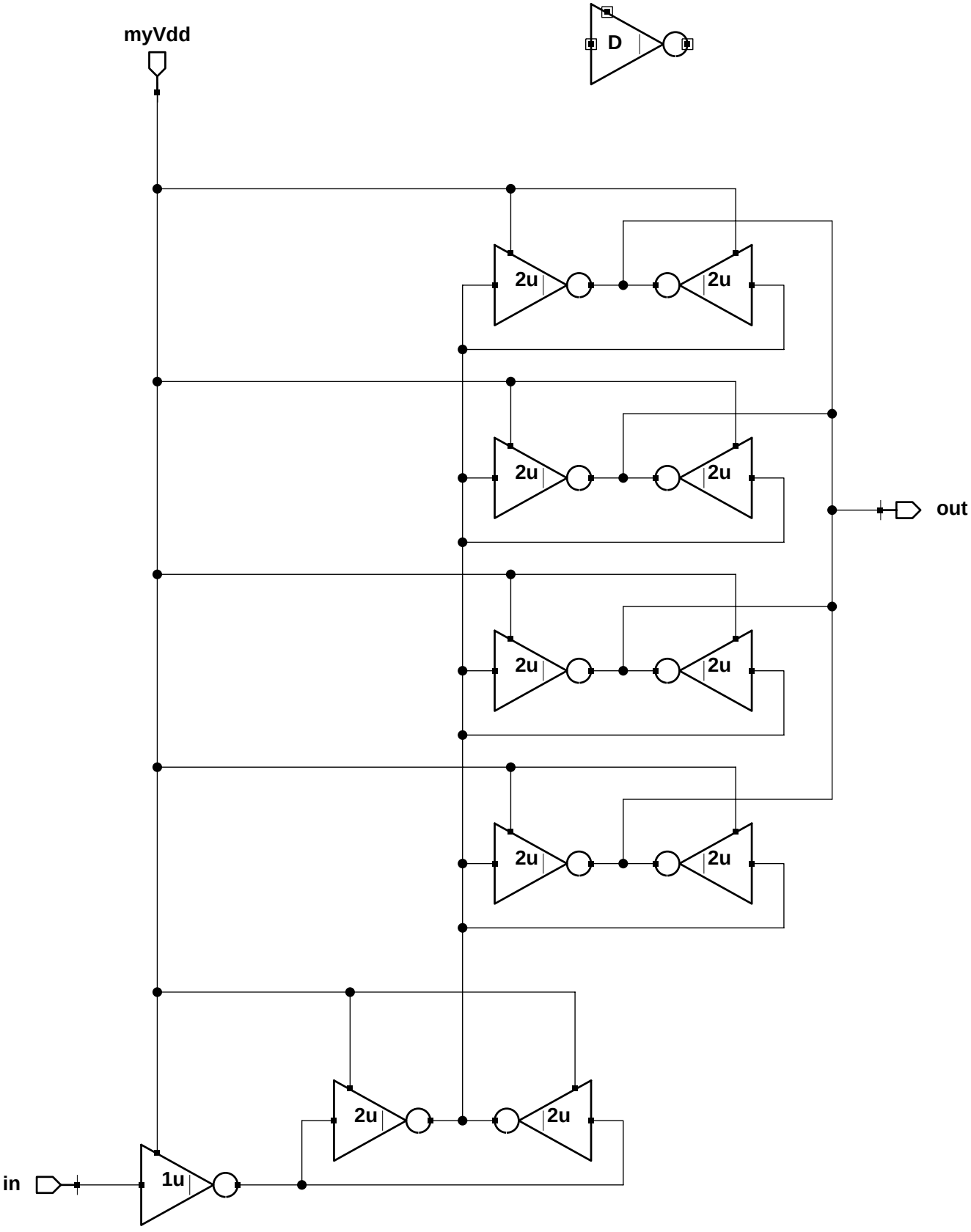

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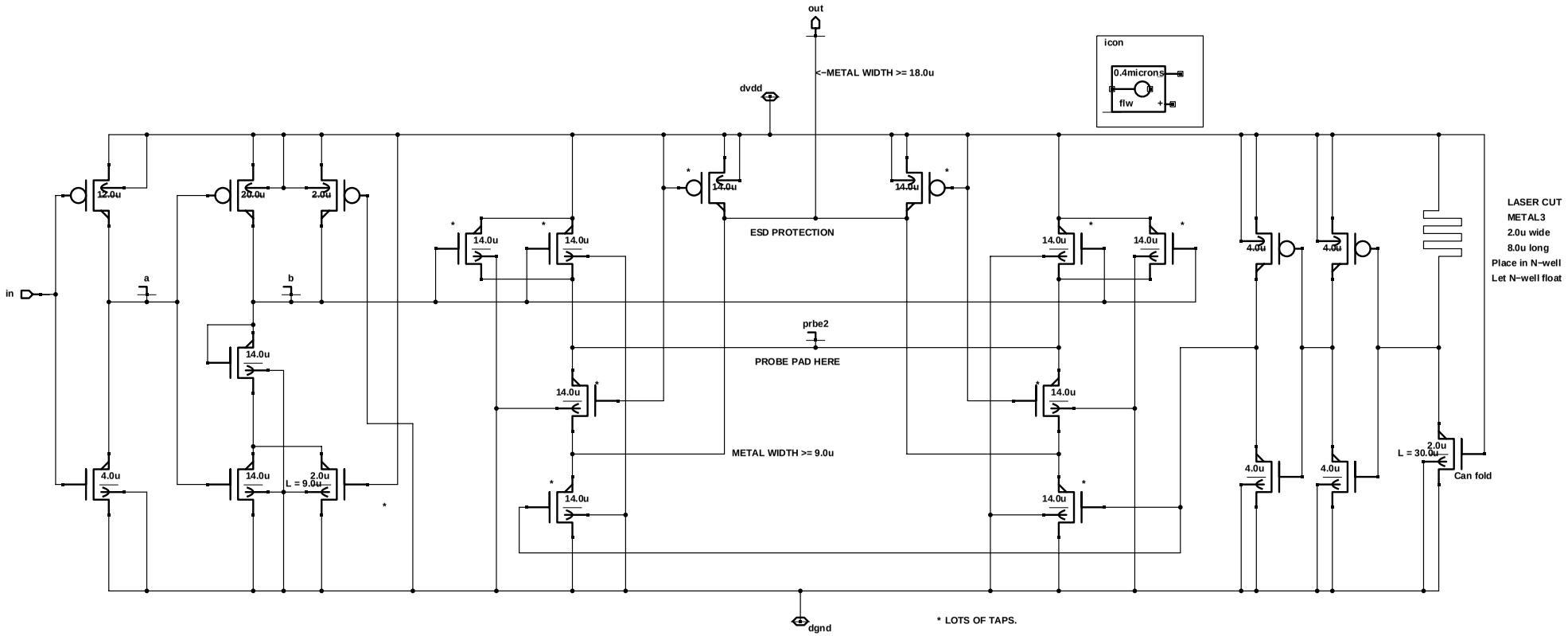
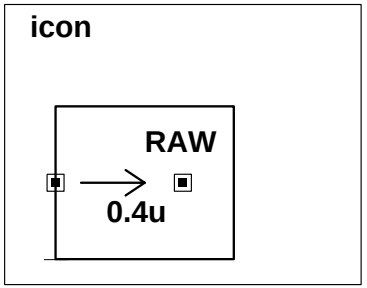


SUE

owner: boz modified: Fri Jan 07 01:47:0p PST 2000

cell: pad_flwout file: /proj/async/db/2000/duchess_2000_0002/schematics/suelib_pads/pad_flwout.sue



SUE

owner: coates modified: Fri Jan 07 01:47:0p PST 2000

cell: pad_raw file: /proj/async/db/2000/duchess_2000_0002/schematics/suelib_pads/pad_raw.sue

Appendix B

Schematics

2000−0278 Schematics for the DuchessII Test Chip
Gainsley, 14 June 2000

Sun Microsystems Laboratories

Subject: **Schematics for the DuchessII Test Chip**
Date: **14 June 2000**
From: **Jonathan Gainsley**
Sun Lab#: **2000-0278**

References:

[1] SML #2000-0247: “The DuchessII Chip (CHIP),” *Gainsley*, 7 June 2000
[2] SML #2000-0262: “Rings for the DuchessII Chip,” *Lexau*, *Gainsley*, 6 June 2000

Introduction

This memo archives the Sue4 schematics for the DuchessII chip [1] which was submitted to MOSIS on 12 June 2000 for the 0.35u TSMC process. For a description of the chip, refer to [2].

Organization

The schematics are organized alphabetically, due to the script that imported all of the postscript files into this document. However, because of similar naming conventions, they ended up being organized somewhat loosely by groups. The top level schematics come first, followed by the various inverter schematics, and then schematics for the 8-way OR. The ring schematics come next, followed by the wire model schematics.

Top level - pages 4-6

DuchessII
ringGuts
ringGuts_Icon

Inverters - pages 7-17

driver	inv	inv00	inv01	inv02
inv03	inv10	inv10_1	inv11	inv12
inv13				

8-way OR - pages 18-20

or8	orGate	orLoad

Poly load - page 21

polyWire

Rings - pages 22-53

ring00	ring01	ring02	ring03
ring10	ring10_1	ring11	ring12
ring13	ring14	ring15	ring16
ring20	ring21	ring22	ring23
ring24	ring30	ring31	ring32
ring33	ring34	ring35	ring36
ring37	ring41	ring42	ring44
ring45	ring46	ringXX	

Wire - pages 54-68

wire	wire0	wire21	wire22
wire23	wire24	wire31	wire32
wire33	wire34	wire41	wire42
wire43	wire44	wire45	

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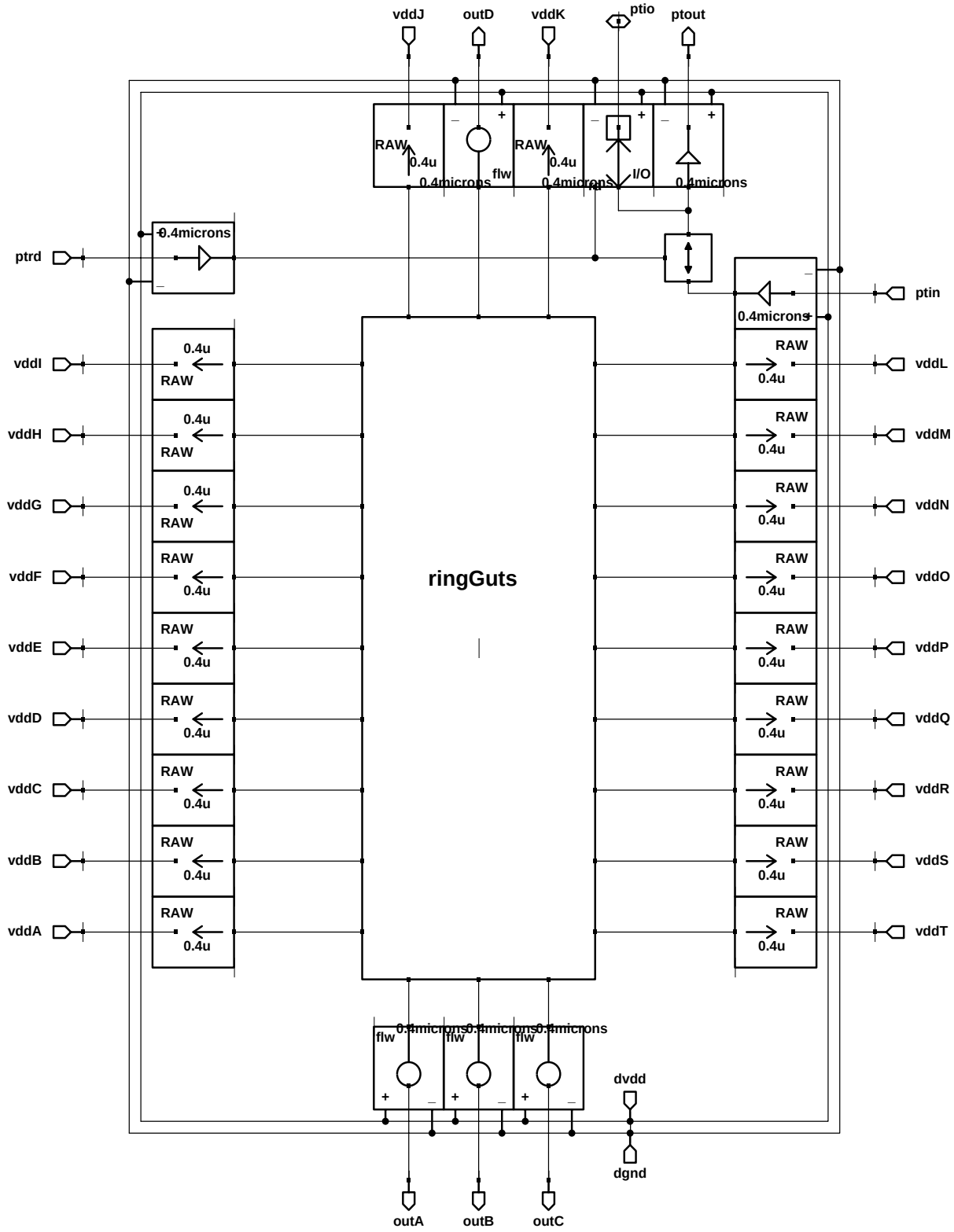

Sue 4.0	Cell: DuchessII Version: %I%	modified: Thu May 25 03:14:0p PDT 2000
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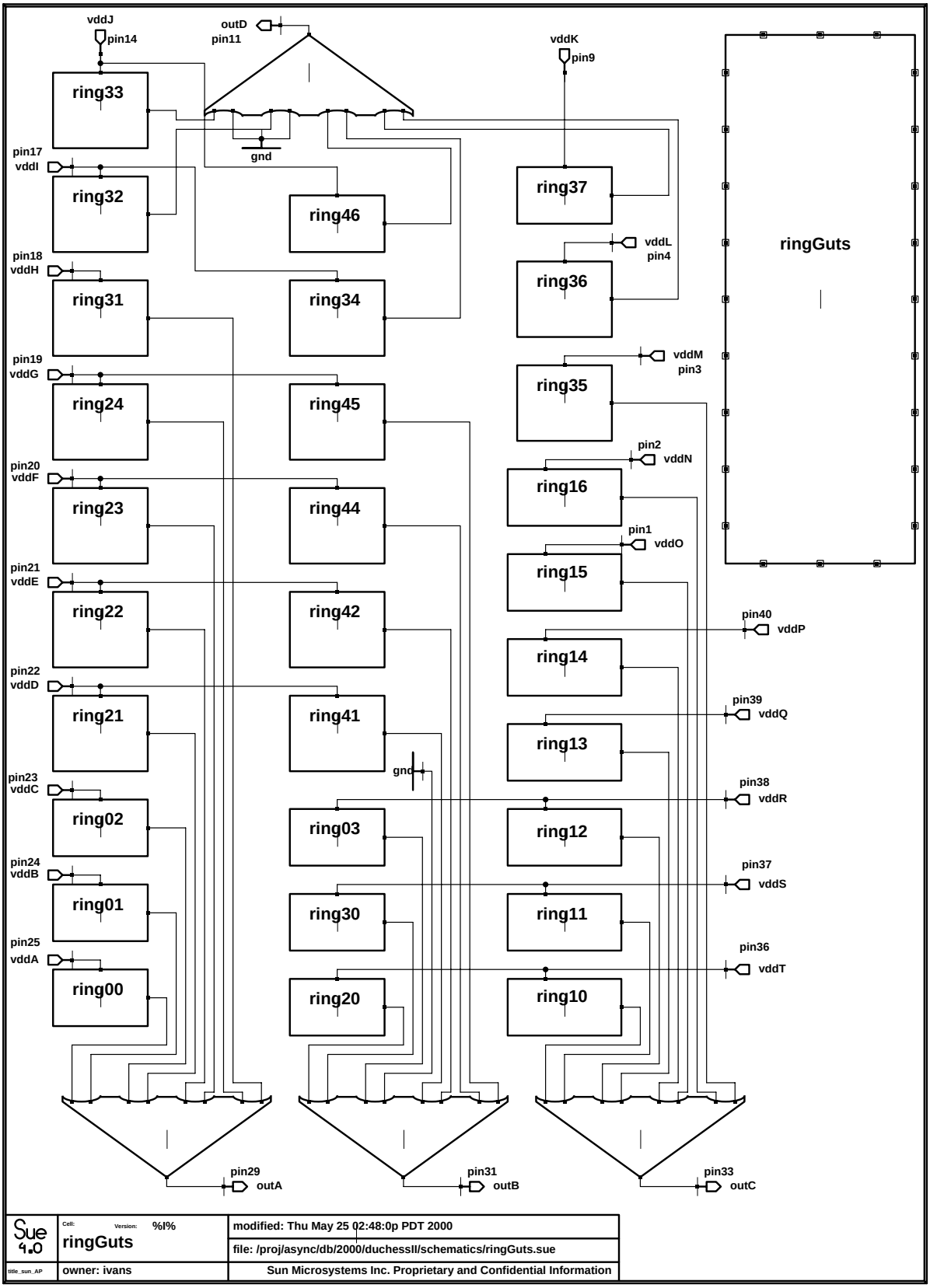
vddJ
pin14
outD
pin11
vddK
pin9
ring33
gnd
pin17
vddI
ring32
ring46
ring37
vddL
pin4
ringGuts
pin18
vddH
ring31
ring34
ring36
vddM
pin3
pin19
vddG
ring24
ring45
ring35
pin2
vddN
pin20
vddF
ring23
ring44
ring16
pin1
vddO
pin21
vddE
ring22
ring42
ring15
pin40
vddP
pin22
vddD
ring21
ring41
ring14
pin39
vddQ
gnd
ring13
pin23
vddC
ring02
ring03
ring12
pin38
vddR
pin24
vddB
ring01
ring30
ring11
pin37
vddS
pin25
vddA
ring00
ring20
ring10
pin36
vddT
pin29
outA
pin31
outB
pin33
outC
Sue 4.0
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ringGuts
Version:
%I%
modified: Thu May 25 02:48:0p PDT 2000
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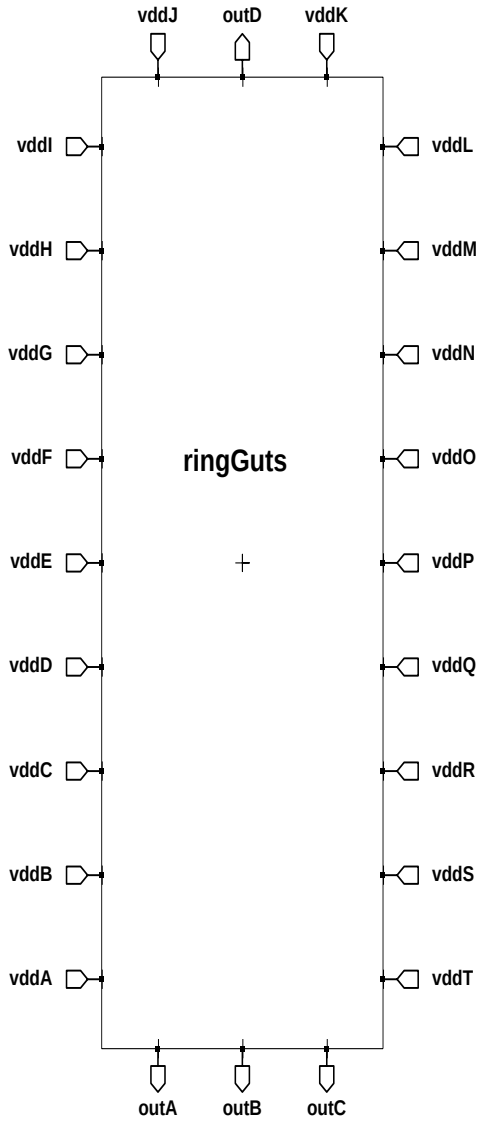
owner: ivans
Sun Microsystems Inc. Proprietary and Confidential Information



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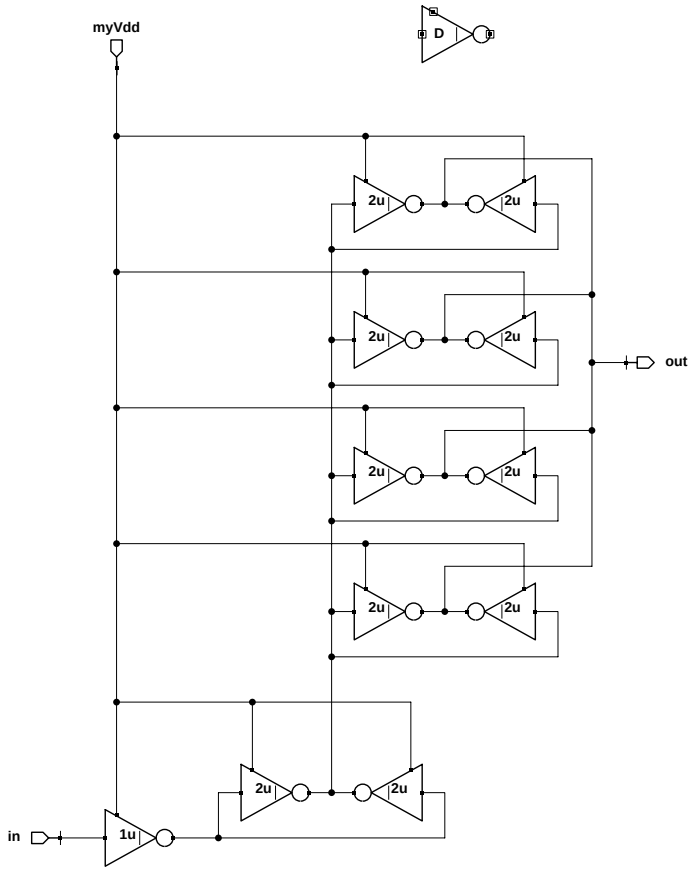

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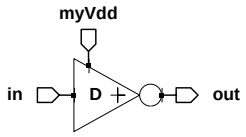

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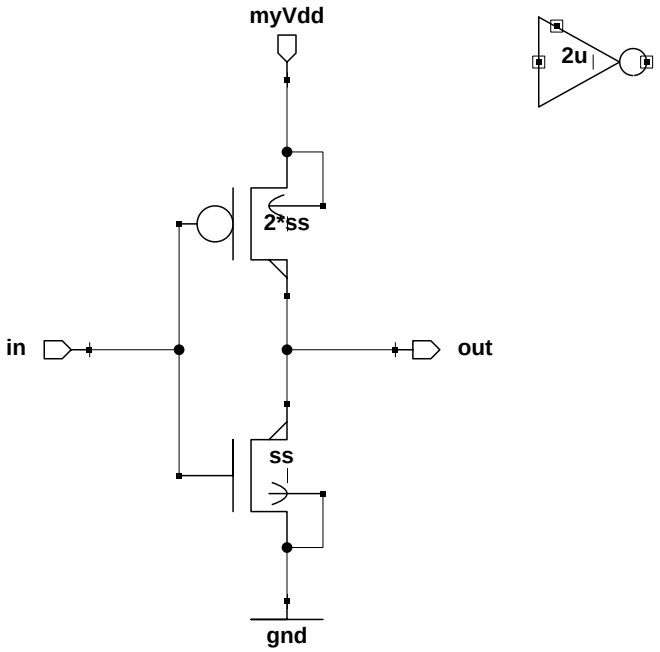

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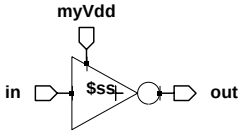

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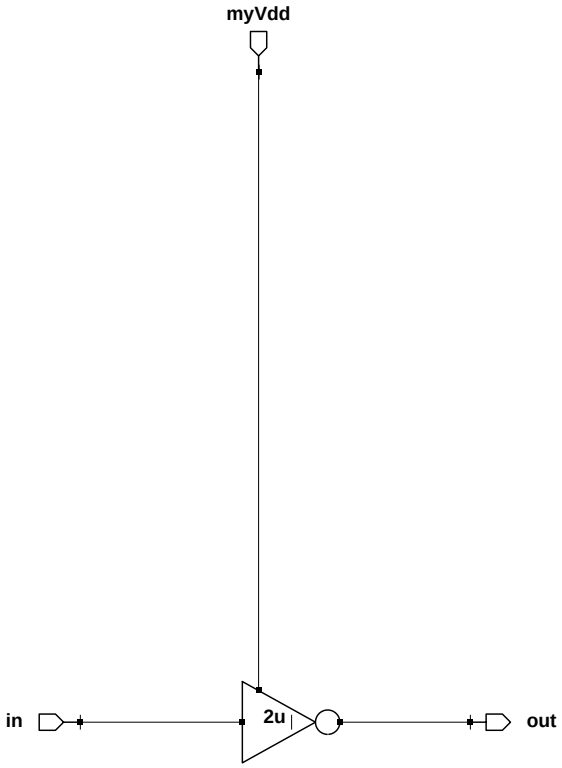

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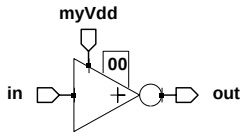

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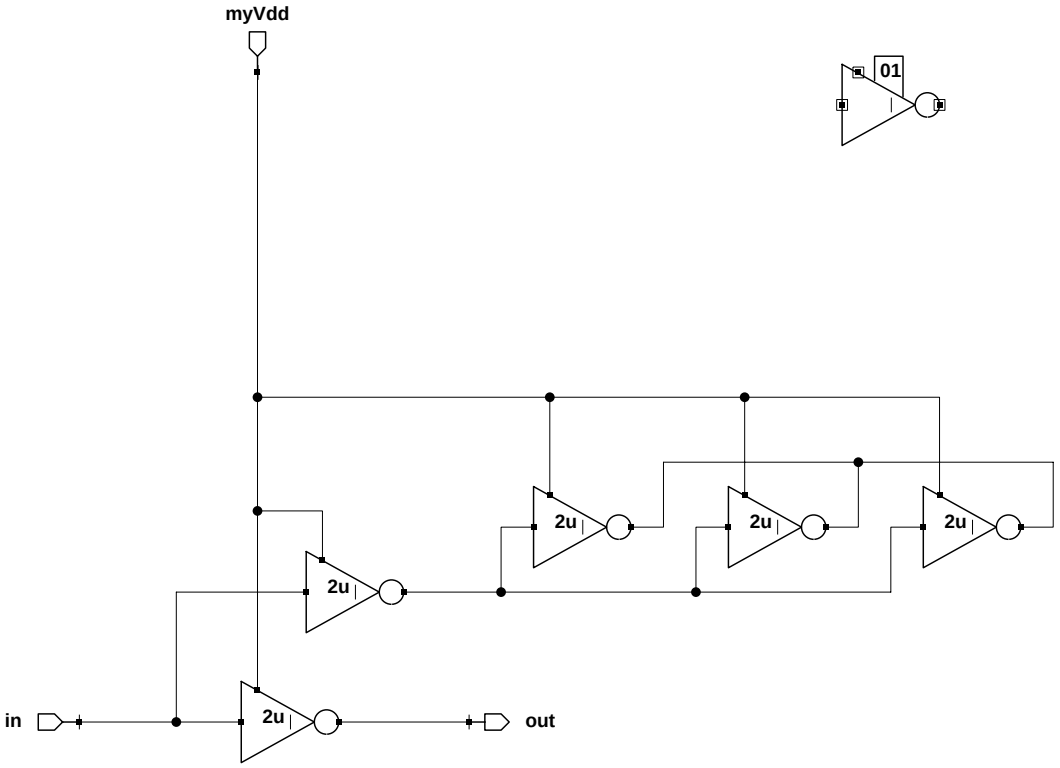

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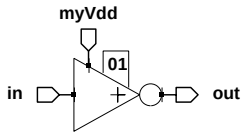

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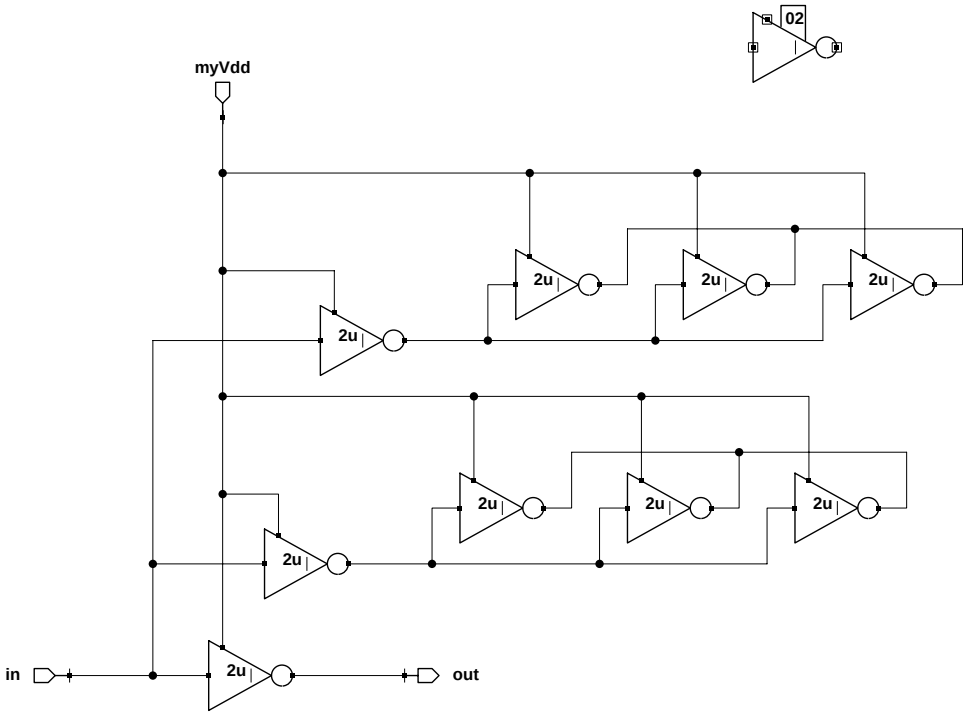

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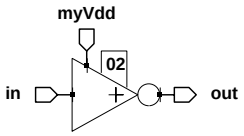

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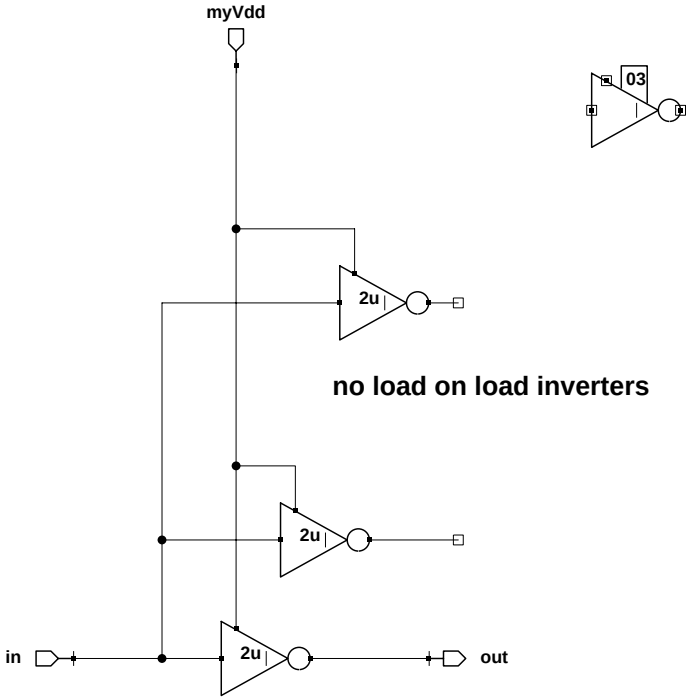

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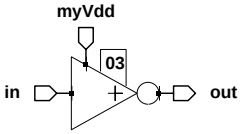

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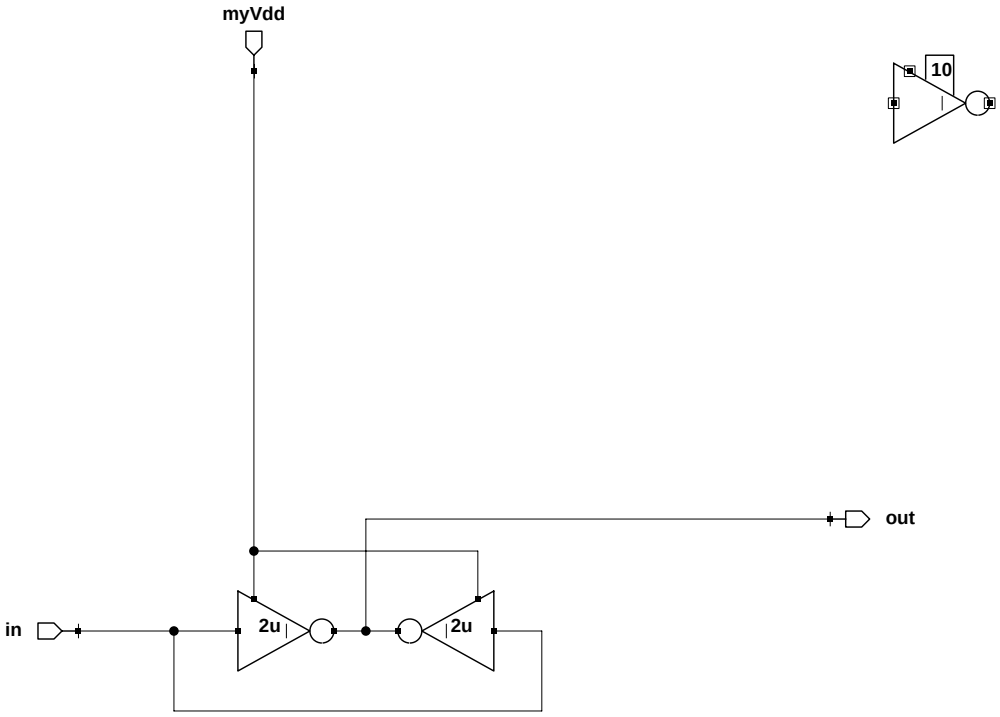

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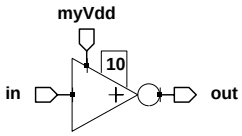

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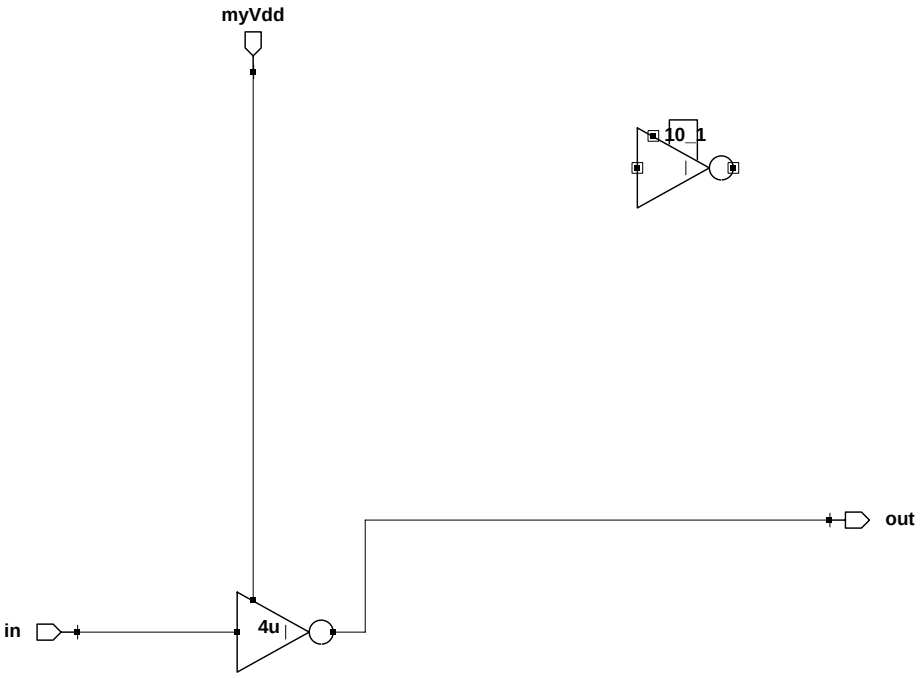

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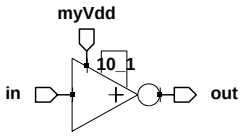

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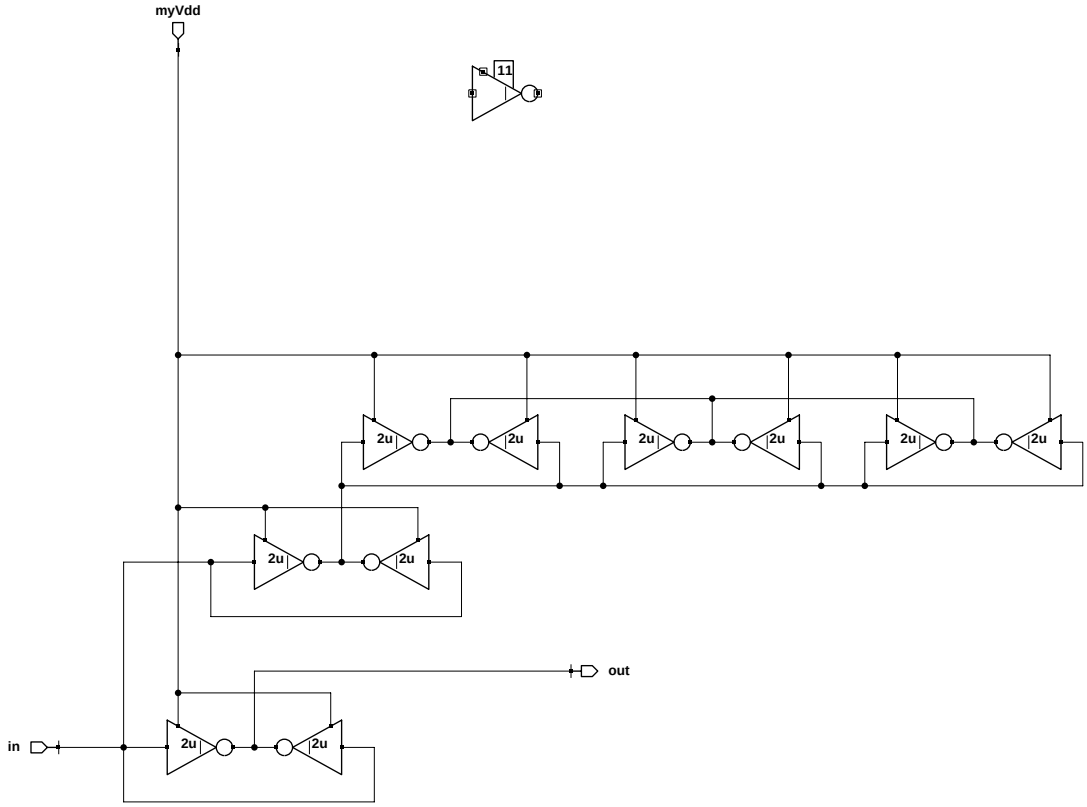

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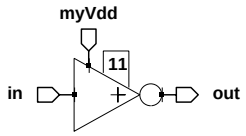

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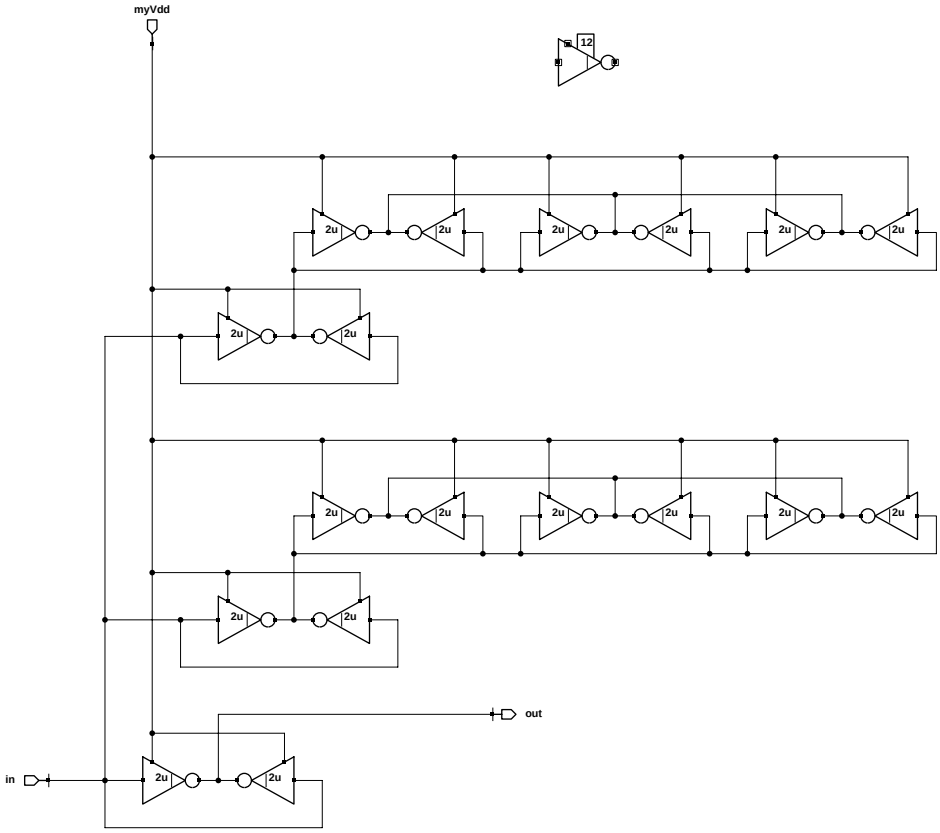

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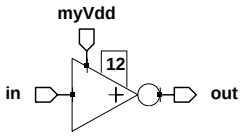

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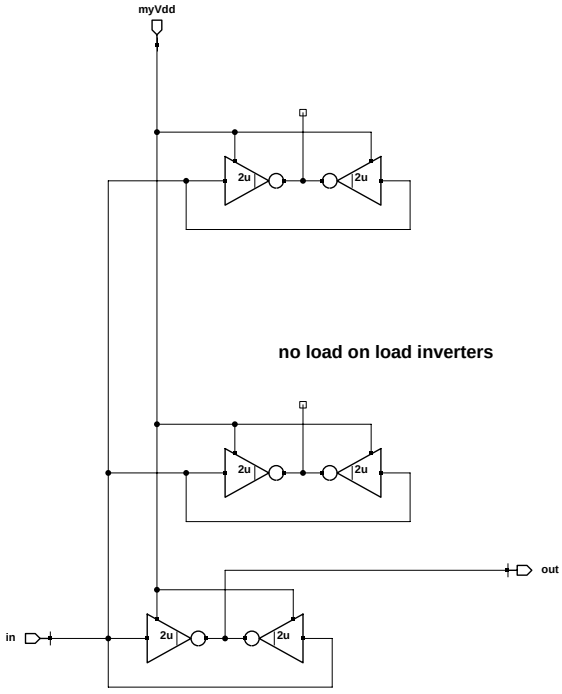

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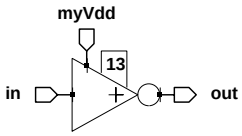

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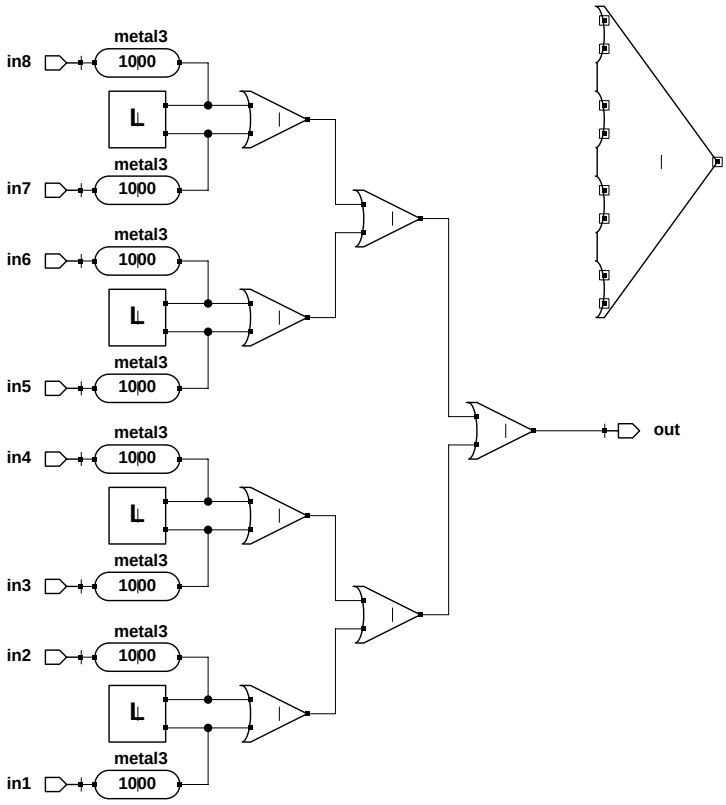

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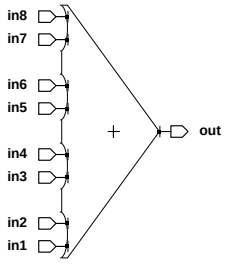

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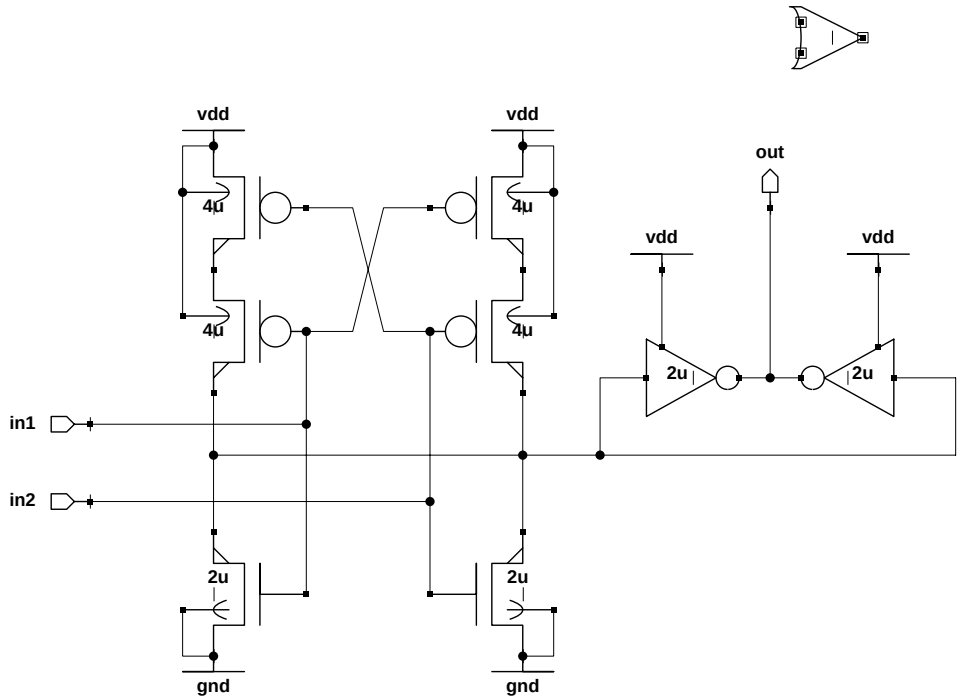

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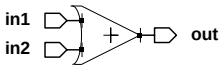

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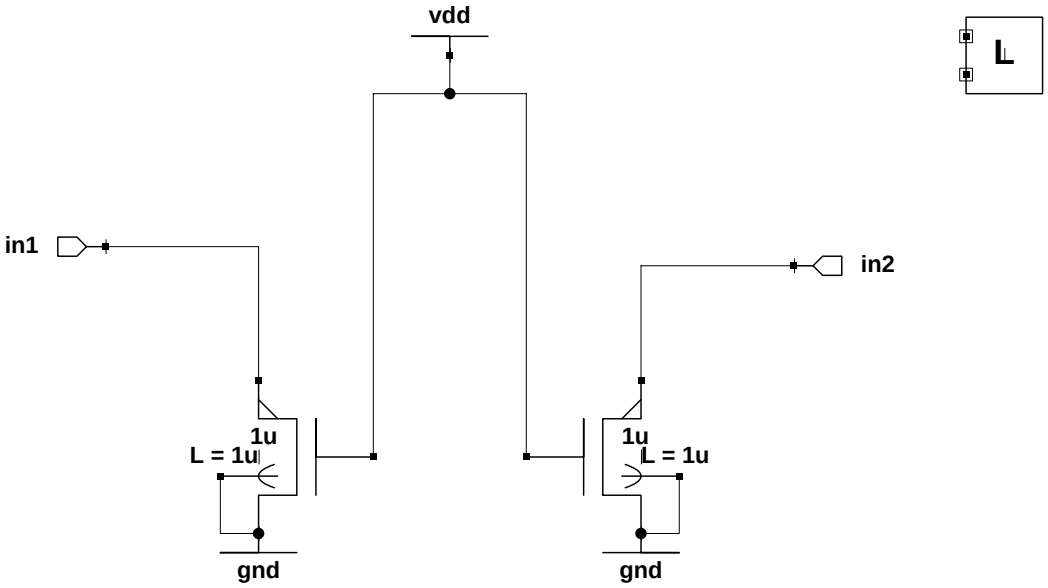

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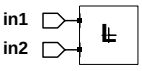

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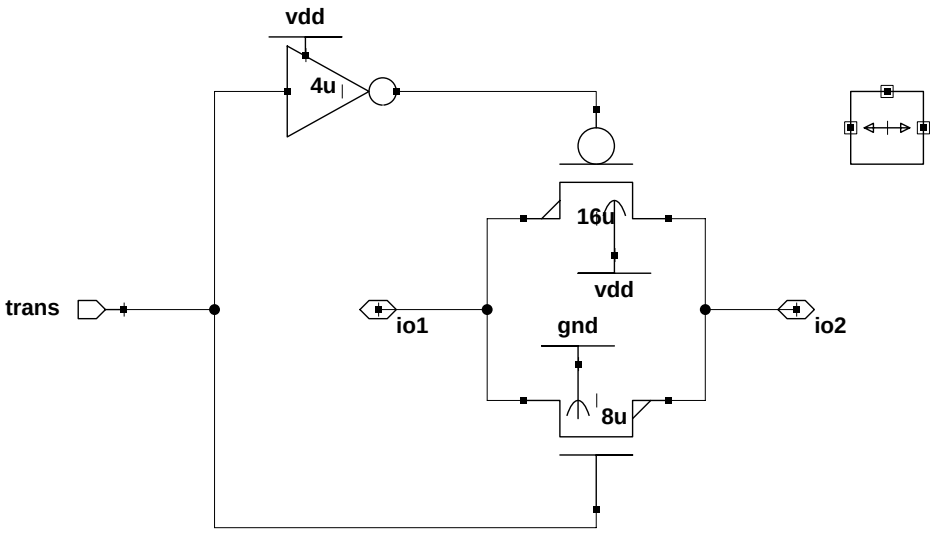

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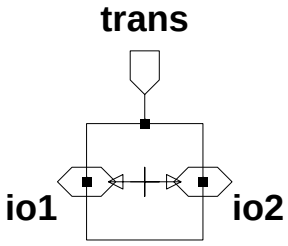

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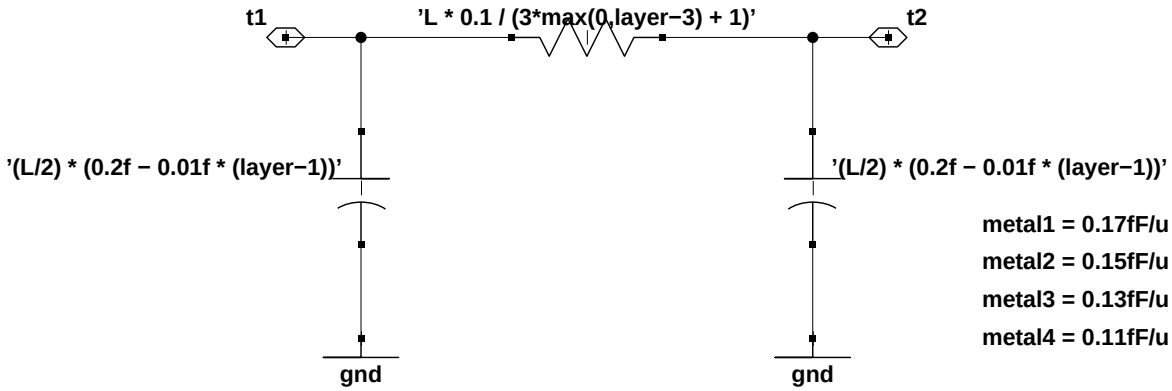
paramaterized wire model for the HP GMOS10qa process

denominator is 1 for metal1,2,3 and 4 for metal4



SUE

owner: Ian W. Jones	**modified: Thu May 04 02:52:0p PDT 2000**
cell: polyWire	**file: /proj/async/db/2000/duchessII/schematics/polyWire.sue**

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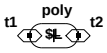

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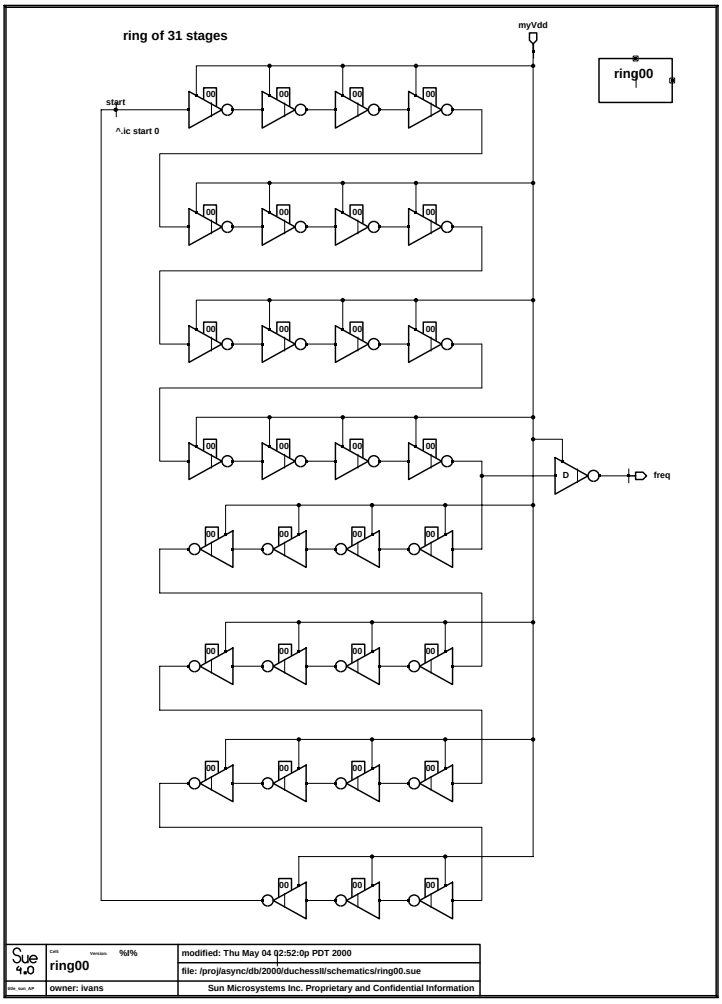

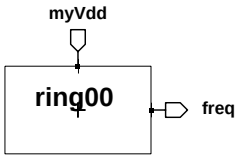

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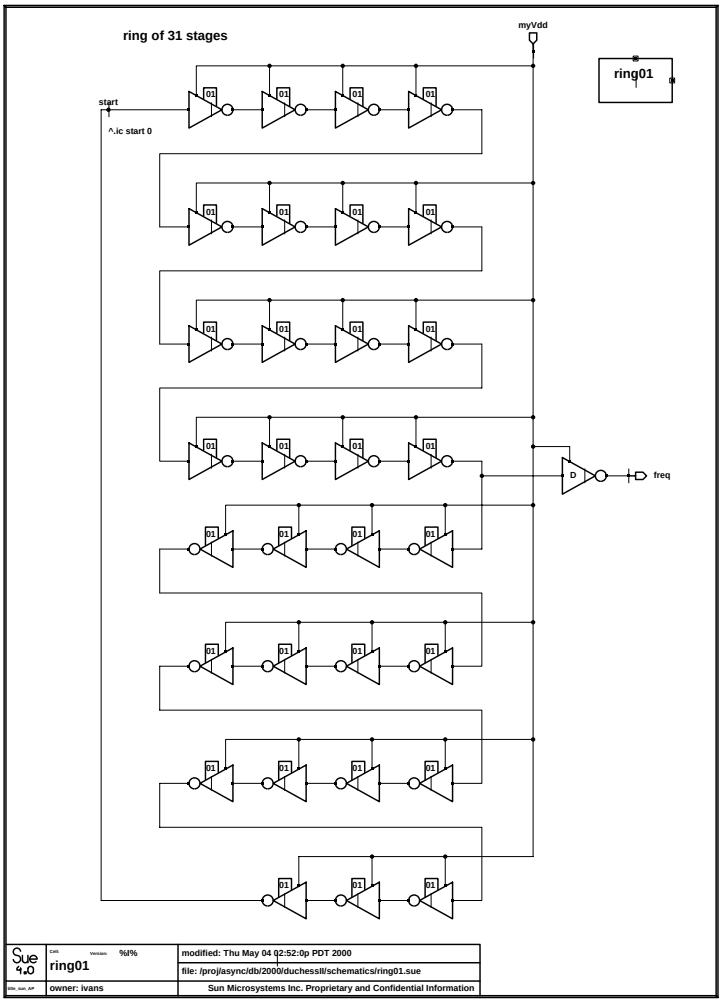

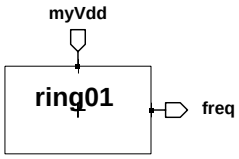

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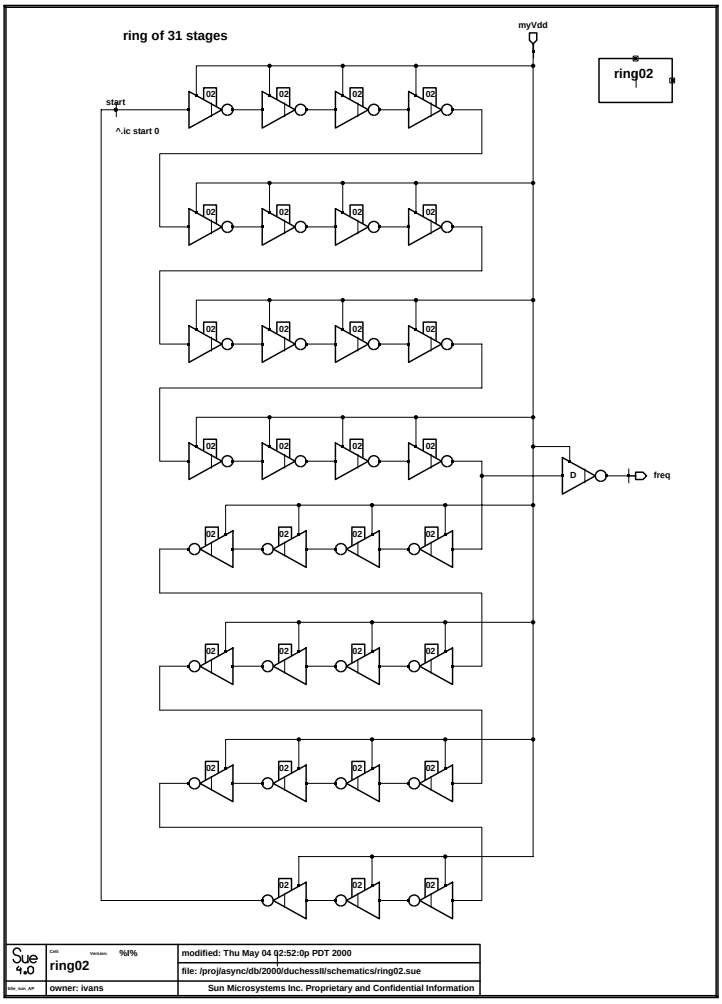

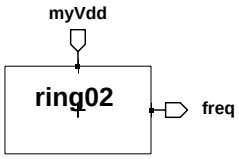

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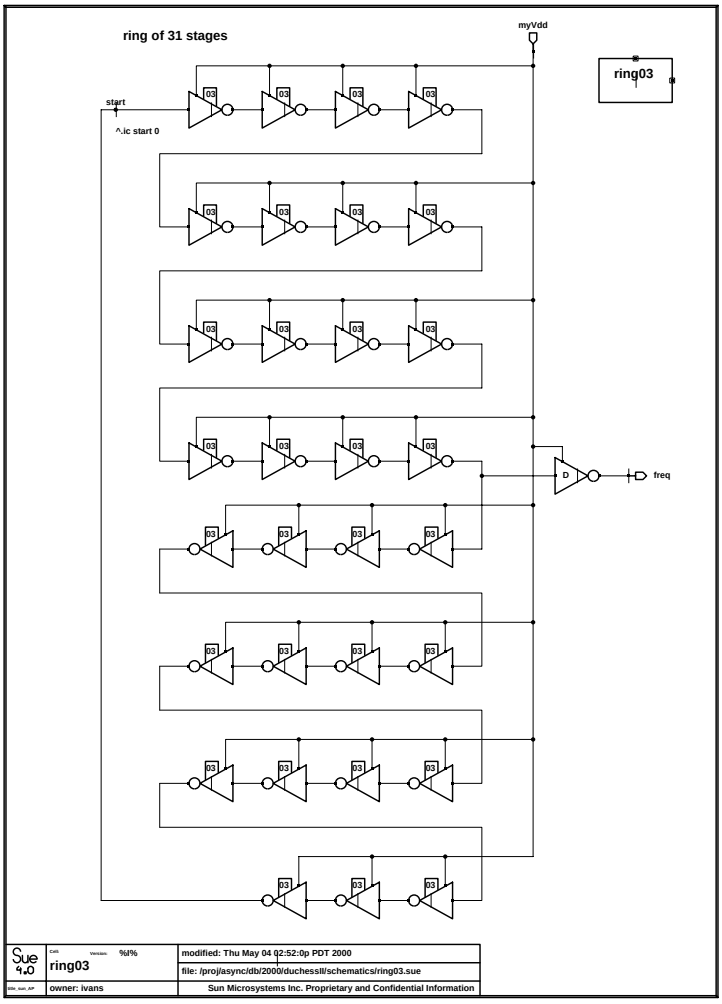

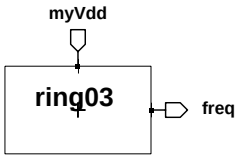

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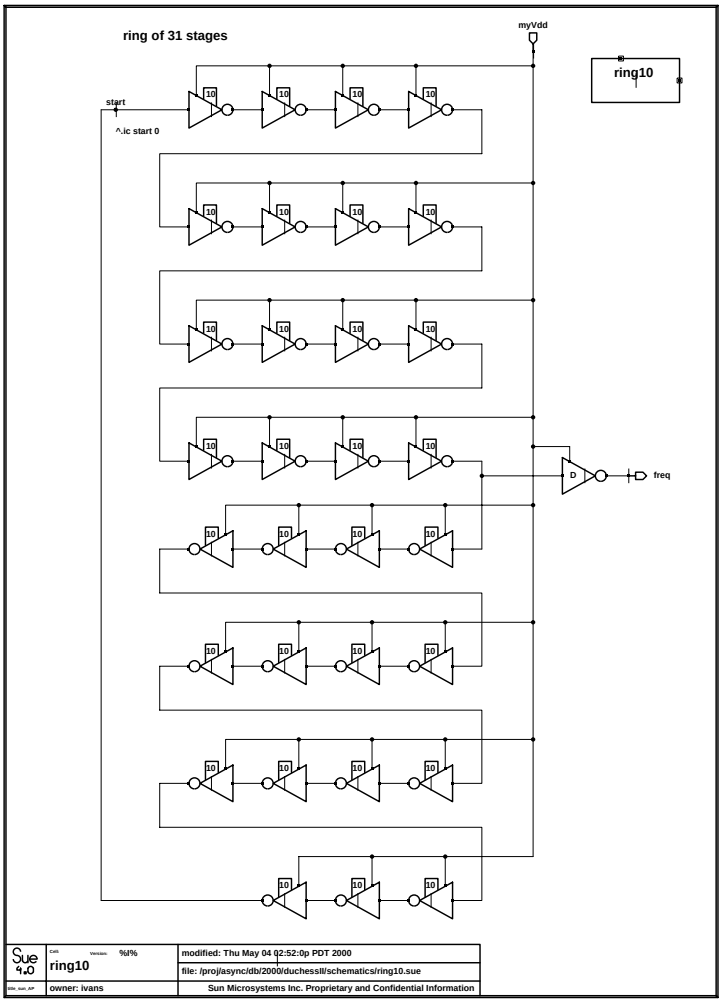

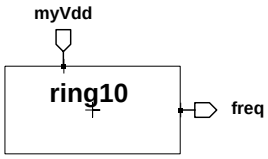

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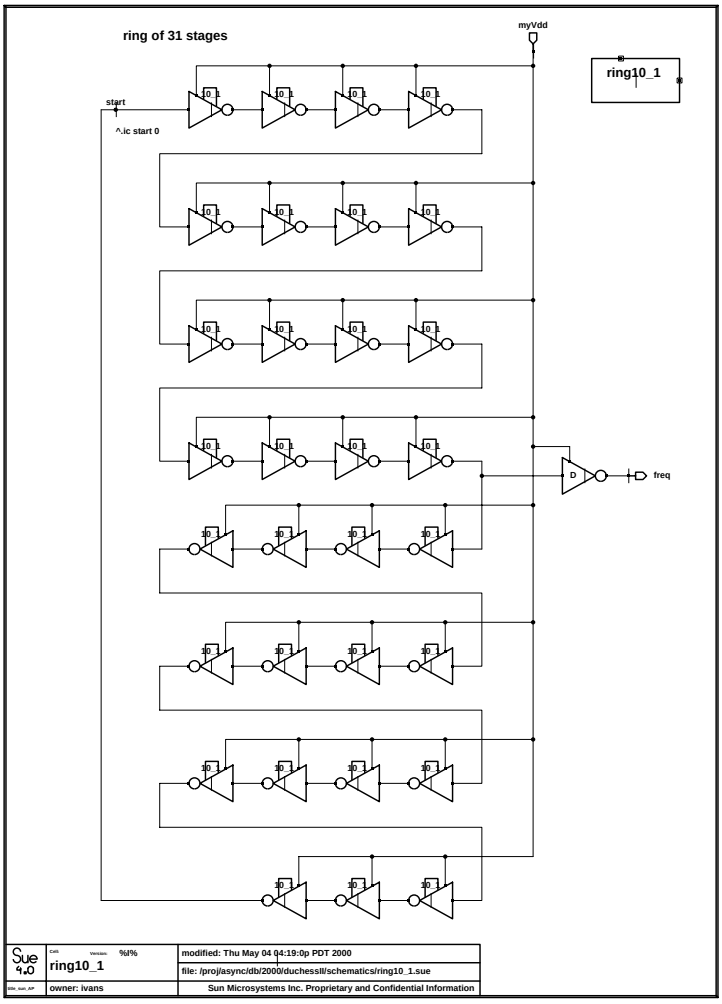

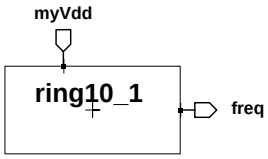

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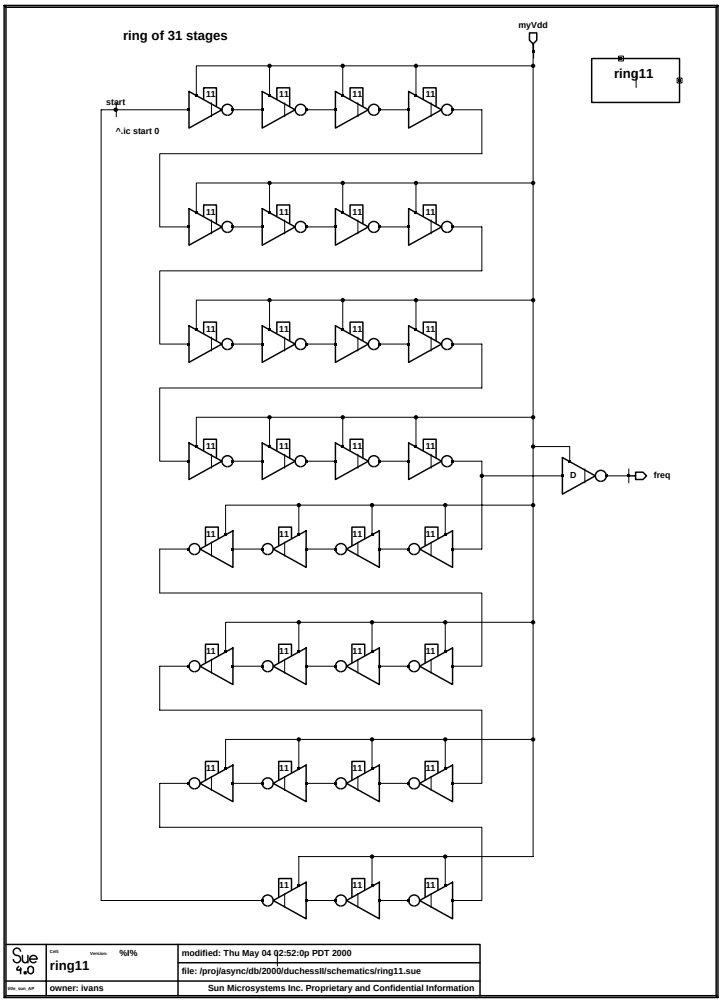

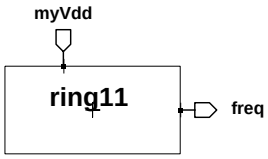

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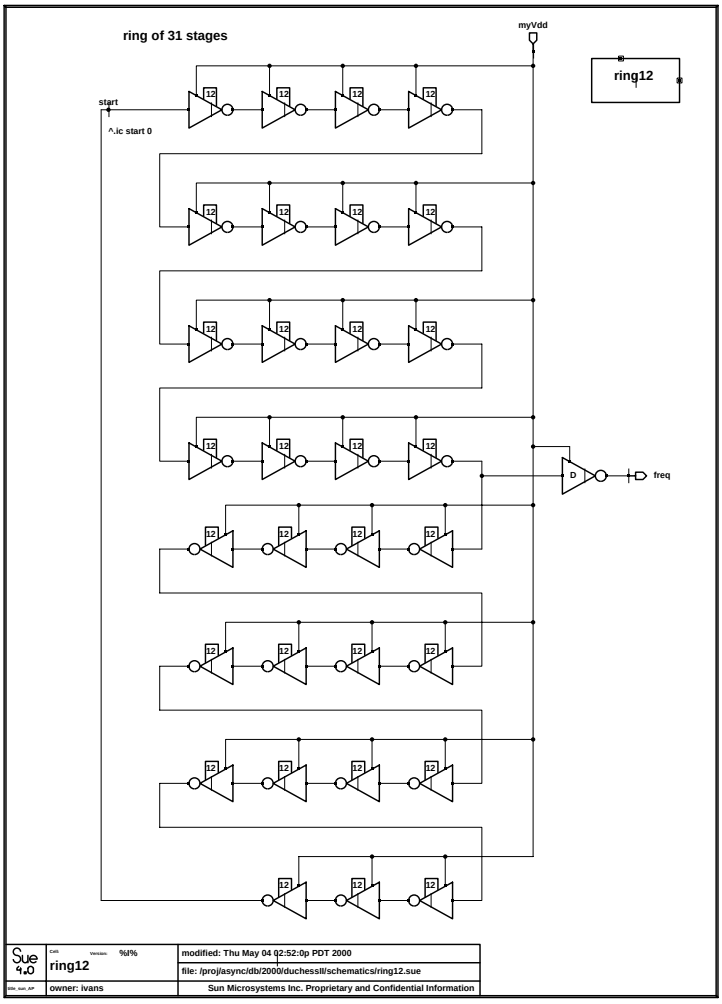

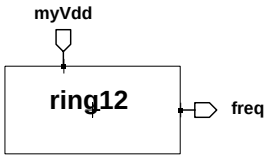

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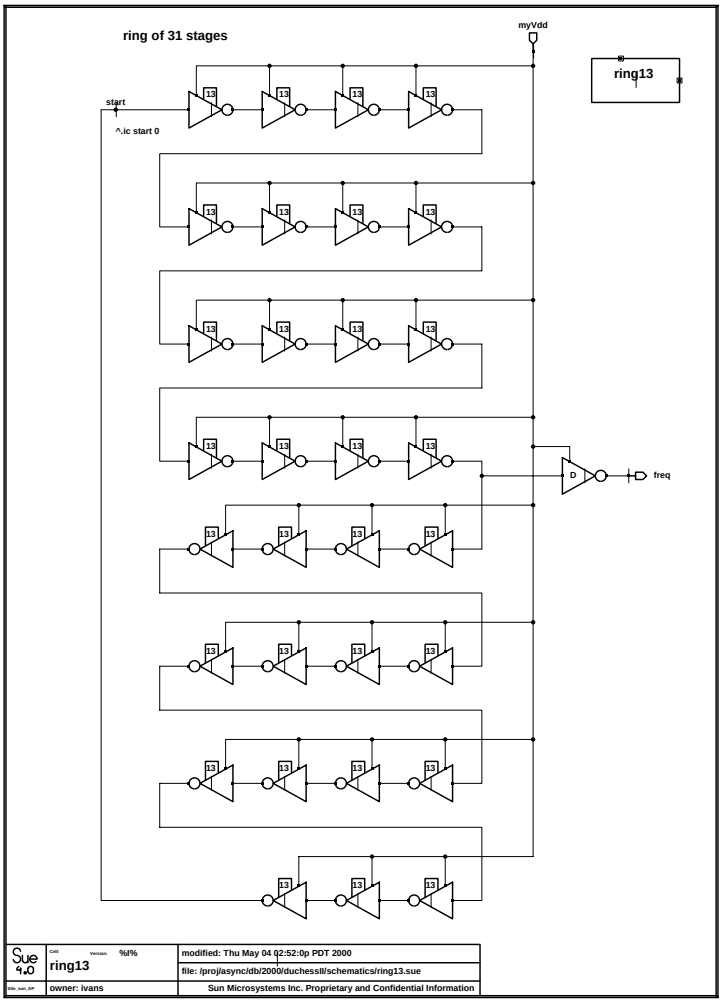

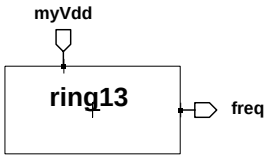

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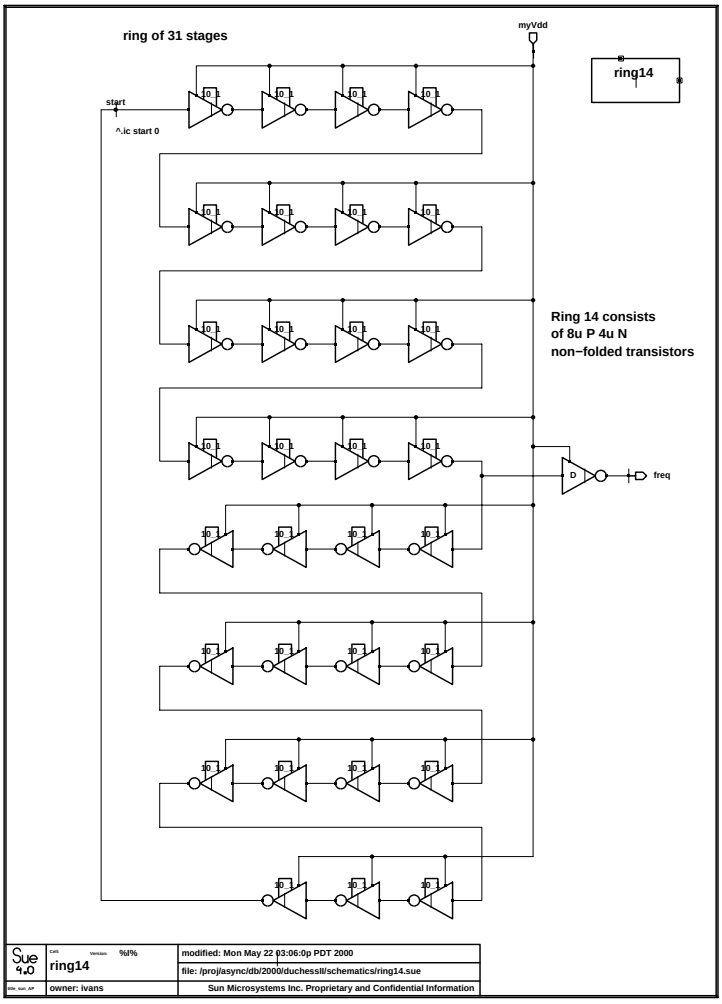

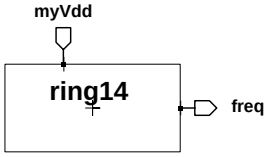

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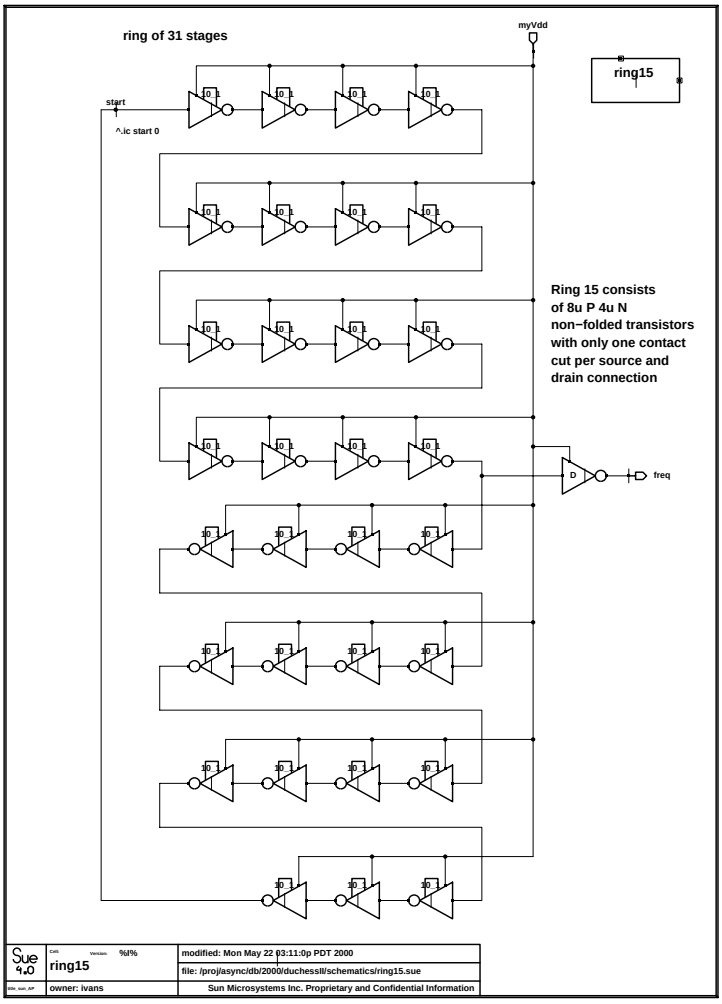

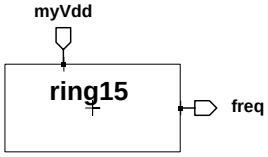

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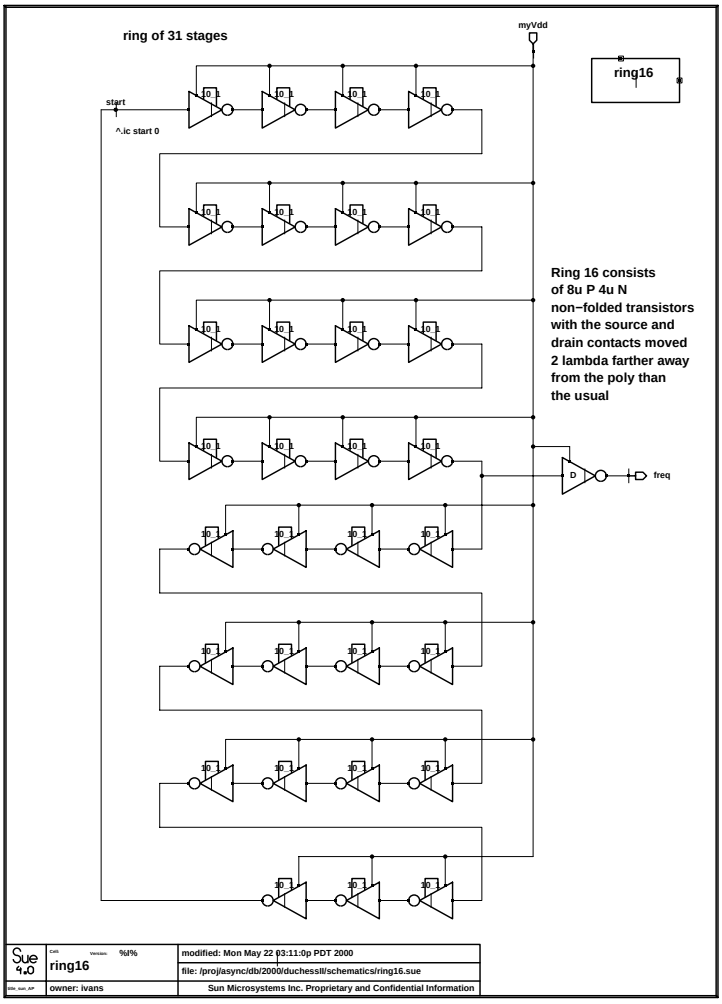

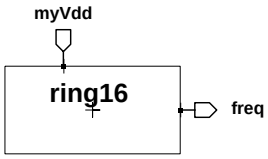

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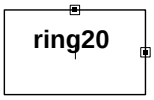
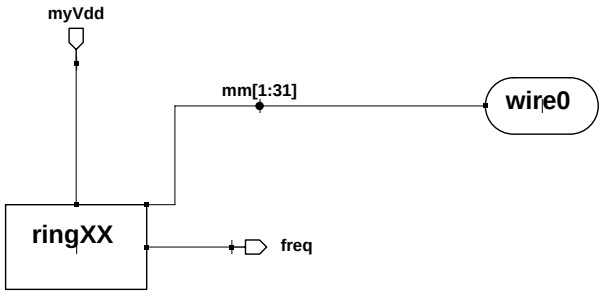


this has 50 micron poly wire loads



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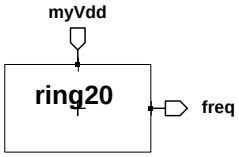

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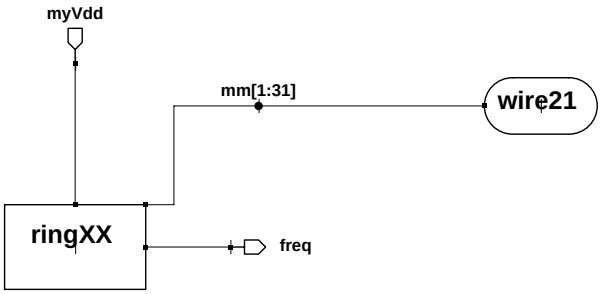
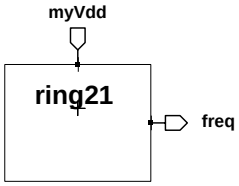
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

this has 100 micron metal 1 wire loads



Sue 4.0	Cell: ring21 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring21.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

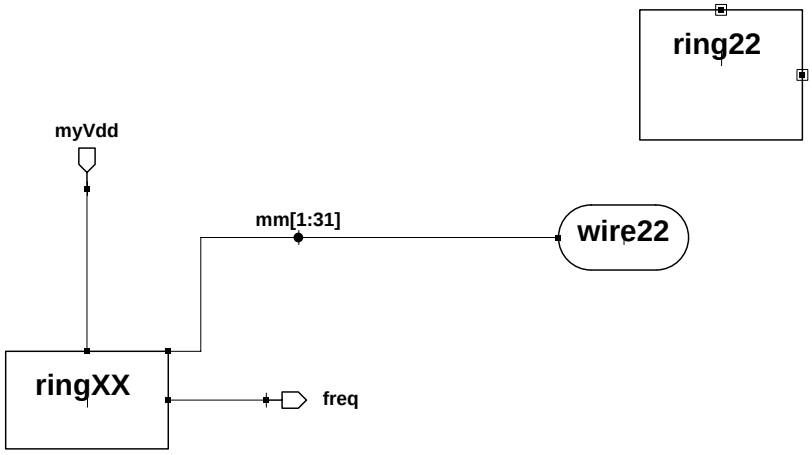


−type user −name name

−type user −name M

Sue 4.0	Cell: ICON_ring21 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring21.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

this has 100 micron wire loads



Sue 4.0	Cell: Version: %I% ring22	modified: Thu May 04 02:52:0p PDT 2000
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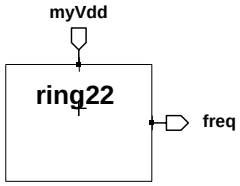
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



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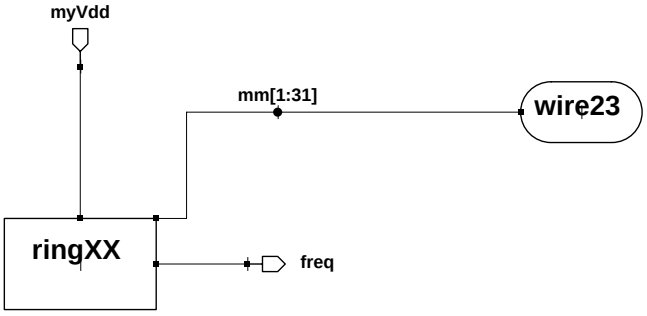
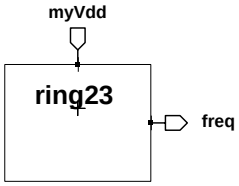
Sue 4.0	Cell: Version: %I% ICON_ring22	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring22.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

this has 100 micron wire loads



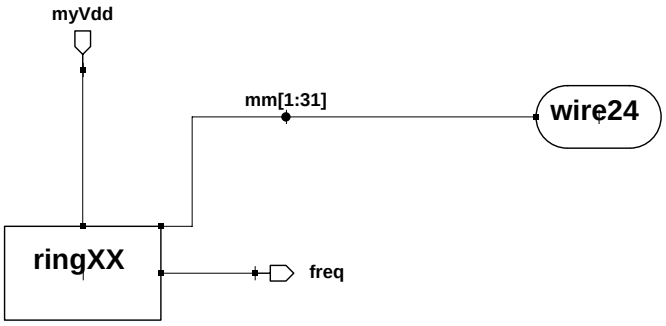
Sue 4.0	Cell: Version: %I% ring23	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring23.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



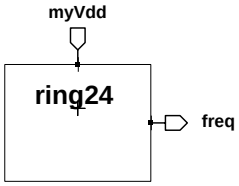
−type user −name name
−type user −name M

Sue 4.0	Cell: Version: %I% ICON_ring23	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring23.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

this has 100 micron wire loads



Sue 4.0	Cell: ring24 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring24.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



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Sue 4.0	Cell: ICON_ring24 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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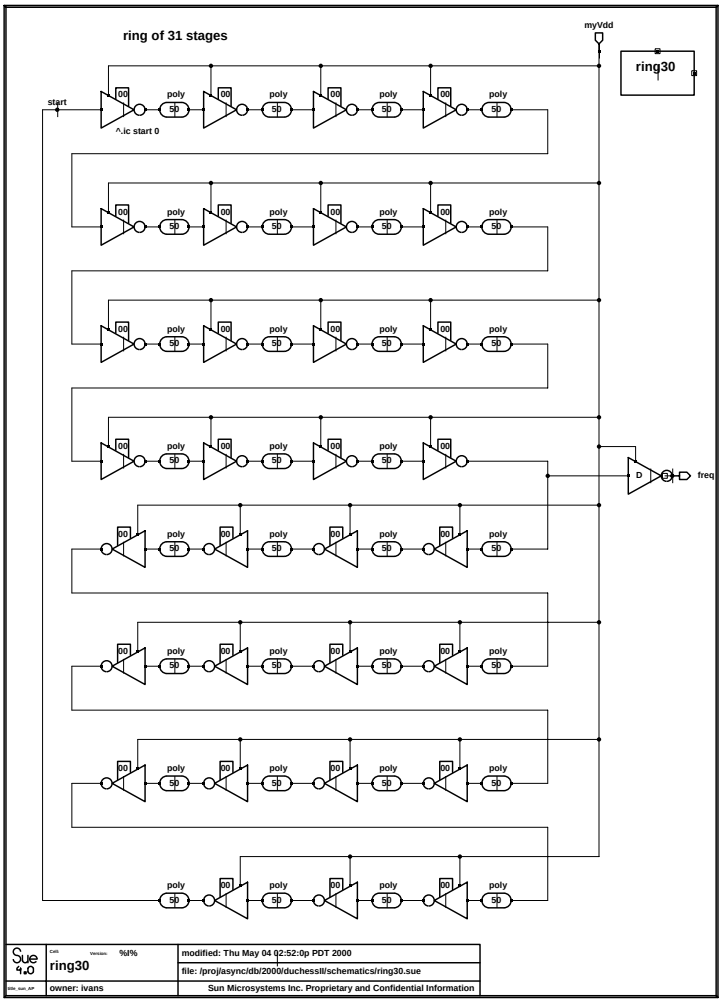
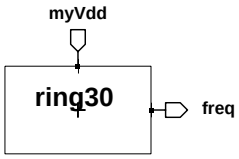
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information





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Sue 4.0	Cell: ICON_ring30 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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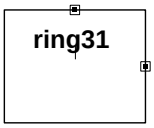
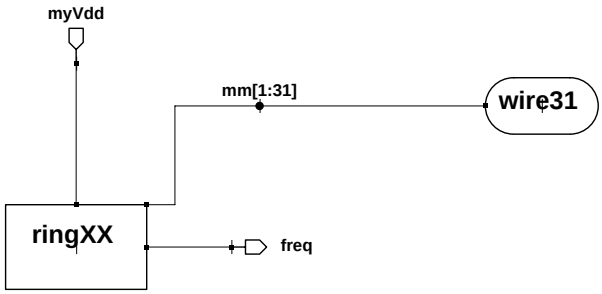
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron metal wire loads with extra grounds



Sue 4.0	Cell: Version: %I% ring31	modified: Thu May 04 02:52:0p PDT 2000
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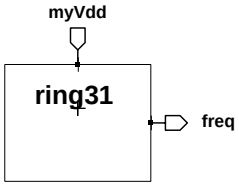
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name
−type user −name M

Sue 4.0	Cell: Version: %I% ICON_ring31	modified: Thu May 04 02:52:0p PDT 2000
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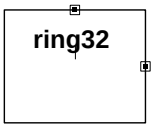
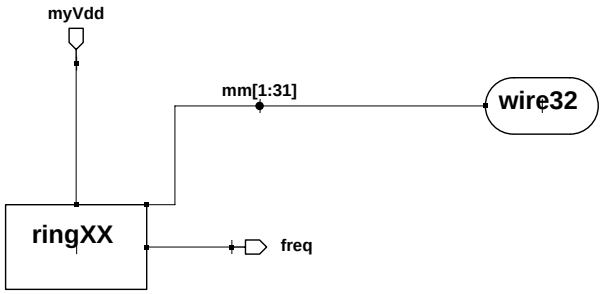
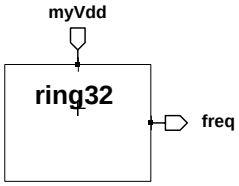
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron metal wire loads with extra grounds



Sue 4.0	Cell: Version: %I% ring32	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring32.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name

−type user −name M

Sue 4.0	Cell: Version: %I% ICON_ring32	modified: Thu May 04 02:52:0p PDT 2000
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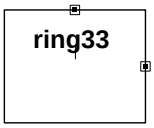
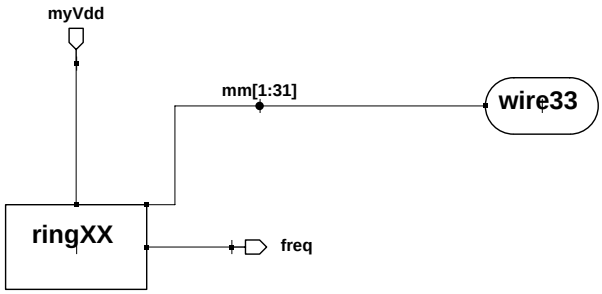
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron metal wire loads with extra grounds



Sue 4.0	Cell: ring33 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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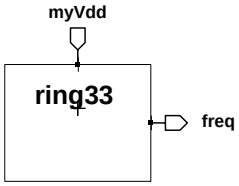
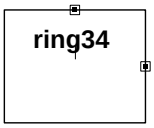
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



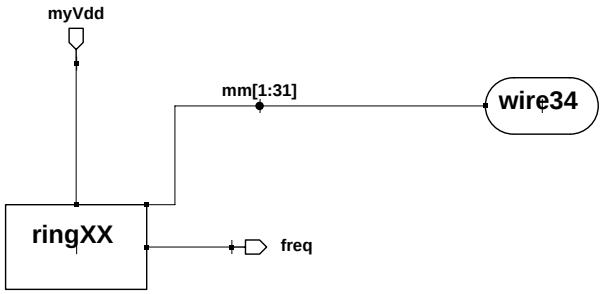
−type user −name name
−type user −name M

Sue 4.0	Cell: ICON_ring33 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring33.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

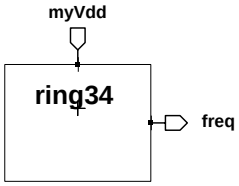


this has 100 micron metal wire loads with extra grounds

100 u of metal 4 loading with grounded
metal 4 runs for sidewall capacitance:
2.4u center to center spacing



Sue 4.0	Cell: Version: %I% ring34	modified: Mon May 22 03:47:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring34.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name
−type user −name M

Sue 4.0	Cell: Version: %I% ICON_ring34	modified: Mon May 22 03:47:0p PDT 2000
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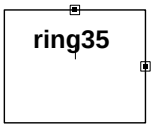
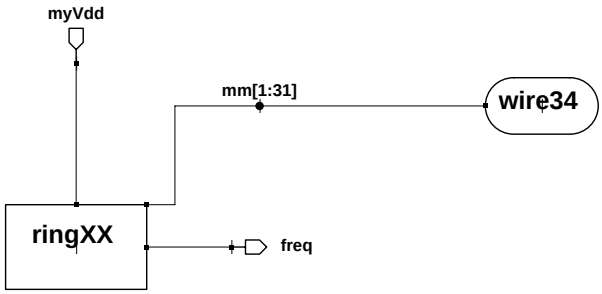
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron metal wire loads with extra grounds

100 u of metal 4 loading with grounded
metal 4 runs for sidewall capacitance:
3.2u center to center spacing



Sue 4.0	Cell: Version: %I% ring35	modified: Mon May 22 03:47:0p PDT 2000
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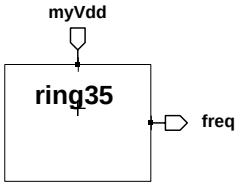
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



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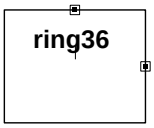
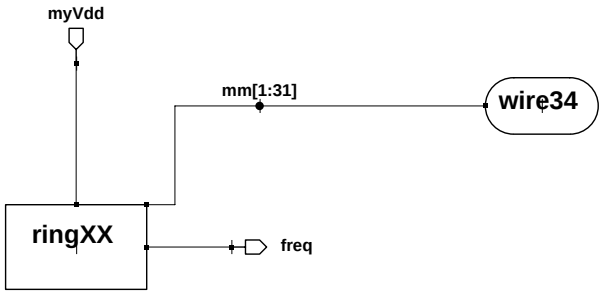
Sue 4.0	Cell: Version: %I% ICON_ring35	modified: Mon May 22 03:47:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring35.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

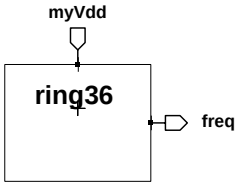


this has 100 micron metal wire loads with extra grounds

100 u of metal 4 loading with grounded
metal 4 runs for sidewall capacitance:
6.4u center to center spacing

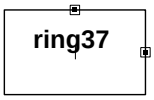


Sue 4.0	Cell: Version: %I% ring36	modified: Mon May 22 03:48:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring36.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

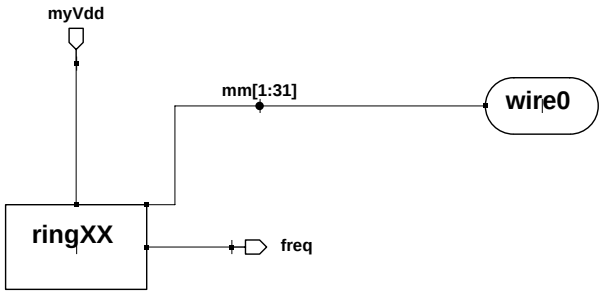


−type user −name name
−type user −name M

Sue 4.0	Cell: Version: %I% ICON_ring36	modified: Mon May 22 03:48:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring36.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron series poly wire loads



Sue 4.0	Cell: ring37 Version: %I%	modified: Mon May 22 03:49:0p PDT 2000
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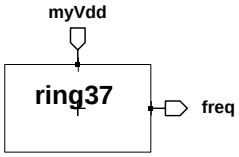
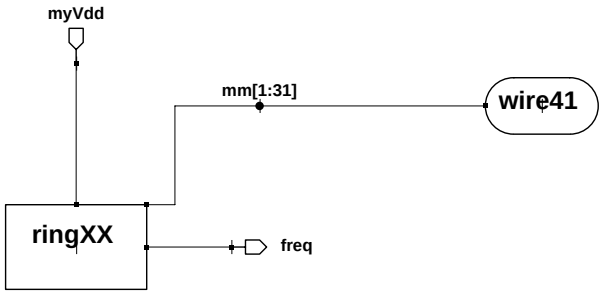
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



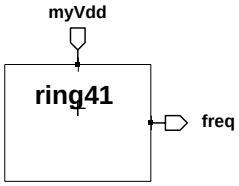
−type user −name name
−type user −name M

Sue 4.0	Cell: ICON_ring37 Version: %I%	modified: Mon May 22 03:49:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring37.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

this has 100 micron metal wire loads with surround and cross



Sue 4.0	Cell: Version: %I% ring41	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring41.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



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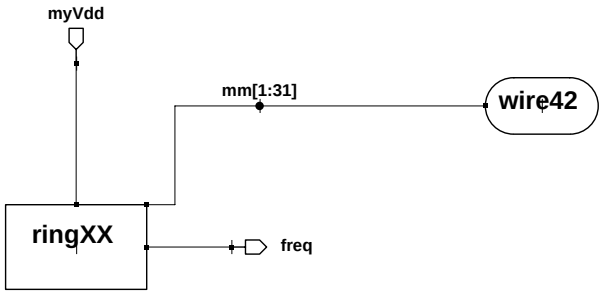
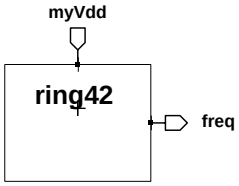
−type user −name M

Sue 4.0	Cell: Version: %I% ICON_ring41	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring41.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

this has 100 micron metal wire loads with surround and cross



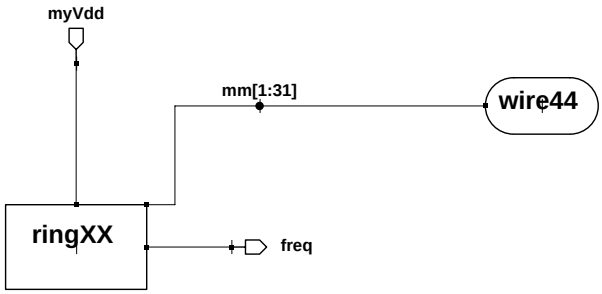
Sue 4.0	Cell: Version: %I% ring42	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring42.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



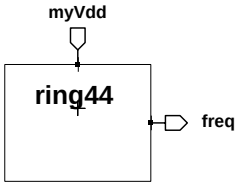
−type user −name name
−type user −name M

Sue 4.0	Cell: Version: %I% ICON_ring42	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring42.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

this has 100 micron metal wire loads with surround and cross



Sue 4.0	Cell: Version: %I% ring44	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring44.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name
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Sue 4.0	Cell: Version: %I% ICON_ring44	modified: Thu May 04 02:52:0p PDT 2000
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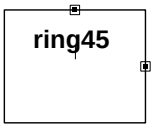
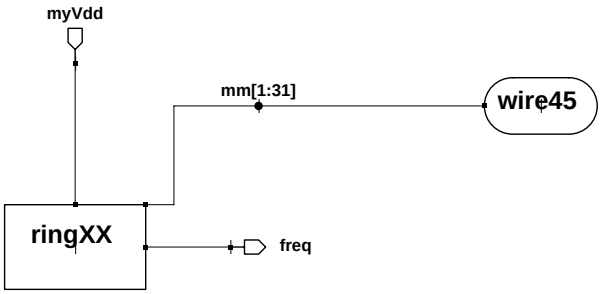
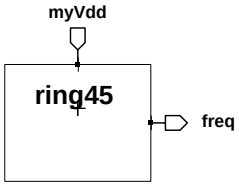
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



this has 100 micron metal wire loads with surround and cross



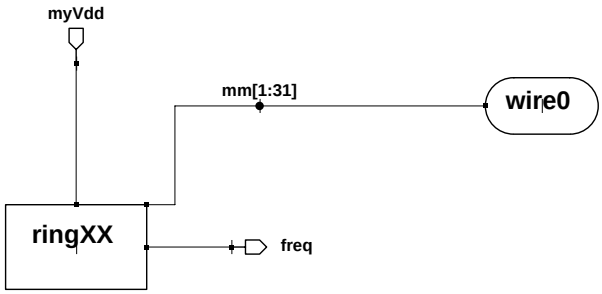
Sue 4.0	Cell: Version: %I% ring45	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring45.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



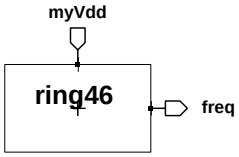
−type user −name name
−type user −name M

Sue 4.0	Cell: Version: %I% ICON_ring45	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring45.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

this has 50 micron poly wire loads
crossed by m1 wires



Sue 4.0	Cell: ring46 Version: %I%	modified: Mon May 22 03:40:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/ring46.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name
−type user −name M

Sue 4.0	Cell: ICON_ring46 Version: %I%	modified: Mon May 22 03:40:0p PDT 2000
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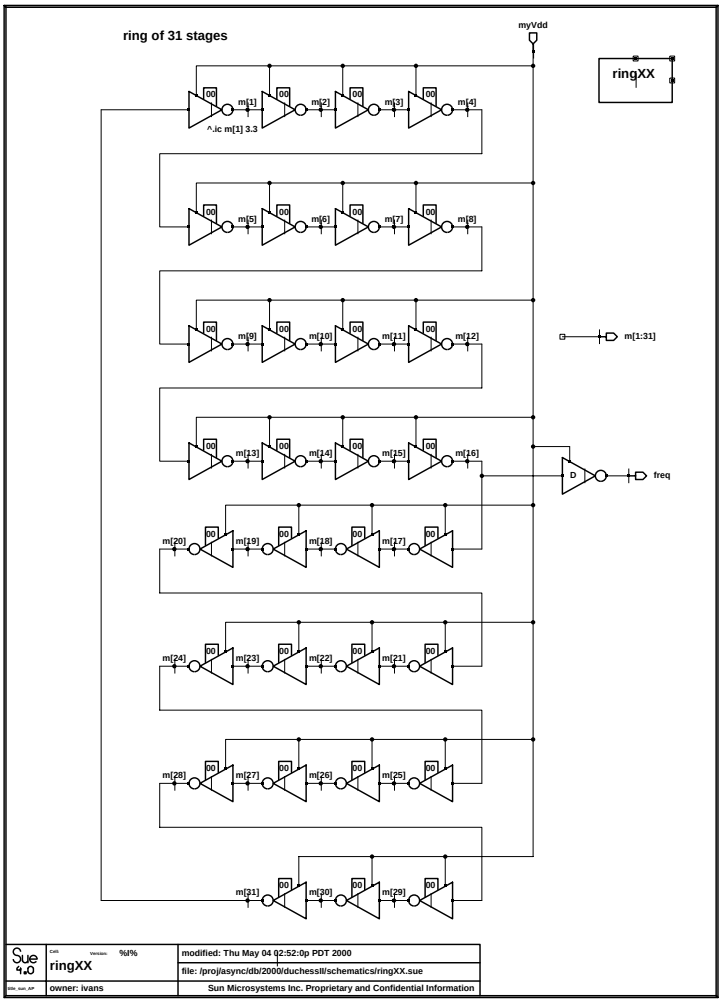
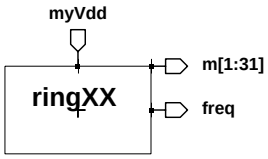
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information





−type user −name name

−type user −name M

Sue 4.0	Cell: ICON_ringXX Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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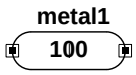
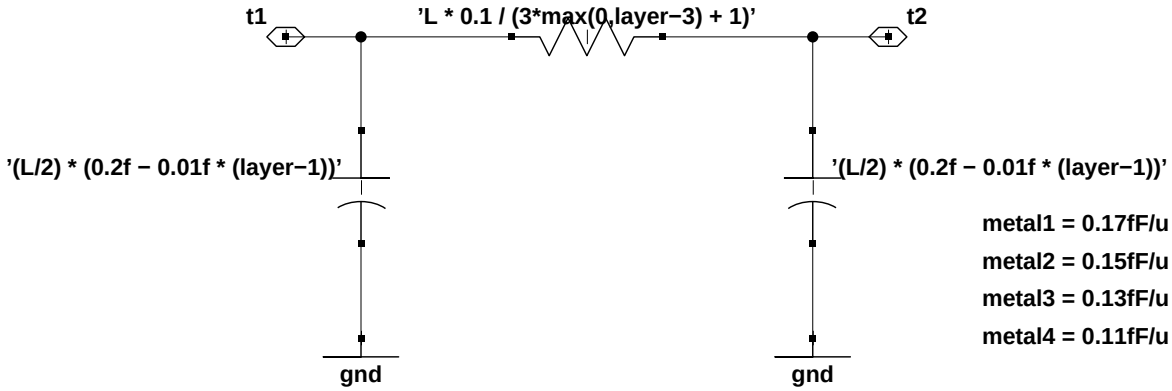
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



paramaterized wire model for the HP GMOS10qa process

denominator is 1 for metal1,2,3 and 4 for metal4



SUE

owner: Ian W. Jones	**modified: Thu May 04 02:52:0p PDT 2000**
cell: wire	**file: /proj/async/db/2000/duchessII/schematics/wire.sue**

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```
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−type user −name L −default 100
−type fixed −name cdlold −text {equiv $t1 $t2}
−type user −name layer −default 1
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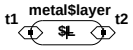
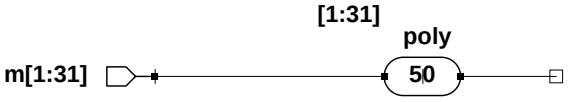


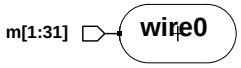
Sue 4.0	Cell: ICON_wire Version: 1.9	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire.sue
title_bar_sun	owner: Ian W. Jones	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of poly wire each 50 microns long



this is poly, in spite of saying metal1

Sue 4.0	Cell: wire0 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire0.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name
−type user −name M

Sue 4.0	Cell: ICON_wire0 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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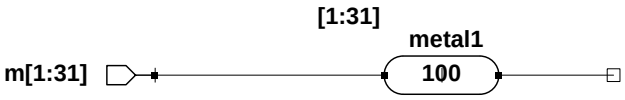
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long



Sue 4.0	Cell: wire21 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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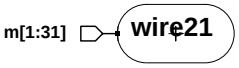
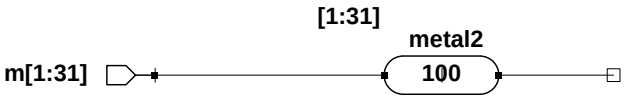
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name
−type user −name M

Sue 4.0	Cell: ICON_wire21 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire21.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long



Sue 4.0	Cell: wire22 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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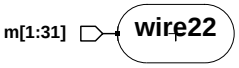
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name
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Sue 4.0	Cell: ICON_wire22 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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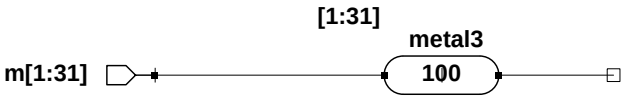
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long



Sue 4.0	Cell: wire23 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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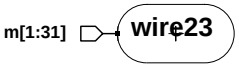
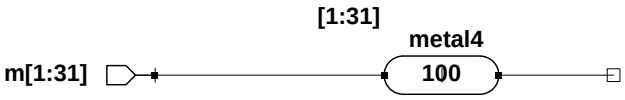


−type user −name name
−type user −name M

Sue 4.0	Cell: ICON_wire23 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire23.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long



Sue 4.0	Cell: Version: %I% **wire24**	modified: Thu May 04 02:52:0p PDT 2000
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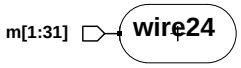
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name
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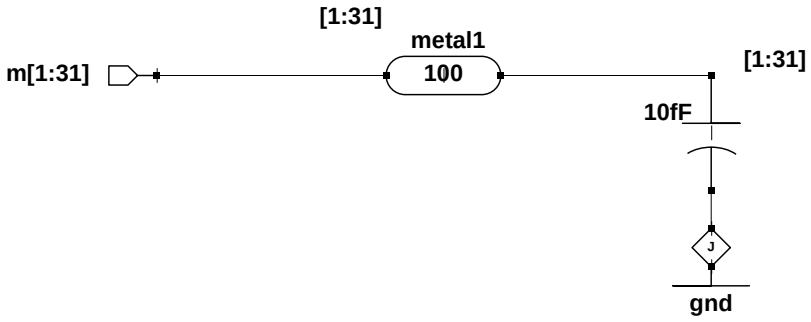
Sue 4.0	Cell: Version: %I% **ICON_wire24**	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire24.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides



Sue 4.0	Cell: Version: %I% **wire31**	modified: Thu May 04 02:52:0p PDT 2000
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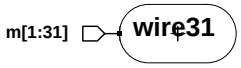
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name

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Sue 4.0	Cell: Version: %I% **ICON_wire31**	modified: Thu May 04 02:52:0p PDT 2000
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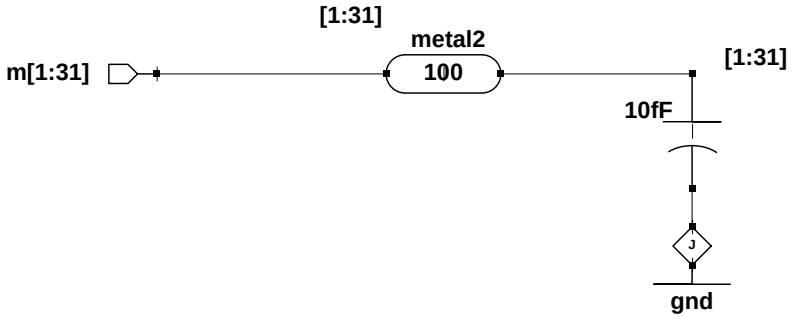
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides



Sue 4.0	Cell: Version: %I% **wire32**	modified: Thu May 04 02:52:0p PDT 2000
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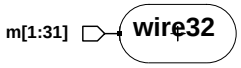
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name

−type user −name M

Sue 4.0	Cell: Version: %I% **ICON_wire32**	modified: Thu May 04 02:52:0p PDT 2000
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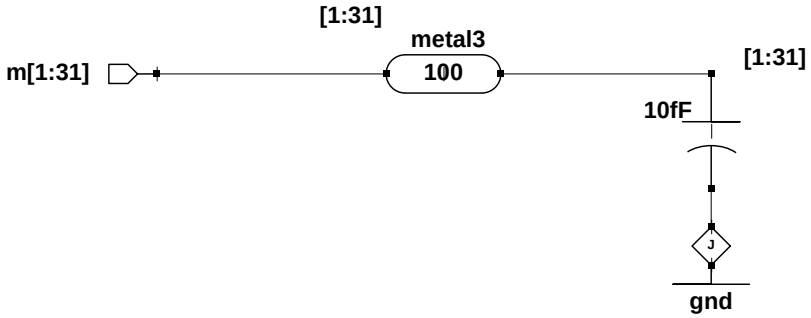
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides



Sue 4.0	Cell: Version: %I% **wire33**	modified: Thu May 04 02:52:0p PDT 2000
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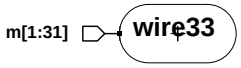
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name
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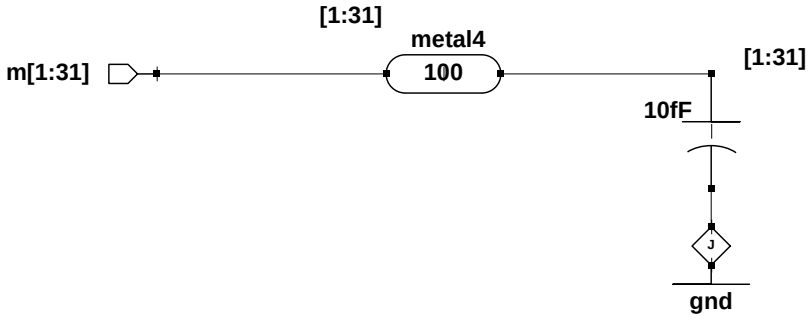
Sue 4.0	Cell: Version: %I% **ICON_wire33**	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire33.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides



Sue 4.0	Cell: Version: %I% **wire34**	modified: Thu May 04 02:52:0p PDT 2000
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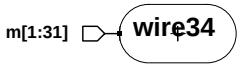
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



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Sue 4.0	Cell: Version: %I% **ICON_wire34**	modified: Thu May 04 02:52:0p PDT 2000
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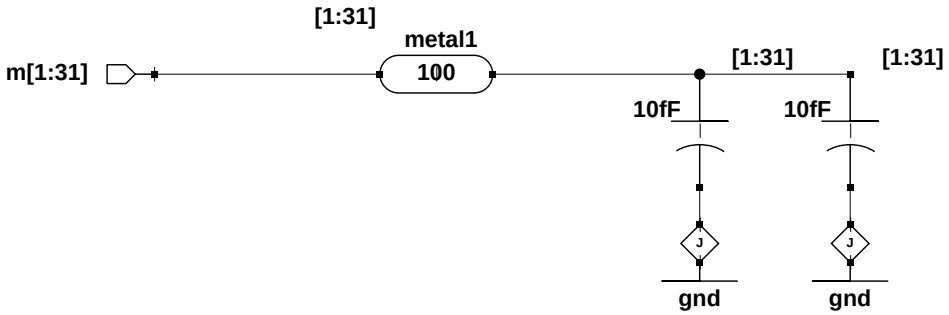
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



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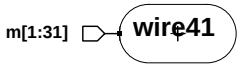
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name

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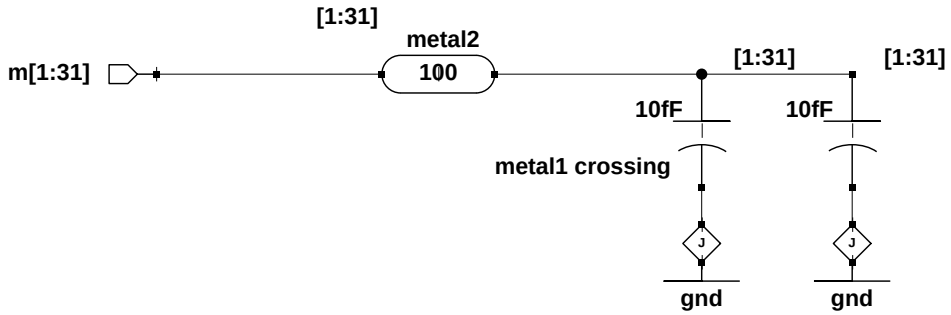
Sue 4.0	Cell: ICON_wire41 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire41.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



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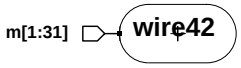
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name

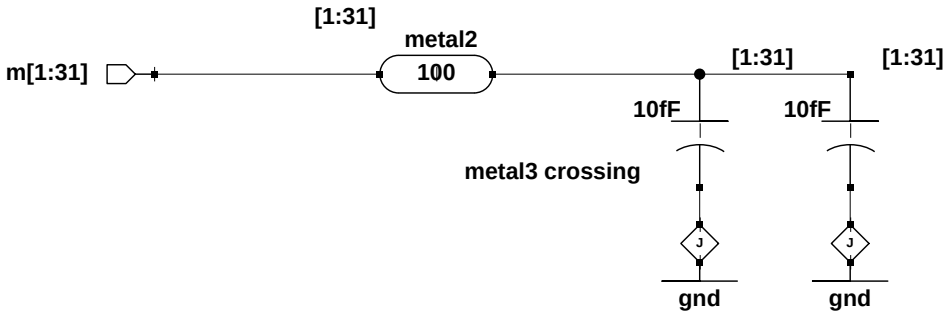
−type user −name M

Sue 4.0	Cell: ICON_wire42 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire42.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

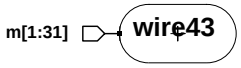
there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



Sue 4.0	Cell: wire43 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire43.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name

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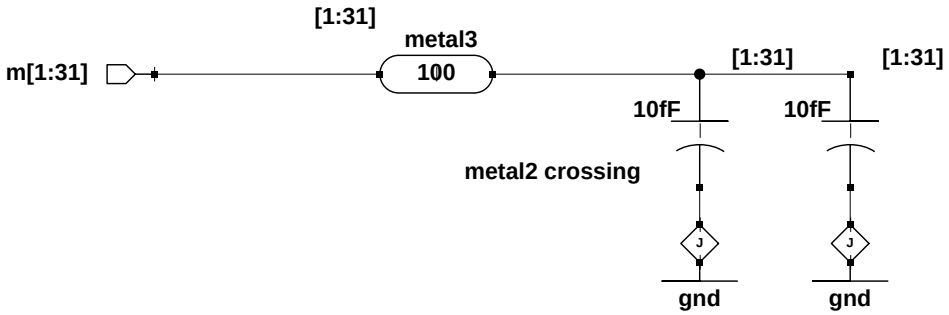
Sue 4.0	Cell: ICON_wire43 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire43.sue
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

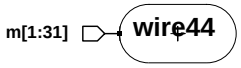
there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



Sue 4.0	Cell: wire44 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
		file: /proj/async/db/2000/duchessII/schematics/wire44.sue
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



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Sue 4.0	Cell: ICON_wire44 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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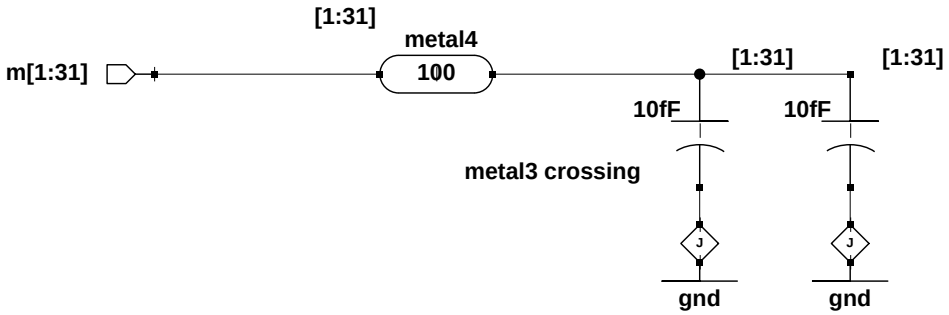
title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

there are 31 pieces of wire each 100 microns long

each is flanked by matching wire on both sides

each passes over or under 50 crossings of adjacent layers



Sue 4.0	Cell: wire45 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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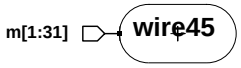
title_bar_sun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information



−type user −name name

−type user −name M

Sue 4.0	Cell: ICON_wire45 Version: %I%	modified: Thu May 04 02:52:0p PDT 2000
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title_bar_iconsun	owner: ivans	Sun Microsystems Inc. Proprietary and Confidential Information

Appendix C

Schematics

2001−0097 DuchessIII − Schematics and Pinout
Gainsley, 5 February 2001

Sun Microsystems Laboratories

Title: **DuchessIII - Schematics and Pinout**
Date: **5 Feb 2001**
Author: **Jonathan Gainsley**
SML #: **2001-0097**

References:

[1] SML# 2001-0076: “DuchessIII - The Chip,” Gainsley, 22 Jan 2001
[2] SML# 2000-0271: “Pinout for the DuchessII Chip,” Gainsley, 12 Jun 2000
[3] SML# 2000-0278: “Schematics for the DuchessII Test Chip,” Gainsley, 14 Jun 2000
[4] SML# 2001-0092: “DuchessIII - Changes from DuchessII,” Gainsley, 30 Jan 2001

Introduction

This memo documents the schematics and pinout of the DuchessIII [1] chip.

Pinout

The pinout of the DuchessIII chip remains unchanged from the DuchessII chip [2]. However, twelve probe pads have been added to the chip, arranged in two columns. Figure 1 shows the probe pad location and numbering. The numbers correspond to the terminal names on the schematic in Figure 3.

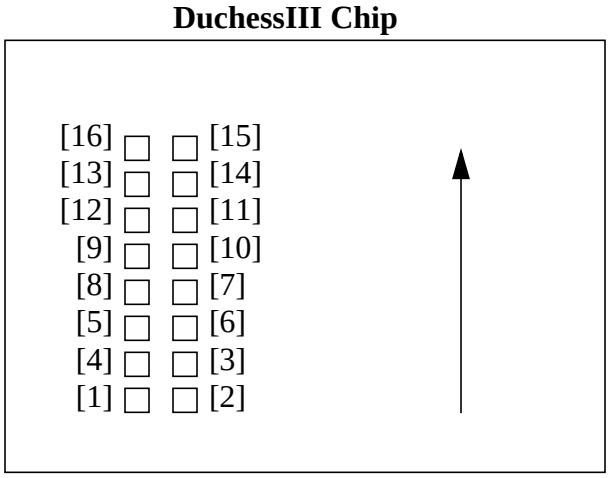

Figure 1: Probe Pad Locations and Numbering

Schematics

Only minor changes were made to DuchessII to make it DuchessIII. I will only show schematics that have changed since the DuchessII schematics [3].

Figure 2 shows the top-level schematic of the DuchessIII chip. The only change is the addition of the probe pads, shown by the ‘pT’, or probeTest cell.

Figure 3 is the probeTest cell. The terminals are the probe pads, and correspond to the numbering of the pads in figure 1.

Figure 4 is the ringGuts cell of the top-level schematic. The only change is the minor bug-fix rewiring described in [4].

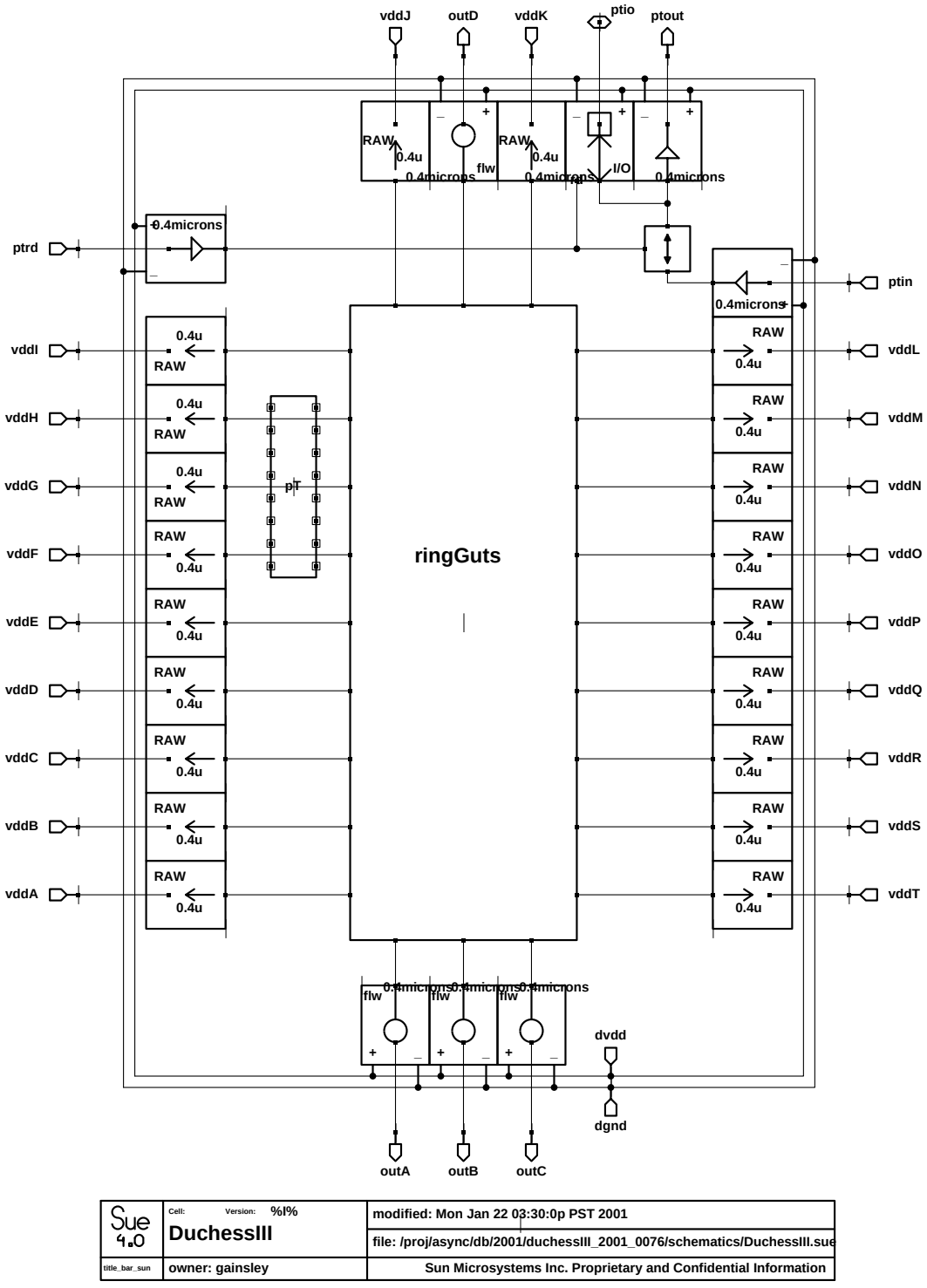

Figure 2: Top Level Schematic of the DuchessIII Chip

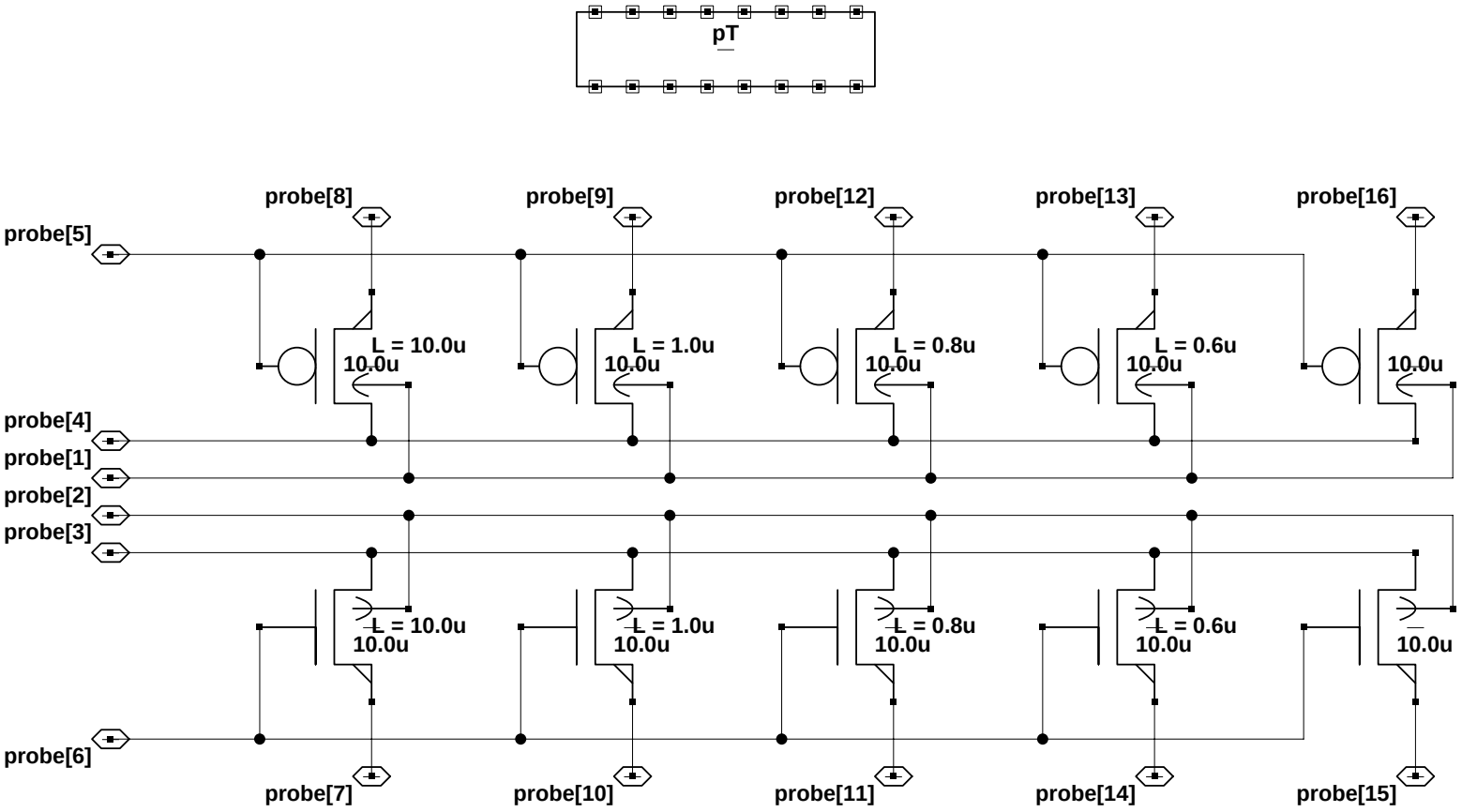

Figure 3: Schematic of probeTest Cell

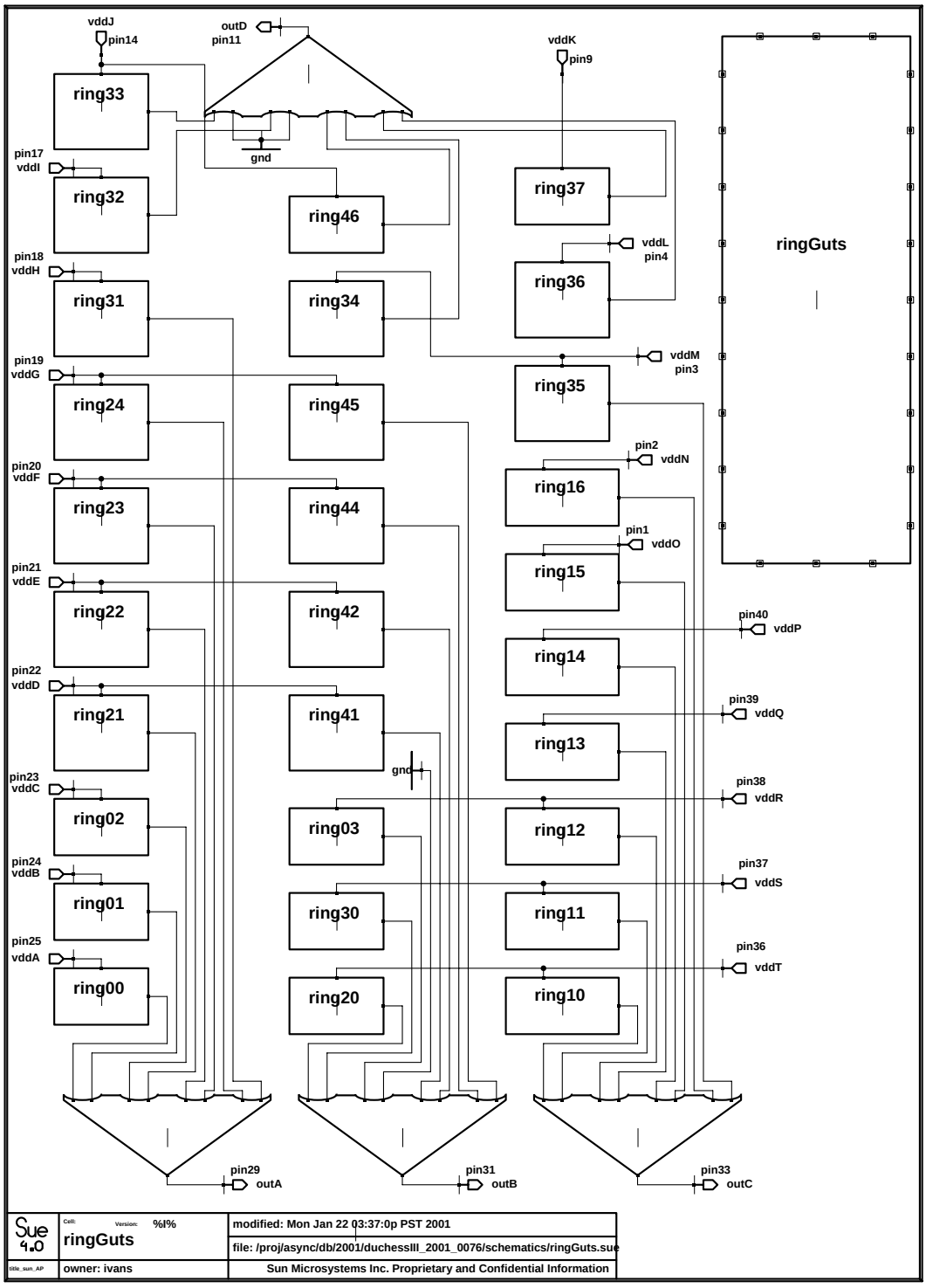

Figure 4: Schematic of ringGuts Cell

About the Authors

Ann Coulthard is an Engineering Project Coordinator for the Asynchronous Design Group at Sun Microsystems Laboratories. She does chip layout, designs and creates web pages, monitors patent progress, and oversees publications of group documentation. She first worked on layout for the Duchess Chip.

Ann has as B.S. degree in Psychology from the University of Washington and an M.S. degree in University Administration from Indiana University, Bloomington. Prior to joining Sun in 1996, she did freelance work in publishing and corporate administration. From 1982−1992, Ann was Assistant Director of the Ph.D. program in the Graduate School of Business at Stanford University. She held various student advisory roles in research departments at the University of Washington from 1976−1982.

Jonathan Gainsley is a member of the technical staff of the Asynchronous Design Group at Sun Microsystems Laboratories in Mountain View where he is working on designing asynchronous chips. His research interests include asynchronous chip design, tool development, layout issues, printed circuit board design, and testing.

Before joining Sun in 1999, Jonathan attended Harvey Mudd College in Claremont, California, where he received his B.S. degree in Engineering.

Jon Lexau received his B.S. degree in Computer and Systems Engineering from Rensselaer Polytechnic Institute in 1989 and his M.S. degree in Electrical Engineering from Stanford University in 1994.

From 1989 to 1993, he worked for the Amdahl Corporation designing high−performance mainframe CPUs. Since 1994, he has been with Sun Microsystems Laboratories in Mountain View, California working in the Asynchronous Design Group. His current areas of interest include high−performance asynchronous circuit design, analog circuit design, and digital signal processing.

Ivan Sutherland is Vice President and Fellow at Sun Microsystems. In addition to his own project in asynchronous system design, he helps Sun to adopt new technologies.

From 1980 until the firm was acquired by Sun, Dr. Sutherland was a vice president of the consulting firm Sutherland, Sproull, and Associates, Inc. Dr. Sutherland founded the Evans and Sutherland Computer Corporation (E&S) with Dr. David Evans and continues to serve as an active member of its Board of Directors. Dr. Sutherland has taught at Caltech, the University of Utah, and Harvard.

In the early 80s Dr. Sutherland's research centered on robots that walk. More recently his research program has involved new designs and design techniques for asynchronous digital systems. A "Theory of Logical Effort" resulted from this work. The asynchronous design style was the subject of Dr. Sutherland's 1988 ACM Turing Award Lecture, "Micropipelines," published in the June 1989 issue of *Communications of the ACM*. Dr. Sutherland was the 1988 recipient of this award.

Dr. Sutherland received his Ph.D. degree from MIT in 1983, following an M. S. degree from Caltech, and a B.S. degree from Carnegie Tech, all in electrical engineering. He holds honorary degrees from Harvard, Caltech, University of Utah, and the University of North Carolina. Dr. Sutherland is a member of the National Academy of Sciences and the National Academy of Engineering. In 1996, he won the prestigious Smithsonian Price Waterhouse Information Technology Leadership Award for Lifetime Achievement. He was chosen by the IEEE to receive their John Von Neumann Medal in 1998. Dr. Sutherland is author of 29 patents, as well as numerous publications and lectures.