Ultralow Power 80 Gb/s Arrayed CMOS Silicon Photonic Transceivers for WDM Optical Links

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***Abstract*—Silicon photonic interconnects offer a promising solution to meeting the ever growing demand for more efficient I/O bandwidth density. We report an ultralow power 80 Gb/s arrayed silicon photonic transceiver for dense, large bandwidth inter/intrachip interconnects. Low parasitic microsolder-based hybrid bonding enables close integration of silicon photonic array devices optimized on a 130 nm silicon-on-insulator CMOS platform with CMOS very large scale integration circuits optimized on a 40 nm silicon CMOS platform to achieve unprecedented energy efficiency. The hybrid CMOS transceiver consists of eight 10 Gb/s channels with a total consumed power below 6 mW/channel. The eight-channel wavelength division multiplexing transmitter array using cascaded tunable ring modulators demonstrated better than 100 fJ/bit energy efficiency for 10 Gb/s operation excluding the laser power and tuning power, while the eight-channel receiver array using broadband Ge p-i-n waveguide detectors show sensitivity of better than -15 dBm for a bit error rate of 10^{-12} at a data rate of 10 Gb/s with energy efficiency of better than 500 fJ/bit.**

***Index Terms*—Optical communications, optical interconnections, optical receivers, optical transmitters, silicon photonics, transceiver array.**

I. Introduction

CONTINUING to scale the performance of computer systems within reasonable power constraints requires increasing total system parallelism. The number of processors per chip and the chips per board must all steadily increase in order to grow the aggregate computational power, thereby raising requirements for aggregate interconnect bandwidth across the entire system. At the processor level, multicore architectures have enabled continued performance growth, even as clock rates have stopped scaling. Consequently, as shown in Fig. 1, designers have been pushing the I/O bandwidth of general purpose multicore processors and commercial field-programmable gate arrays (FPGAs) to follow Moore's Law scaling, doubling every two years to maintain balanced systems [1]–[8]. Given that such chips already require 2–5 Tb/s, it is extremely challenging to maintain such scaling using traditional electrical solutions. Transmission line driver technologies have achieved impressive results; state-of-the-art commercial electrical links recently demonstrated 28 Gb/s per channel, 8.82 pJ/bit energy efficiency, and 35 Gbps/mm^2 bandwidth per unit area [9]. The many on-going research and academic efforts further pushing these aggregate bandwidth and energy targets have found the design space to be tightly constrained; however, significant improvements are nonetheless necessary to keep up with integration scaling trends. Projecting forward using the metrics above, 20 Tb/s of I/O bandwidth would consume 90 W and 285 mm^2. Higher data rates will reduce the number of links, but will need more equalization and noise cancellation due to channel loss, thus increasing power and area. It is not clear that electrical links can be denser and more power efficient even with more advanced CMOS technology node. In addition, error encoding may also be needed for low bit error rate (BER), resulting in increased link latency. These, and other considerations, thus motivate a need for an interconnect technology with low power, low latency, and high bandwidth density.

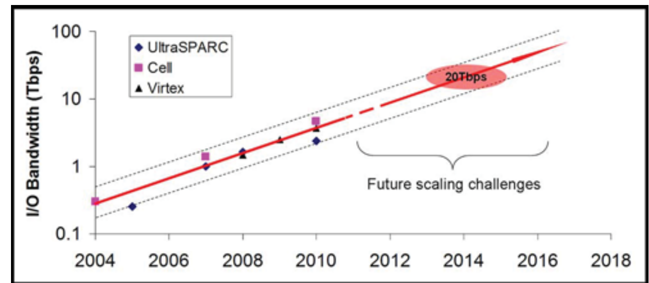

Fig. 1. I/O bandwidth scaling of general purpose processors and commercial FPGA chips.

Silicon photonic interconnects offer a promising solution to help meet these demands [10]–[12]. Many different inter/intrachip architectures have been proposed to exploit these interconnects [13]–[15]; in particular, by using optical proximity communication [16]–[18], photonic networking can allow a collection of discrete chips to function as a logically contiguous piece

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Fig. 2. Conceptual view of WDM interconnects using hybrid-integrated silicon photonic transceivers.

of silicon. By seamlessly scaling silicon beyond its physical reticle limits, such a "macrochip" offers unprecedented computational density, energy efficiency, bisection bandwidth, and reduced message latency [19].

A low-power wavelength division multiplexing (WDM) photonic link is key to achieving energy-efficient and high-bandwidth interconnects for macrochip and other system architectures. Such a link must be built around arrayed low-power WDM transceivers. Using high-density microsolder bumping technology [20], we first demonstrated single-channel low-power silicon photonic transmitters and receivers at 5 Gb/s with energy costs as low as 320 fJ/bit [21] and 690 fJ/bit [22], respectively. Later, using the same hybrid integration technique to bond improved silicon photonic devices to improved CMOS circuits, we showed single-channel 10 G transmitters and receivers with a record energy efficiency of 135 fJ/bit and 380 fJ/bit, respectively [23].

In this study, we report on the development of an ultra-efficient WDM ready 80 Gb/s CMOS photonic arrayed transceiver. We show optimized silicon photonics devices arrays built in a Luxtera/Freescale 130 nm silicon-on-insulator (SOI) CMOS platform, and hybrid-integrated with high-speed very large scale integration (VLSI) circuits optimized for low power using the TSMC 40 nm Silicon CMOS process.

II. 80 Gb/s Hybrid Integrated CMOS Photonic Array WDM Transceiver

Previous single channel demonstrations [20], [21], [23] have proven that hybrid integration is a valid approach for building efficient silicon photonic transceivers. It allows photonics and electronics to be independently optimized on different technology nodes for best-of-breed performance from each. Densely integrated multiple transmitters and receivers in an arrayed WDM transceiver can take advantage of the same technology. Using such hybrid integration, a conceptual view of WDM interconnects is shown in Fig. 2. Silicon photonic opto-electronic (OE) device chips are hybrid integrated with VLSI driver circuits as photonic bridges, which are then interconnected optically via a WDM optical routing layer using optical proximity coupling. The WDM multiplexer (Mux) and demultiplexer (DeMux) devices can be integrated together with the OE devices on the photonic bridges, or with the routing waveguides on the WDM routing chip.

To achieve an energy-efficient WDM silicon photonic transceiver array, we need high-speed OE device arrays with low parasitic loads and low-voltage operation, low-power, high-speed CMOS VLSI arrayed driver circuits, and high-yield low-parasitic integration [20].

A. Arrayed Cascaded Ring Modulators With Tuning

Silicon ring modulators offer compelling size and power characteristics. High-speed voltage modulation across a reverse-biased p-n junction embedded in the ring waveguide can be very efficient [21]. The highly wavelength-selective nature of the ring modulators, often considered a disadvantage, can be used to make compact WDM array transmitters by cascading multiple ring modulators along the same bus waveguide without significant interference. We designed eight slightly differently sized rings, each with a radius of approximately 7.5 μm, to accommodate eight wavelength channels at 1.6 nm channel spacing within one free spectral range (FSR) of 12.8 nm. To overcome the static resonance shifts due to fabrication tolerances, and dynamic drift from changes in ambient temperature, doped silicon-resistor-based thermal tuners are integrated into each modulator.

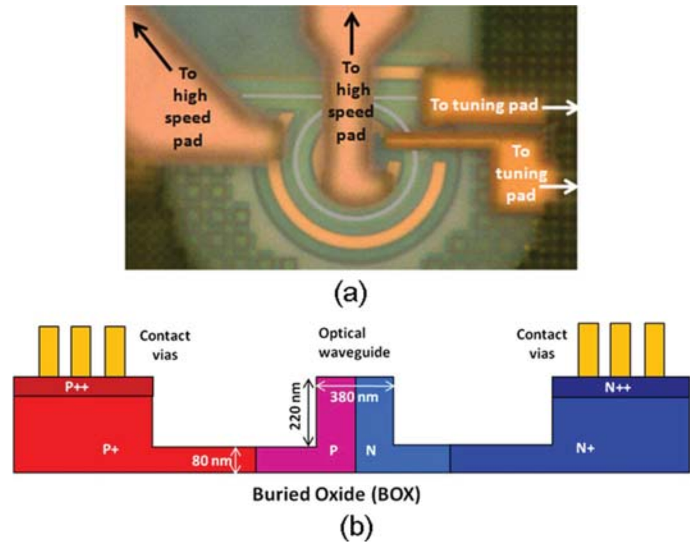

Fig. 3. (a) Ring modulator. (b) Cross section diagram of the ring waveguide high-speed section.

Fig. 3(a) shows a photograph of one fabricated ring modulator fabricated in Freescale's 130 nm HIP7_SOI process. 67% of the ring is doped as a p-n junction [1.5×10^{18} cm^{-3} doping, shown in Fig. 3(b)] for high-speed modulation, while the upper-right 25% is n-type doped as an Si resistor for thermal tuning. There are 2 μm wide isolation gaps, where the ring waveguide is undoped, between the p-n diode and the thermal-resistor sections. Multiple metal layers are used for the layout of electrodes. The ring waveguide is 380 nm wide, with 220 nm etch depth and 80 nm thick Si slab. We made the ring waveguide wider than the bus waveguide (300 nm wide) for smaller bending loss and better coupling phase matching. The doping densities in the p-n junction are determined by the tradeoff between the modulation efficiency and the speed.

The high-speed behavior of the ring modulator was examined using a circuit model extracted by curve-fitting the measured S11 data for both phase and amplitude. The circuit model and the extracted circuit values at 1 V are shown in Fig. 4. C_P denotes the capacitance between the electrodes through the top dielectrics, R_s and C_J model the current path through the reverse-biased p-n junction, $R_{\rm Si}$ and $C_{\rm OX}$ model the current path through the BOX and the Si handler.

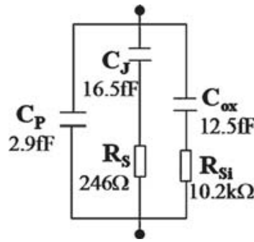

Fig. 4. Small-signal circuit model for the ring modulator with circuit values at 1 V reverse bias.

The modulator EO frequency response was tested using a microwave network analyzer, and a 3 dB bandwidth of $>$10 GHz was obtained at 1 V. The modulation bandwidth of the device is mostly subject to the photon lifetime limit, which is 12 GHz based on the measured quality factor.

B. Ge p-i-n Waveguide Photo Detectors

Ge p-i-n waveguide photodiodes (PDs), fabricated in Freescale's HIP7_SOI 130 nm CMOS technology with Luxtera's Ge-enabled optoelectronic process [24], have demonstrated exceptional performance. Such evanescent coupled Ge detectors are fabricated by selective epi growth of Ge on a 1.5 μm wide and 15 μm long multimode silicon waveguide, tapered from a 0.3 μm wide single-mode waveguide. These devices are very compact in area and have electrical bandwidths exceeding 12 GHz, room temperature dark current less than 3 μA at 0.5 V reverse bias, measured responsivity of $>$ 0.8 A/W for wavelength less than 1535 nm (which drops to about 0.7 A/W at 1540 nm, and 0.6 A/W at 1550 nm due to Ge band edge), and diode capacitance of only 10 fF [23]. Because a Ge waveguide PD has very broad optical bandwidth, eight identical PDs were designed into an array WDM receiver.

C. Photonic EO Device Array Layout

The photonic device arrays were optimized using a specialized process design kit developed at Luxtera. The floorplan of the chip is shown in Fig. 5(a). Eight ring modulators are cascaded along a shared bus waveguide, and each ring modulates a wavelength channel out of an eight-wavelength comb with 1.6 nm channel spacing within the 12.8 nm FSR. These rings are slightly different in size with nominal radius of approximately 7.5 μm. Eight Ge waveguide detectors, however, are arranged as a 1×8 array with separate waveguide because they are broadband devices. The photonic device array is laid out in a column with 250 μm cell pitch.

Grating couplers are used as the optical I/O interface, with a pitch of 250 μm to support optical testing using fiber arrays. To form a complete WDM link using such arrayed modulators and PDs, a WDM comb source or a wavelength Mux is needed to multiplex single wavelength sources together to drive the cascaded modulators, and a wavelength DeMux is needed to separate the wavelength channels before the PD array. We assume that the WDM Mux/DeMux devices [25], [26] can be integrated on the WDM routing chip as one possible option. Using the grating coupler interface, complete WDM links can be established between the transceiver bridges through a WDM routing chip equipped with matching optical I/O configuration, as the schematics shown in Fig. 5(b). One can also integrate the WDM Mux/DeMux devices directly with the OE devices on the bridge to simplify the routing chip as an alternative option.

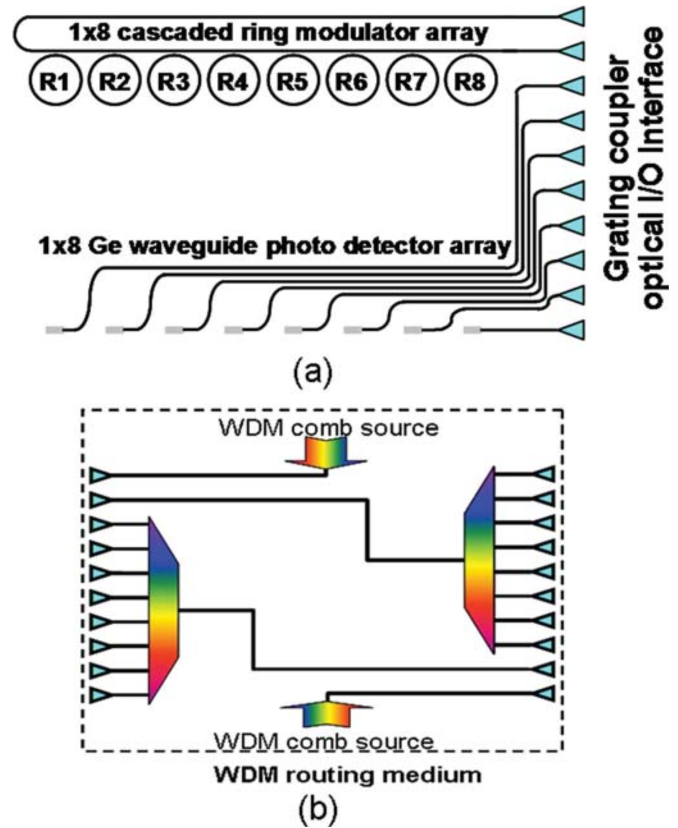

Fig. 5. (a) and (b) Arrayed photonic device lay out of an 80 Gb/s silicon photonic transceivers for WDM links using cascaded ring modulators, broadband Ge waveguide photodetectors, and gr ating couplers for optical I/O.

D. Low-Power VLSI Circuits

Low-power, high-speed VLSI circuits were developed in TSMC's 40 nm bulk CMOS node. As the circuit model indicates, the reverse-biased depletion ring modulator appears largely as an *RC* load to a CMOS driver. We use cascode drivers to modulate 10 Gb/s data on the cascaded rings with up to 2 V swing, as the circuits diagram shown in Fig. 6.

Pulse generators on the cascode devices activate them within a timing window designed to minimize $V_{\rm gs}$ and $V_{\rm gd}$ overstress during output transitions [27]. Each driver consumes a silicon area of only 120 μm^2. Sixteen copies of these compact modulator driver are arranged in a column with a pitch of 125 μm. For testing purposes, the modulator drivers can take data from either a common on-chip pseudorandom bit sequence (PRBS) generator or from an off-chip pin. The datapath, however, can selectively invert and/or delay that data stream at each individual modulator. This allows data bits at different experiments to be independent and thus enables more realistic device array testing. In order to simplify the on-chip digital circuitry, data are moved across the chip in two parallel "single-data-rate" 5 Gb/s streams and converted at the modulator driver into one "double-data-rate" 10 Gb/s stream.

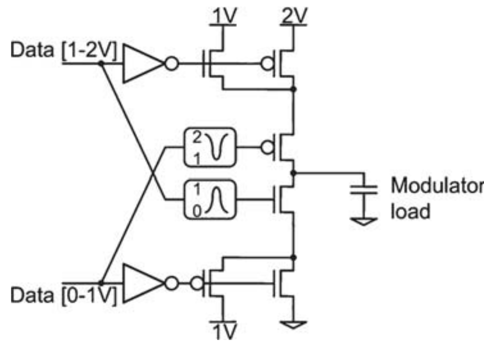

Fig. 6. Cascode modulator driver circuit.

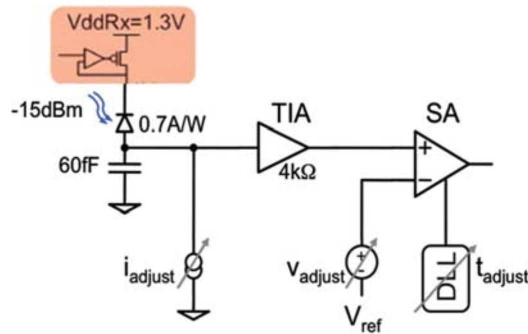

Fig. 7. Diagram of low-power receiver circuit with retiming and power supply regulator.

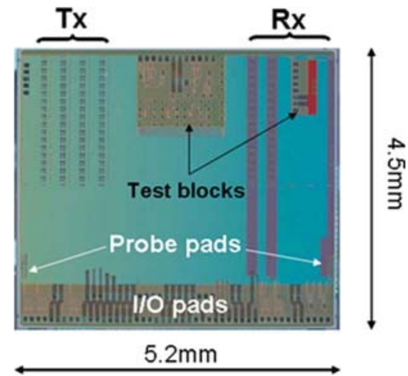

Fig. 8. Arrayed transceiver VLSI chip.

Tuning helps to align the ring modulators with their corresponding wavelength channels. To drive the silicon resistor heater built in each ring modulator, current-source-based tuning circuits with up to 6 mW output power to a 400 Ω resistor, and with 12-bit resolution, are also included in every modulator driver cell.

The low-power receiver [28], [29] is based on a transimpedance amplifier (TIA) followed by a strobed sense-amplifier (SA). The SA, more efficient than traditional limiting amplifiers, restores the received signal to full CMOS voltage levels. As the circuit diagram depicts in Fig. 7, the receiver includes a clock-phase recovery circuit, based on a delay-locked loop (DLL), to properly clock the SA. The receiver also includes a facility to adjust the input current so that the TIA output swings symmetrically around the SA switching threshold, so that SA can correctly determine whether the data were a “0” or a “1.” Because SAs suffer from intrinsic mismatch and comparison inaccuracy, the receiver implements offset compensation.

Setting the DLL for appropriate clocking of the SA, setting the input level to center the SA input around the voltage threshold, and setting two distinct offset compensation circuits requires a total of four digital-to-analog converters (DACs) in the receiver. Digital finite-state machines drive and set these four DACs during periodic recalibration of the optical link, once every millisecond or so.

The three-stage TIA is designed for a gain of 4 kΩ at a bandwidth of 7 GHz, assuming an input capacitive load of 60 fF that include both PD and hybrid bonding pads. This enables operation at -15 dBm average optical input power with a worst case extinction ratio (ER) of 3 dB and a PD responsivity of 0.7 A/W, and targeting a signal-to-noise ratio sufficient for a BER of 10^{-12}.

Each low-power receiver consumes silicon area of less than 8000 μm^2 excluding the bonding pads. Bonding pads are smaller than the circuits and may be placed directly above the CMOS circuits. Sixteen copies of such receiver circuits are arranged in a column with a pitch of 125 μm. To minimize the supply noise and crosstalk from neighboring channels in an array, a linear regulator on the power supply of each receiver offers low-frequency noise rejection better than 30 dB [29].

The VLSI test chip was fabricated in TSMC’s 40 nm bulk CMOS technology. Its organization, in Fig. 8, shows four transmit (TX) columns of 16 modulator drivers each, as well as three columns arrayed receivers instantiated [29].

For our arrayed transmitters and receivers, capacitive and inductive crosstalk between array sites is small. Traditional electrical links, which employ large soldered structures to carry signal currents, can suffer from significant crosstalk, particularly from high-current transmitters placed in close proximity to sensitive low-swing input receivers. In such circumstances, capacitive coupling between soldered pins, plus capacitive and inductive coupling between transmission lines, can generate noise that overwhelms the sensitivity limits of the receiver circuits. In our case, however, the transmitters drive small capacitive loads of only a few tens of fF, over small (25 μm) hybrid bonding pads, so the circuits are small and do not couple strongly to each other. Also, the waveguides carry no net electrical current and generate neither inductive loops nor injected capacitive noise. We saw no effects of running many other transceivers while measuring one selected channel.

However, noise may still couple between receivers, or from transmitters to receivers, by means of the power supply. For a TIA aiming at -15 dBm sensitivity, a power supply transient can easily swamp out the received signal: in fact, simulations show the TIA has a nearly 18 dB gain from power supply to output. To compensate, our test chip employs power supply regulators on the TIA, on re-timing DLLs, and on DACs used for receiver calibration. The regulators, based on a differential amplifier, show in excess of 18 dB of broadband noise rejection (simulated) across all process corners, and hence just cancel the TIA’s supply noise gain. In order to further avoid coupling noise between the TIA and the timing circuits, we use separate power supply regulators for these different blocks.

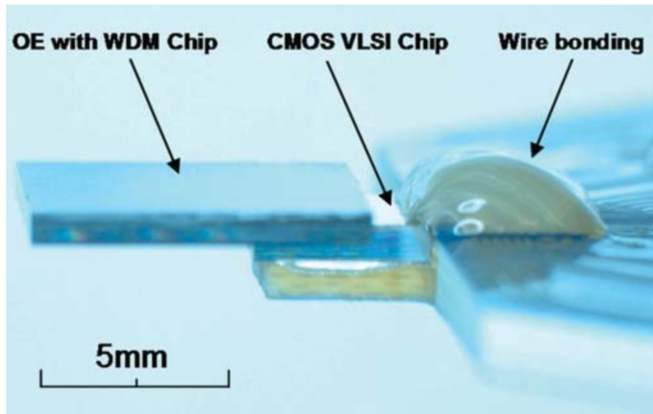

Fig. 9. Hybrid integrated WDM transceiver on a test PCB.

E. Hybrid Integration

Hybrid integration [30] allows photonics and electronics to be independently optimized on different technology nodes for best-of-breed performance from each. Employing a special under-bump-metallization solution and microsolder bumps fabricated through lithography, metal deposition, and liftoff, we developed a low-parasitic microsolder bump technology compatible with 40 nm bulk CMOS using extreme low-κ interlayer dielectrics [31]. 25 μm bonding pads are used for achieving the targeted less than 20 fF hybrid integration capacitance.

OE device chips and VLSI chips are flip-chip bonded using thermal compression to collapse the microsolder bumps. The hybrid chip assembly is then die-attached and wire bonded to a carrier substrate to provide power, clocking and digital data I/Os needed for a complete transceiver. Fig. 9 shows a photo of the complete arrayed silicon photonic transceiver, with the photonic device and VLSI hybrid chip assembly wire-bonded to a test PCB.

III. WDM Transceiver Performance

A. Arrayed WDM Transmitter Performance

A fiber array enables characterization of the transceiver performance through the grating coupler I/O interface. Since the on-chip silicon waveguide only supports TE polarization, the source laser light was polarization controlled and polarization maintained fibers were used to match the waveguide polarization. As discussed earlier, deep optical trench etching was used to enable ultracompact ring design, which unfortunately made the fiber grating coupler performance worse. A $\sim$5 dB coupling loss was measured through the fiber/grating coupler interface. Using optimized grating trench depth [32], and introducing backside mirror [33], such coupling loss is expected to be less than 1 dB. For thermal stability, a room temperature passive copper heat sink was attached to the photonic device chip. Fig. 10(a) shows the "through" spectra of the cascaded ring modulators with -5 dBm optical power in the input fiber. As expected, due to manufacturing tolerances, the ring resonances are not evenly distributed on the designed 1.6 nm channel spacing. However, it is encouraging to see that the resonances of the cascaded rings (designed using slightly different radius for each ring) in close physical proximity are separated in order. Using

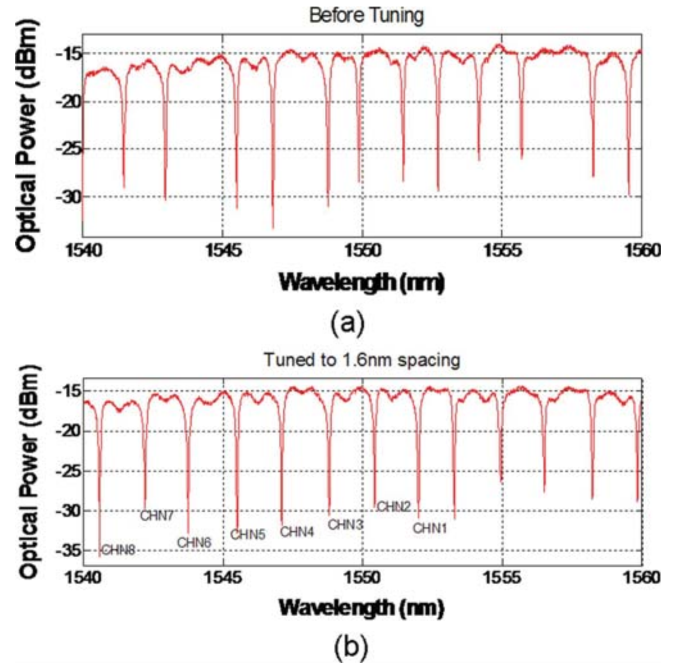

Fig. 10. Through spectra of the cascaded ring modulator array (a) before and (b) after tuning.

the built-in thermal tuners, we were able to position the ring modulator resonances to a 1.6 nm channel spacing as intended [see Fig. 10(b)], overcoming any resonance shifts due to fabrication variances [see Fig. 10(a)]. The resonance shift needed were 0.543, 0.577, 0.043, 0.346, 0.005, 0.8, 0.77, and 0.588 nm for CHN1 to CHN8 as labeled in Fig. 10(b), corresponding to individual ring turning power of 2.74, 2.92, 0.22, 1.75, 0.03, 4.09, 3.89, and 2.97 mW, respectively.

The built-in silicon resistor thermal tuner was driven by the 12 bit digital current source. The tuning capability of such a tuner is shown in Fig. 11. The resistance of the doped resistor was measured about 600 Ω, slightly larger than the design target of 400 Ω, which limits the maximum power that can be delivered to the heater to be about 4 mW. As indicated by Fig. 11, maximum tuning of only about 0.8 nm can be achieved with 4 mW of tuning power. Using thermal engineering by trench isolation and undercut [34], or substrate removal by back side etch pit [35], up to 20 times tuning improvement have been demonstrated. With improved tuning efficiency, we will be able to position a ring resonance anywhere within one FSR with less than 4 mW of tuning power.

With the modulators tuned to the correct channel spacing, high-speed transmission performance was tested by injecting WDM continuous wave wavelengths into the input bus waveguide with about 1 mW of in-waveguide optical power, and driving the modulators with a 10 Gb/s PRBS stream generated on-chip. Limited by WDM laser source availability, a single tunable laser source was used to test different wavelength channels sequentially with electrical modulation turned on for all rings. An erbium-doped fiber amplifier (EDFA) was used to amplify the modulated optical signal before an Agilent reference receiver. The 10 Gb/s modulated optical "eyes" of the eight WDM transmitter channels are presented in Fig. 12 and show dynamic

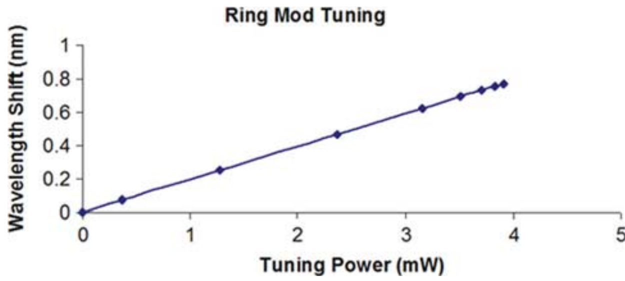

Fig. 11. Ring modulator resonance shift in wavelength driven by the digital current source.

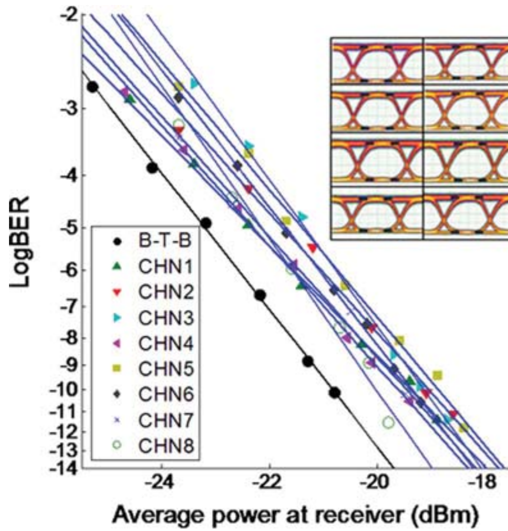

Fig. 12. Measured received power penalty using a reference InGaAsP-based receiver at 10 Gb/s for the cascaded ring transmitters with the inset picture showing the optical eye diagrams of eight WDM channels.

ER ranging from 5.6 to 8 dB for the same "ON" state loss of -4 dB (excluding the fiber to waveguide coupling loss). The plots in Fig. 12 indicate a received power penalty of 1–2 dB for the WDM array transmitter when compared to an Agilent lightwave transmitter with 12 dB ER, mostly attributable to the ring modulator array's imperfect dynamic ERs.

With an array spacing of 250 μm, we expect little optical crosstalk. Electrical crosstalk impairment was measured by measuring the "eye" closure penalty on a channel with and without all the neighboring channels turned on as aggressors. The channels in the middle of the array suffer from the most electrical crosstalk. The measurement result of one such channel, CHN5, was shown in Fig. 13. The measured received power penalty with crosstalk is about 0.5 dB better than without crosstalk at BER of 10^{-12}. This is mostly due to the error in average power measurements. The EDFA output power fluctuates about ± 0.2 dB. In addition, we had to switch the fiber connection between an optical receiver and a power meter to measure the average power. The fiber connection brings in additional uncertainty about ± 0.1 dB. We, therefore, believe that the crosstalk is negligible.

The power consumption of the modulators was measured directly from the driver supply voltage and current. The modulation power was measured to be 0.94, 0.71, 0.70, 0.70, 0.92, 0.68, 0.66, and 0.91 mW, respectively, for the 8 transmitters. A record high efficiency of less than 100 fJ/bit per channel is achieved.

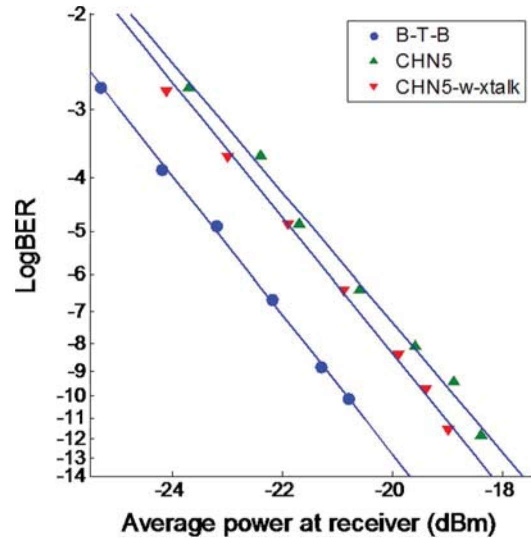

Fig. 13. Worst case channel crosstalk induced "eye" closure penalty of the arrayed WDM transmitters.

B. Arrayed Receiver Performance

The arrayed receiver used multiple individual clocks: each receiver employed its own DLL to phase-align its SA strobe to the incoming data stream. The array was tested using a modulated 10 Gb/s PRBS $(2^{31} - 1)$ input optical signal from an Agilent lightwave transmitter. An on-chip PRBS error checker measured the receiver performance. The receiver circuit allows a test interface to externally set both the SA's decision threshold voltage and the DLL's phase delay. By sweeping this voltage and time, and evaluating the BER for each (voltage, time) pair, we obtain the receiver eye diagram. The receiver also offers a test mode with direct measurement of the average input photocurrent. Fig. 14 shows the eight measured receiver eyes with 24 μA of average input photocurrent at wavelength of 1535 nm. The vertical axis of each "eye" represents the sense amplifier threshold voltage range of 160 mV, while the horizontal axis represents the timing of one UI or 100 ps. The white opening in the middle of the eyes represents a BER under 10^{-12}. Because the error counter used for the on-chip error checker has only 8 bits, and a 20 min error counting time period was used to make sure credible measurement of BER under 10^{-12}, BER above 2×10^{-11} would overflow the error counter and processed as the black region in each "eye." The abrupt changes around the edge of the "eye" opening are also due to such effect. Assuming a PD responsivity of 0.8 A/W, all the receivers achieved a sensitivity of better than -15 dBm for 10 Gb/s at BER of 10^{-12} without optical crosstalk from WDM channels.

With no WDM DeMux integrated, channels spacing of 250 μm, and waveguides laid out with big enough spacing to minimize optical crosstalk, we believe that electrical crosstalk dominates. We measure the crosstalk impairment from neighboring channels for this study. We reduce the average input optical power of one channel in the middle of the array to about -17 dBm at the detector such that the receiver "eye" has

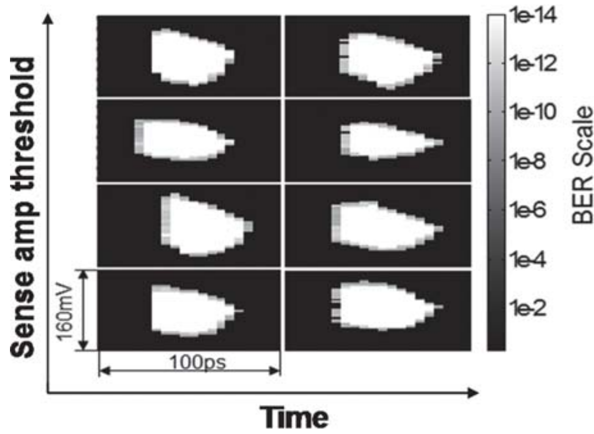

Fig. 14. 10 Gb/s eye diagrams of eight receiver channels measured one channel at a time using the on-chip PRBS error checker.

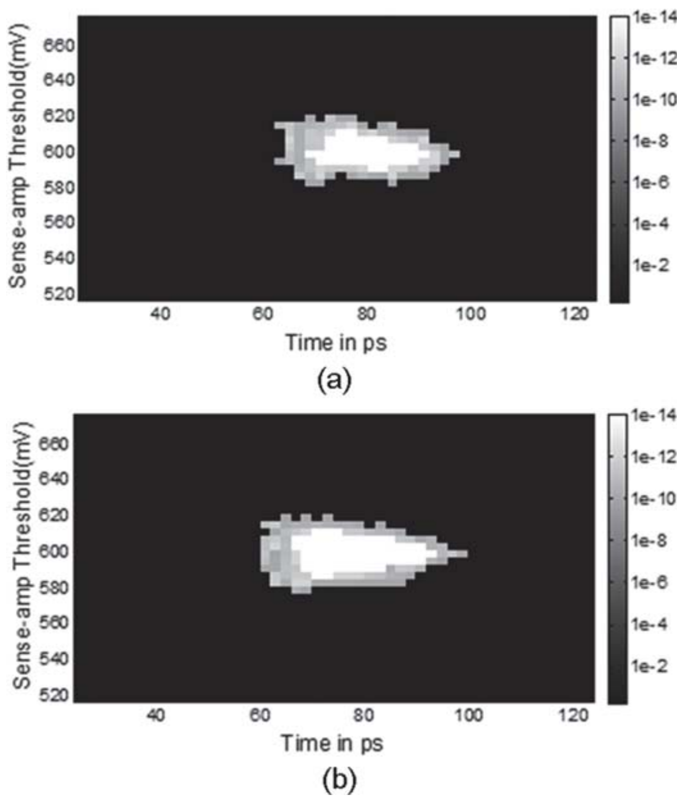

Fig. 15. Measured receiver "eye" at 10 Gb/s with minimum opening at BER of 10^{12} (a) before and (b) after crosstalk aggressor channel was turned ON.

minimum opening at BER of 10^{-12}, as shown in Fig. 15(a). We then turn ON the crosstalk aggressor channel with about -15 dBm average on the detector to see its impact on the measured channel "eye" opening. As the measured result shown in Fig. 15(b), the "eye" opening is actually slightly better than the "eye" with the neighboring channel turned OFF. We believe that such small difference is most likely due to the power fluctuation during the hours long measurement, and the crosstalk in the arrayed receivers is negligible.

Similar to the transmitter measurement, the receiver power was also measured directly from its supply voltages and currents. The measured power consumptions are 4.52, 2.72, 2.6, 2.92, 3.2, 2.84, 2.72, and 4.04 mW, respectively, for eight channels. At less than 500 fJ/bit per channel, it is the most energy efficient receiver array with retiming ever reported [22], [23].

IV. Conclusion

Energy efficiency and bandwidth density of interconnects are becoming the most critical issues for computing system scaling. While pure electrical solutions are running out of tricks in the tool box, and struggling to meet the need of future system scaling, WDM optical link solutions based on silicon photonics offer a promising alternative with potentially orders of magnitude improvement in both bandwidth density and energy efficiency.

Low-parasitic hybrid integration again proves to be a viable approach to enable high energy efficiency for dense silicon photonic interconnects, with which an arrayed silicon photonic transceiver was successfully developed for use in 80 Gb/s WDM silicon photonic links by employing a cascaded ring modulator array with thermal tuning and a Ge waveguide PD array, optimized and cointegrated using the Luxtera/Freescale 130 nm SOI CMOS process. A full accounting of the power of a silicon photonic link, particularly when being considered as a replacement for a digital electronic link, must include transmitter and receiver functionality, link retiming requirements, additional supply regulation needs, as well as tuning requirements and the required laser power. In the transceivers described in this paper, we have incorporated the first three functions. Low-power, high-speed VLSI circuits were designed in the TSMC 40 nm bulk CMOS process. Excluding tuning and laser power, the 80 Gb/s arrayed transceiver consumes a record-low power of less than 6 mW per channel. In other work, we have shown that the tuning power for cascaded ring devices similar to those described here, with appropriate back-end CMOS processing [35] can be reduced to less than 0.5mW per microring in fully processed CMOS wafers with 193nm lithography [36]. To complete the power accounting, a final consideration is to develop suitable tunable optical sources with high electrical-to-optical conversion efficiency.

The transceiver circuits reported here, together with input–output grating couplers for power and I/O, provide an I/O density of 700 Gbps/sq·mm. Through the optical interface using grating couplers, the highly efficient hybrid WDM transceiver serves as a promising key element enabling various intra/interchip networking applications with compelling bandwidth, density, and energy efficiency advantages.

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