A Package Demonstration with Solder Free Compliant Flexible Interconnects.

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Abstract.

Flexible, stress-engineered spring interconnects is a novel technology potentially enabling room temperature assembly approaches to building highly integrated and multi-chip modules (MCMs). Such interconnects are an essential solder-free technology facilitating the MCM package diagnostics and rework. Previously, we demonstrated the performance, functionality, and reliability of compliant micro-spring interconnects under temperature cycling, humidity bias and high-current soak. Currently, we demonstrate for the first time the package with the 1st level conventional fine pitch C4 solder bump interconnects replaced by the arrays of microsprings. A dedicated CMOS integrated circuits (ICs) have been assembled onto substrates using these integrated microsprings. Metrology modules on the ICs are designed and used to characterize the connectivity and resistance of each micro-spring site.

Introduction.

Current trends and progress in microelectronics continue to be enabled by chip packaging technologies. As die sizes, I/O count, and power densities grow, significant challenges develop in connecting chips and their first-level packages. Additionally, ongoing developments in 3D integration and multi-chip modules (MCMs) present new opportunities for novel I/O technologies that improve performance despite severe dimensional constraints.

Electronic packaging based on stress-engineered spring interconnects [3] can potentially improve chip testing, rework, and mechanical compliance. With conventional flip-chip bonding, the rigid solder reflown microbumps can cause package failure due to excessive shear, as there is a significant CTE mismatch between a silicon integrated circuit (IC) die and the package substrate. Spring-based interconnects, on the other hand, are flexible and compliant; they present a stress-free, lead-free packaging solution for connecting an IC die to ceramic and organic substrates. They also provide rematable connections to enable a reusable, reworkable MCM platform where an ability to separate non-functional and functional die, *i.e.* identifying known good die (KGD), is key to enhancing assembly yield.

The microsprings are lithographically-defined metal cantilever beams with large initial stress gradients. When a spring is released from the substrate, the stress relaxes and its tip lifts out of the substrate plane, becoming a 3D-compliant interconnect that can be compressed against a metal pad to form an electrical contact. Previously, we have realized micro-spring prototypes that meet the stringent electrical and mechanical demands of a typical modern, high-performance microprocessor package; each spring presents <100 mΩ per connection and >30 μm of compliance; spring reliability was also confirmed under 0 – 100°C temperature cycling, 85/85 temperature humidity bias, and a high-current soak [1-2].

The micro-springs are lithographically-defined metal cantilever beams which self-assemble on the wafer level during fabrication. Beams are sputter deposited with large initial stress gradients. When a spring is released from the substrate, the stress relaxes and its tip lifts off of the substrate plane, becoming a 3D-compliant interconnect that can be compressed against a matching metal pad to form an electrical contact. In previous work we have demonstrated high density gold-gold pressure contacts at 6μm for a laser bar array, and at 20μm pitch for an LCD driver chip [4]. Soldered springs have also been demonstrated for chip to board applications such as memory [3]. The fabrication approach has also been used to build high quality factor coils [5], large angle MEMS actuators [6], and tall tip atomic force microscopy tips [7].

We have transferred the interconnect spring technology onto two types of standard electronic substrates. Fine-pitch substrates with ceramic or organic built-up layers have been populated with high-density arrays of micro-springs; these provide electrical connections to one or more silicon CMOS ICs housed within the package. Each IC contains metrology circuits that allow us to measure the connectivity and resistance of each individual spring connection.

In this paper, we report on the development of the microfabrication process that for the first time enables the integration of compliant, fine pitch microspring interconnects with ceramic and organic substrates. We show a semiconductor IC packaged onto a substrate using these interconnects, describe assembly details, and present the metrology results.

1. Micro-spring processing.

Fabricating thin film structures onto ceramic requires careful surface preparation. The spring fabrication process uses sputtering and plating of thin films as well as photoresist based lithography, so smooth substrate surfaces are required. The substrate is built out of 16 alumina layers with tungsten conductors arrayed at 180μm pitch on the chip side and at 1 mm pitch on its BGA socket side. The substrates are designed to package two active chips “bridged” with a third one establishing that establishes capacitive proximity

communication (PxC) between the first two [9]. The substrates' dimensions and initial surface properties have been described earlier [9]. The manufactured ceramic is initially not fully compatible with thin processing, because the solder bumps and under bump metallurgy (Ni/Au) are too tall while the alumina top surface is too rough and non-planar. To planarize and smooth the surface out, the substrates are polished, resulting in a local roughness of less than 0.1 um and step heights of <0.5µm near tungsten vias. However, the original granularity of the ceramic substrate remained, consisting of many 2 µm deep holes. To address this non-uniformity and to ensure adequate metal thin film adhesion, a spin-on dielectric, benzocyclobutene (BCB), is applied to the substrate for planarization. Figure 1 displays a fragment of the pre-BCB planarized ceramic surface after polishing step. The sequence of fabrication steps is demonstrated in Figure 2.

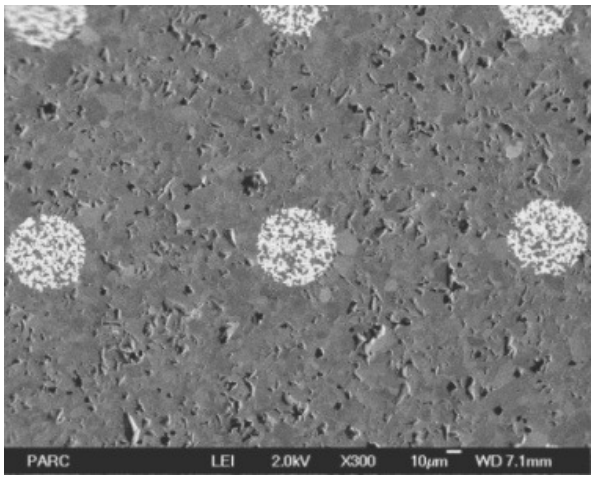

Figure 1. SEM micrograph of the top ceramic substrate surface after polishing. Tungsten filled vias are shown on the 180 µm pitch.

Next, photoresist lithography and etching is used to open up the BCB dielectric over the tungsten vias (Figure Figure 2 b). The substrate is then placed in a sputtering tool to deposit a release layer (Ti) and spring metal stack (Au-MoCr-Au). The stress in the MoCr is controlled such that there is a vertical gradient of intrinsic stress ranging in magnitude from a GPa compressive to a GPa tensile. The spring metal stack is patterned with photolithography to form the spring anchor, body and tip (Figure Figure 2 c). Another photoresist mask is spin-coated and patterned to define spring release regions. A selective wet etch is then used to extract the release titanium layer underneath the spring and allow the stress to relax, so that each spring lifts its body out of the deposition plane and self-assembles. Finally the springs are plated with additional metals (Au) for extra strength and conductivity (Figure 2e).

The spring contacts are arranged on a 180µm × 180µm pitch array (Figure Figure). The pattern matches a dedicated test chip specially designed for contact resistance measurements and spring yield as well as proximity communication (PxC) experiments. The substrate has a cavity to house "bridge" chips and facilitate future proximity packaging demonstrations. Achieving high yield lithography around this cavity requires careful attention to the photoresist coating uniformity.

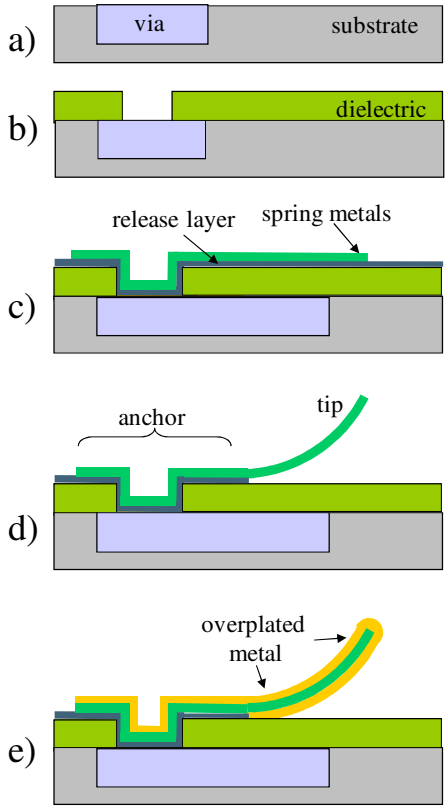

Figure 2 . Micro-spring fabrication process flow.

Close-up images of the contacts show the circular tungsten filled via underneath the rectangular spring anchor (Figures 4, left and right). The position of the tungsten filled vias is not registered well on the 180µm pitch array because of the thermal runout inherent in the substrate co-firing fabrication process. Tungsten filled vias are visible to the left side of the spring anchor (Figure 4 left). Each contact site is a dual micro-spring structure. Each spring is 100 µm long, 30 µm wide and 3.5µm thick. The tip is originally 45 µm above the surface.

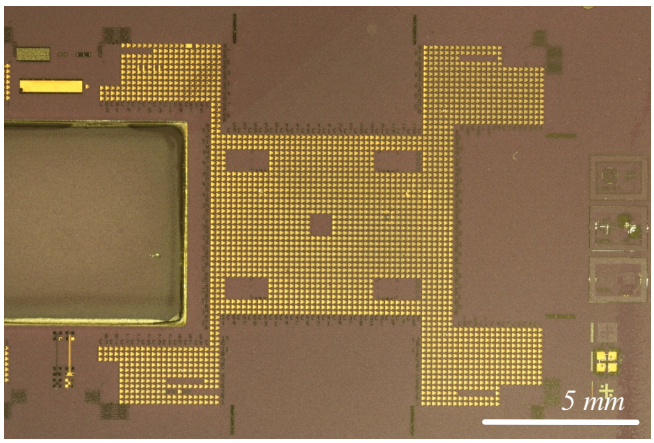

Figure 3. Optical microscope micrograph of the array of gold plated micro-springs fabricated on a ceramic substrate.

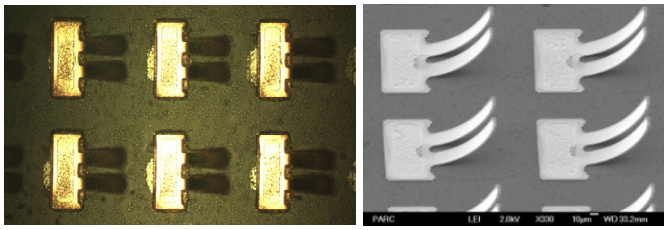

Figure 4. Left: optical image of the top view of the processed micro-springs on ceramic substrate. Right: SEM micrograph of the micro-springs showing lifted-off dual micro-springs on every via site.

2. Package Assembly.

An active IC was flip chip assembled onto a ceramic substrate with springs to form the package (Figure 5). The silicon IC has incorporated four corner etch pits each housing a precision spacer sapphire balls. In previous work, matching pits in another substrate were used to enable very precise 3D alignment of chips (with tolerances below +/- 2 µm) while only requiring coarse (>25 µm) assembly precision [1]. In this demonstrated package, the ceramic substrate does not have matching pits, so the balls are used only to establish accurate gap. A ball diameter of 135 µm was selected to reside on the bottom of the 95 µm deep etch pit. By design the gap between the ceramic substrate and flipped IC top surface is targeted at uniform 20 µm, For this spring design, this corresponds to a spring compression of 25µm. Previous four-wire measurements of resistance versus compression suggest that this puts the spring well into the resistance plateau region where the resistance is insensitive to amount of further compression [7]. The resistance has been verified to be uniform (<10 mΩ variation) for any gap below 35 µm.

The flip chip optics and assembly process need to provide the x-, y- alignment. The IC contact pads are 80 µm with a 70 µm passivation window. The spring pair is 60 µm wide, so the alignment error should be less than +/- 5 µm to ensure that both tips are entirely situated on the pad. If one of the two tips is half off the pad (Figure

Figure), the effect tip-pad interface area will decrease by 25%, but the overall resistance increase should be <10 mΩ. This estimate is based on previous modeling of the contact which suggested that the sum total of the resistance due to the tip-pad contact area of both tips is ~10-40 mΩ. The total spring contact resistance is 70-100 mΩ, consisting of the sum of contributions from the tip-pad area, spring body, spring anchor and pad spreading, suggesting this misalignment increase the total resistance by <10% [7]. Future packages can be designed to readily provide improved alignment tolerances.

After aligning the springs to the IC pads, the IC is lifted and compressed at least three times to pre-scrub the tip and pad surfaces. This has been found to lower the resistance 5-20 % [7]. Before the final compression, adhesive if placed on the edges of the packages and UV cured from the edge of the chip. Thermal cures have previously been used for spring assemblies and may be implemented in future assemblies. Figure Figure shows completed packages.

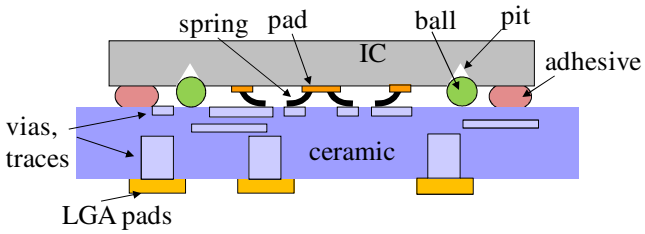

Figure 5. Schematic cross-section of the assembled package.

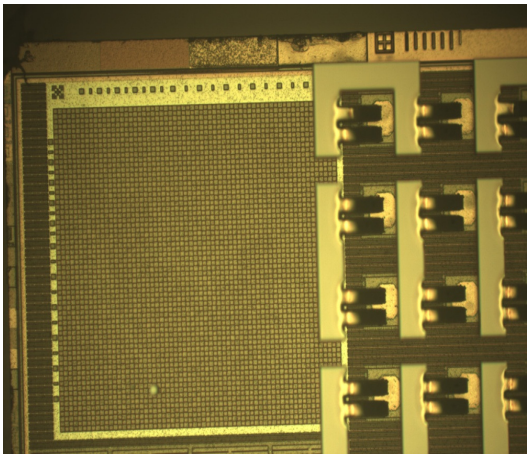

Figure 6. Top view image of spring tips aligned and assembled to the IC pad chip. In this practice assembly the springs were first fabricated on the glass substrates, enabling visual inspection. The springs are misaligned by 15-20um in the y-direction, causing one of the two tips to land outside of the pad window, which should increase the total resistance by <10%.

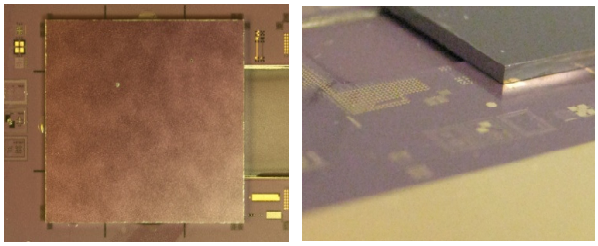

Figure 7. Assembled packages displaying attached IC chip on the ceramic substrate. Left: top view. Right: angled view.

3. The Test IC Chip.

To study the yield and electrical characteristics of microspring (and other types of) connections, we built a test chip with metrology circuits that let us characterize the thermal, electrical, and mechanical properties of various packages [10]. If used with a proper cooling and power delivery system, the test chip can also dissipate up to 355W of power at 1.8V; this simulates the thermal profile of a typical high-performance microprocessor, and allows us to study the performance of packages under these extreme thermal loads. For this reason, the test chip was code named the “Package Killer” chip (PKIC). Note, however, that we did not exercise

the full power dissipating capability of the PKIC, as the microspring test setup was not designed to deliver high power or remove the resulting heat.

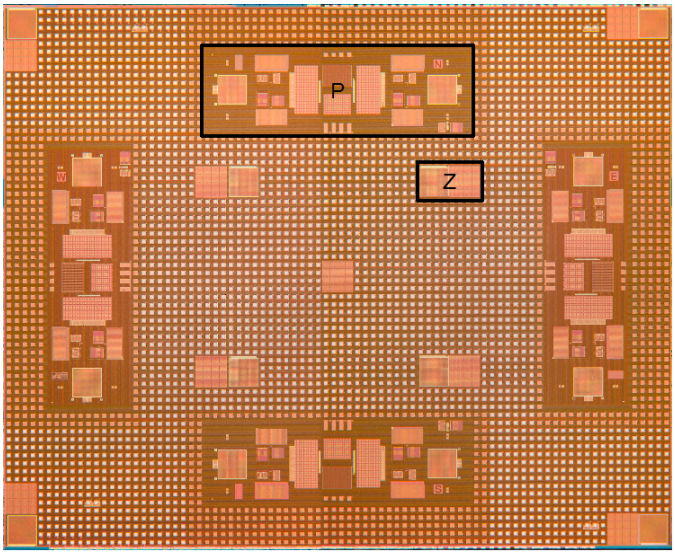

Figure 8. Die photo of the Package Killer IC (PKIC).

The PKIC was fabricated in a 0.18 µm, 6-layer Aluminum metal, CMOS technology. The chip (Figure Figure 8.) has a relatively large footprint of 15mm×12.5mm. The nine small rectangular structures (labeled "Z") at the center and corners of the chip are sensor structures used to measure the separation between the chip and the substrate. The four large rectangular structures (labeled "P") along the four sides of the chip are used for chip-to-chip data communication [9], and are mostly irrelevant to the experiments described herein.

The remainder of the PKIC consists of an array of unit cells used for interconnect characterization. There are 3944 such unit cells, spaced on a 180 x 180 µm^2 pitch. A unit cell consists of a C4 bump site that can connect to the substrate via a pair of micro-springs; it also contains a set of metrology circuits that can measure the connectivity and resistance of an individual spring connection. Not all unit cells are identical, however. Some unit cells also have on-chip thermometers that can measure the temperature of the chip at that location; some contain sensors for detecting the supply voltages; and others carry sampling circuits for probing on-chip supply waveforms to characterize noise under dynamic loads [11].

Shown in Figure , the metrology circuit in each unit cell can determine the connectivity of each spring connection and measure its resistance through a 3-wire method. Each circuit consists of two switches. One end of both switches is connected to the bond pad, where a connection to a micro-spring can be formed. The other end of switch "V" is connected to a voltage probing line (V line), while that of switch "I" is connected to a current drive line (I line). Both of these lines are shared across all unit cells on the chip, and are connected to the substrate through other micro-springs at two different dedicated sites on the chip (for redundancy).

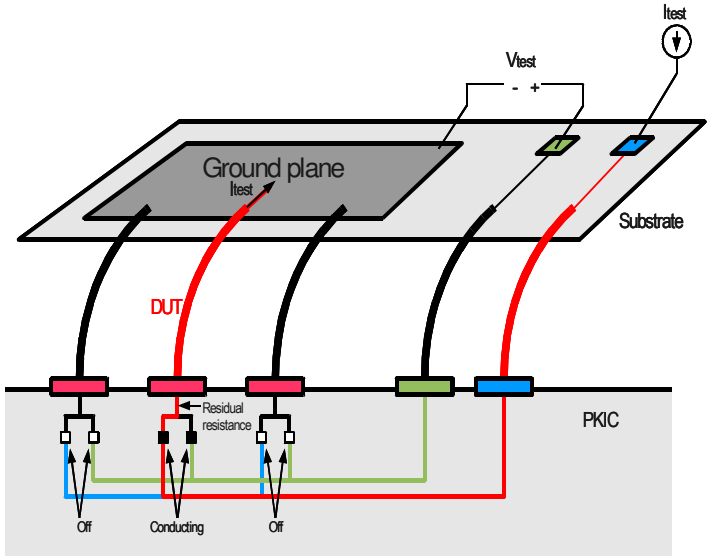

Figure 9. 3-point measurement of micro-spring resistance.

To measure the resistance of a particular micro-spring connection, the pair of switches at the location under test are closed (or shorted), and the switches at all other locations are opened. A known test current, I_{test}, is driven onto the I line from the substrate. This current travels through a micro-spring onto the PKIC, through switch "I" in the unit cell at the location under test, and back to the substrate through the micro-spring under test (DUT), the resistance of which is being measured. As it is infeasible to have a dedicated return pin on the substrate for every connection, this return pin is shared among all the test sites, and is either the power (VDD) or ground (GND) plane.

To perform the 3-point resistance measurement, we probe the voltage between the return pin (VDD or GND) and the V line on the substrate. Since no current flows through this V line, the voltage of the line on the substrate should correspond to that at the bond pad. The value of V_{test} should therefore indicate only the voltage drop across the micro-spring under test (DUT) and the return pin. Unlike a 4-point method, this 3-point measurement includes the undesired resistance of the return pin; however, since it is a ground plane on the substrate, its resistance is typically low. The resistance of the DUT is then simply $R_{DUT} = V_{test} / I_{test}$.

4. IC/micro-spring/substrate package characterization.

Figure Figure is a map that shows the measured spring resistance at each bump site on a ceramic substrate. Some sites on the chip are used for other purposes (*e.g.* data communication, alignment measurement, power delivery) and hence contain no metrology circuitry; these sites have no corresponding resistance data and are shaded black.

The substrate from which the data in Fig. Figure was extracted is the very first substrate assembled using micro-springs. As such, the spring yield was just below 100%. In particular, the spin-on dielectric (BCB) or the photoresist was thicker in one region (toward the lower left corner). As a

result, some vias did not yield in this first preliminary prototype. These sites show a high resistance, and are shaded gray in Fig. Figure . The resistance map allowed us to quickly identify the exact location and cause of failure of these open contacts.

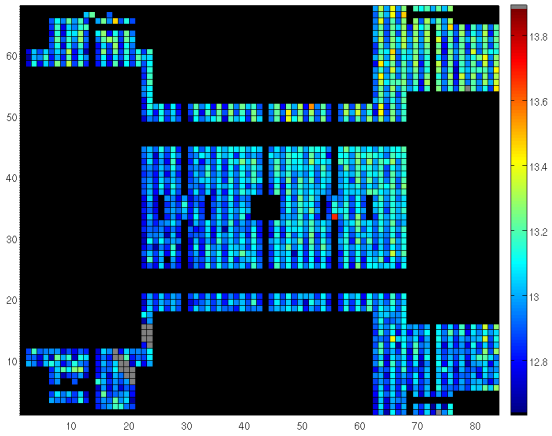

Figure 10. Micro-spring resistance map of the ceramic substrate.

The raw measured data includes the residual resistance of any wire traces that connect the switches to the bond pad. (In fact, it also includes the resistance of the bond pads and any resistance in the supply network on the substrate, but these resistances should be negligible). The residual resistance of these on-chip wire traces is significant (approximately 13Ω) and largely dominates the spring resistance being measured. We calibrated our measurements by repeating the same experiments using the same combination of the substrate and IC which was assembled using conventional reflown C4 solder bumps. The results of such calibration have proven micro-springs contact resistance is within the expected minimal range <0.1 Ω in accordance with previous demonstrations [1]. Slight variations in the measured resistance profile may be caused by die-to-die variations in the residual on-chip trace resistance, as well as variations in the spring resistance due to misalignment and differences in spring compression at different locations.

Conclusions.

We have successfully fabricated flexile micro-springs on the fine 180 µm pitch and demonstrated electronic packages of the large foot print high I/O count die on the ceramic substrate. For the first time the conventional C4 solder bumps have been replaced with compliant interconnects facilitating package rework required for low cost MCM production. The micro-spring interconnects have been characterized and found to have high process yield and low electrical resistance.

Acknowledgments

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