Exploiting CMOS Manufacturing to Reduce Tuning Requirements for Resonant Optical Devices

Ashok V. Krishnamoorthy,[1] Xuezhe Zheng,[1] Guoliang Li,[1] Jin Yao,[1] Thierry Pinguet,[2] Attila Mekis,[2] Hiren Thacker,[1] Ivan Shubin,[1] Ying Luo,[1] Kannan Raj,[1] and John E. Cunningham[1]

(Invited Paper)

[1]Oracle Labs, San Diego, CA 92121 USA
[2]Luxtera Inc., Carlsbad, CA 92011 USA

DOI: 10.1109/JPHOT.2011.2140367
1943-0655/$26.00 ©2011 IEEE

Manuscript received March 5, 2011; accepted March 25, 2011. Date of current version June 28, 2011. This work was supported in part by the Defence Advance Research Projects Agency Microsystems Technology Office under the Ultraperformance Nanophotonic Intrachip Communication program supervised by Dr. J. Shah under contract agreement with SUN Microsystems HR0011-08-9-0001. The views expressed are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government. Approved for public release. Distribution unlimited.
Corresponding author: A. V. Krishnamoorthy (e-mail: ashok.krishnamoorthy@oracle.com).

Abstract: We present manufacturing tolerances of cascaded silicon microring resonators fabricated in a commercial 130-nm complementary-oxide semiconductor (CMOS) foundry using 193-nm lithography and provide statistics gathered from over 500 four-channel microring arrays over multiple wafers and fabrication lots. We quantify intrawafer and interwafer variation of the position and relative spacing of resonance wavelengths for the microring arrays and confirm prior predictions that the absolute resonance positions of such devices cannot be controlled across wafers or even across reticles within a wafer. However, we show that the free spectral range (FSR) of the microrings can be controlled to within 0.66 nm (83 GHz) across wafers and lots, as can the wavelength spacing between closely spaced microrings. To exploit these findings for low-power optical interconnects, we suggest and demonstrate a synthetic resonant comb with $FSR \approx N * \delta\lambda$, wherein resonance wavelengths are spaced equally across the FSR in order to minimize postfabrication tuning. The experimental CMOS 1×8 microring array requires an average tuning of less than 1.2 nm/channel to align to a 200-GHz wavelength division multiplexing (WDM) grid. Monte Carlo simulations on 100 000 sample runs show that an average tuning of 1.72 nm/channel is sufficient for 99% coverage for this component. This indicates that it is possible, with high statistical confidence, to use high-volume CMOS manufacturing to reduce the tuning range and tuning energy requirements of silicon microrings and, hence, enhance their ability to be used in high-density, energy-efficient computing system applications.

Index Terms: Silicon nanophotonics, optical interconnects, technologies for computing.

1. Introduction

Silicon-based optical interconnects are expected to provide high bandwidth and low-power consumption for electronic chip-level communication, due to their electronics integration capability, proven manufacturing record, and improved bandwidth, density, and energy efficiency [1]–[4]. Optical architects have recently proposed several potential system architectures that benefit from such technologies [5]–[7]. Many such architectures rely on integrated resonant optical devices such

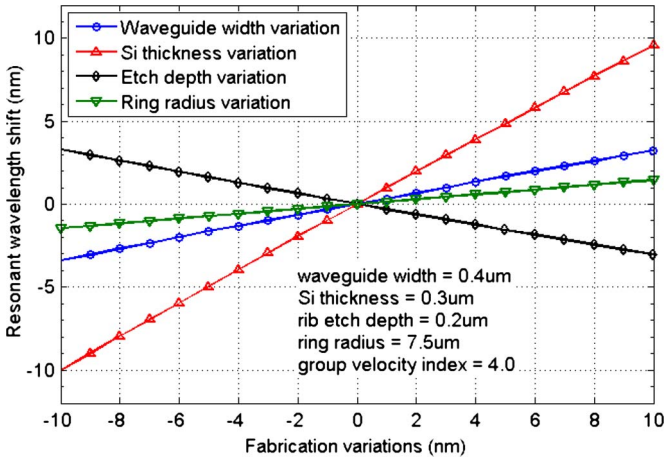

Fig. 1. Resonant wavelength shift due to variations in rib waveguide width, silicon thickness, and etch depth (after [7]).

as rings [8] to create optical filters [9], semiconductor modulators [10], [11], switches [12], and, most recently, nonlinear optical devices. Such devices can now be cofabricated with electronics using a commercial very-large-scale-integration (VLSI) CMOS fabrication facility to create efficient multichannel optical multiplexers and high-speed modulators. Related devices are useful for low-power multiwavelength optical interconnects. This is typically accomplished by making the ring resonator active by introducing an electrically or thermally controllable refractive index to enable a dynamic add/drop function and provide manipulation of the resonant wavelength for tunable add/drop functionality, high-speed modulation, and switching [13]–[24]. These devices promise very small footprints, very low modulation energies, wide working ranges, and adjustable wavelength selectivity. Such devices can be cofabricated with electronics using a commercial VLSI CMOS fabrication facility to create 10-GHz ring modulators [25] integrated with subpicojoule/bit digitally clocked drivers [26] and multichannel tunable CMOS photonic multiplexers and demultiplexers [27].

However, such devices must also be tuned to compensate for nonidealities associated with their manufacture. This requirement can significantly compromise their use in energy-sensitive optical interconnects. We previously showed that manufacturing variations can lead to significant variations from wafer to wafer due to variations in waveguide width, silicon thickness variations, and etch-depth nonuniformities [7]. This is because a small fluctuation in effective index (Δn_{eff}) can result in a large change in resonance wavelength $(\Delta\lambda)$. Depending on the lithography, variations in excess of $\pm$10 nm (or $\pm$1.25 THz) may be expected for resonators using rib-waveguides that underwent a full CMOS process flow. The rib-waveguide structure is interesting because it enables the fabrication of CMOS-compatible high-speed modulators [26] and tunable multiplexers [27] in a common device geometry and possibly even in the same device [28]. The root cause for the resonant wavelength shift can be readily appreciated from Fig. 1, which plots the expected shift in resonant wavelength versus the variation in silicon epi thickness, waveguide width variation, and etch depth for the rib waveguide. The one known parameter is the silicon thickness on a silicon-on-insulator (SOI) wafer—which can result in a total layer thickness variation of up to $\pm$5 nm across multiple wafers, even before the device is processed. Although finer control of SOI thickness is possible [29], this may only be available for ultrathin SOI (under 90 nm thick Si), which is currently not optimized for photonic devices (typically on 300 nm or more thick Si) and which may inordinately increase the cost of such wafers. The other two parameters for the resonant optical device are a strong function of the optical lithography tools and process modules used to create the device. While there have been several successful studies aimed at creating cascaded microrings with varying resonant wavelengths in glass [30], SiN [31], and SOI substrates [32]–[34], there has been limited experimental data available to corroborate the simulated and calculated results from [7]. Most of this work relied on channel (wire) waveguides, which are suitable for mux/demux and

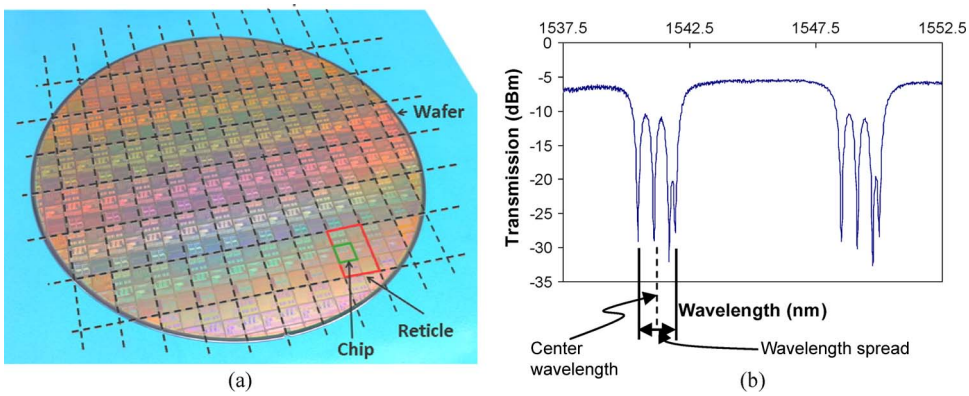

Fig. 2. Wafer scale device study of four identically designed cascaded rings on a common bus waveguide with grating couplers for optical I/O. (a) Fabricated 8-in device CMOS wafer; (b) through-port spectrum of a four-ring Mux/DeMux device showing the definition of the center wavelength and its associated resonance spread across the wafer.

add/drop components but are not also generally applicable to high-speed optical microring modulators. In many cases, e-beam lithography assisted silicon fabrication was employed, which is generally not conducive to low-cost manufacturing. Early work on identical cascaded CMOS-compliant racetrack rings realized for optical buffers showed linewidth broadening owing to the manufacturing-related nonuniformities on the order of 2.4 nm (six sigma) within one chip [35]. Several noteworthy studies of manufacturing tolerances of resonant devices using CMOS high-volume manufacturing tools, optical lithography, and dry etch processes have been launched [36], [37]. In [36], the authors used 193-nm lithography and reported a six-sigma wavelength variation of 0.9 nm for adjacent identical resonators and up to 10.8 nm for resonators physically spaced 20 mm apart. In [37], 248-nm lithography was used with 6-in wafers to determine a potential 1 THz (8 nm) variation in identical microring resonances across a wafer and $>$ 1 THz for rings on separate wafers. However, wafer-to-wafer and lot-to-lot variation of absolute resonance positions for a large number of cascaded microrings of varying sizes was not investigated. To our best knowledge, the optimization of postmanufacturing tuning needs for silicon photonic microrings also remains open.

Here, we analyze data taken over several wafer lots, wafers within each lot, and reticles (or fields) within each wafer that support the predictions from [7] and that identify intrawafer and intrareticle statistics of the fully fabricated cascaded CMOS photonic rings of different sizes based on 193 nm optical lithography. Based on these findings, we suggest the use of *synthetic resonant combs* that relates channel spacing, free spectral range (FSR), and the number of channels to exploit local and global uniformities and significantly reduce the overall tuning requirements for the rings when used in wavelength-division multiplexed interconnects without requiring tighter manufacturing constraints. To generalize the results, Monte Carlo simulation of the synthetic resonant combs seeded with the findings of the manufacturing tolerance studies is used to determine maximum tuning range and power requirements versus confidence level for the optical link. Based on these tuning range requirements, for an 8-wavelength link consisting of cascaded rings with resonances spread across the FSR, tuning energies as low as 15 fJ/bit are predicted.

2. Manufacture of First Generation Microring Arrays

As discussed above, ring resonator based optical devices are sensitive to substrate and fabrication variations. In a first wafer-fab lot, we investigated device performance uniformity experimentally with a 4-ring Mux/DeMux fabricated in an 8-inch 130-nm Freescale-Luxtera CMOS process [25]. Grating couplers were used to test the devices Each of the rings were placed on a common bus and identically designed with a radius of 30 μm. Rings were spaced relatively far apart on the chip (ring center-to-center spacing of 0.5 mm) so as to capture the effect of chip-level nonuniformities. Grating

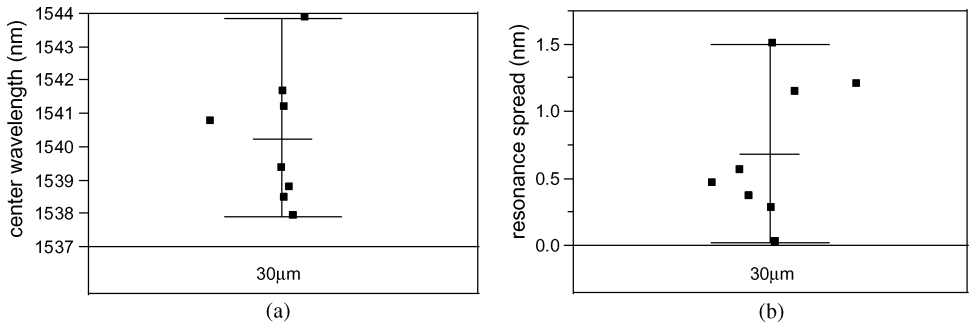

Fig. 3. Wafer scale device uniformity measurement result of four identically designed add/drop rings of 30 μm radius on a common bus waveguide. (a) Resonance center wavelength variation; (b) resonance spread.

couplers were used for optical access to input port, through port, and the drop ports of the individual rings. The rings utilized ridge waveguides optimized for both low loss and to enable tight bending for compact devices with waveguide thickness of 300 nm, width of 360 nm, and slab height of 150 nm. The design is explained in greater detail in [27]. Fig. 2(a) shows a picture of the 8-in device wafer. We measured the resonances of the ring devices across the wafer. No electrical or thermal tuning was applied to any of the devices. A typical through-port spectrum is shown in Fig. 2(b). From the through port spectrum, we measured the center wavelength of the four ring resonances, and the spread of the four resonances in each array.

Fig. 3 summarizes the measurement results of eight 1 $\times$ 4 arrays distributed across the wafer in this first lot of wafers. Because the periodic resonance of a ring device masks inherent variations larger than the FSR, the center wavelength variation in any given array can be no greater than the FSR. As shown in Fig. 3(a), the measured variation in center wavelength of the ring resonances was as large as the FSR of the ring. However, the spread of the resonances within a single 1 $\times$ 4 array was less than 1.6 nm (or 200 GHz), as shown in Fig. 3(b).

From this simple experiment, it appears that the real resonance of any ring devices could be off the design target by a considerable amount. However, rings designed identically in a confined area on a chip (about 1.5 mm in this 4-ring Mux/DeMux case) have tightly spaced resonances (with a high relative accuracy).

Assuming the existence of predefined wavelengths (e.g., the ITU grid or equivalent) that essentially correspond to the laser wavelengths or the modulated data wavelengths depending on whether the resonator comb is being used for modulation, i.e., multiplexing or demultiplexing, a benefit of a series of cascaded ring modulators is that it does not require a separate multiplexer if the laser wavelengths are supplied on a common input bus. From above, it is evident that tuning is required to realign the center wavelength of the wavelength division multiplexing (WDM) filters with the preselected laser wavelengths even if the resonators are designed with some predetermined wavelength spacing. Two common tuning approaches are thermal tuning and forward bias P/N junction tuning. Since forward bias P/N junction tuning changes the Q of the ring, it is only useful when the required amount of tuning is small, and may not be practical for large tuning ranges [7]. However, silicon is featured with a high thermooptic coefficient so that a silicon ring can be tuned in resonance wavelength with a change in temperature by the use of thermal heaters in the direct vicinity to the ring waveguide. Thermal tuning therefore could be utilized in order to compensate for the described fabrication tolerances. The efficiency of the tuning is governed by a proper heater structure configuration with an optimized thermal impedance and high heat flow and optical waveguide overlap [21], [27]. We implemented a doped resistor (N type, 10^{18} cm^{-3}) to create an efficient thermal tuner within the ring itself as reported in [27]. Fig. 4 shows a schematic cross section view of such a ring. When current flows through the doped silicon substrate, the thermal resistance heats the ring waveguide. The effective index of the waveguide changes with the temperature, causing the ring resonant wavelength to shift. This tuning efficiency can be further

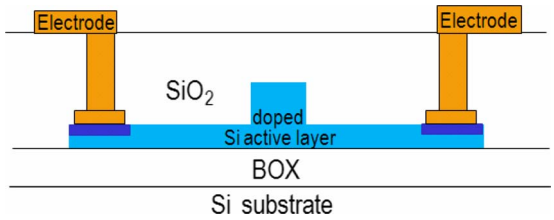

Fig. 4. Schematic of ring thermal tuning with a doped resistor.

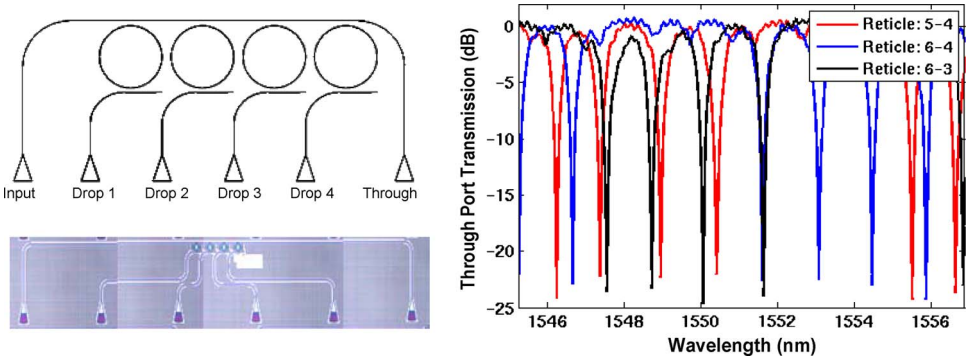

Fig. 5. Schematic and microphotograph of representative 1 $\times$ 4 cascaded ring array with radius $\sim$10 μm and nominal spacing of 200 GHz. Typical through-port spectrum of the array across three different reticles shown on right.

enhanced by an order of magnitude or more by locally removing the substrate under the buried oxide either by back-side etching [38] or by patterning and undercut-etching from the top-surface of the device [39].

We next investigate cascaded microrings with resonances spaced by some predetermined amount and address the question of how to minimize tuning range requirements for a multichannel wavelength-division-multiplexed optical link.

3. Manufacture of Second Generation Cascaded Microring Arrays

In this section, we examine the effect of manufacturing tolerances of cascaded microring resonators fabricated in an 8″ commercial 130 nm CMOS SOI foundry using 193 nm lithography across multiple fabrication runs for demanding computing system applications. We study the reticle-to-reticle, wafer-to-wafer, and lot-to-lot variation in resonance wavelength, wavelength spacing, and FSR for four-channel cascaded microrings of incrementally larger radii spaced 45 μm apart (see Fig. 5). We report these parameters for two "passive" wafers from separate lots that underwent all processing steps up to but not including first metal. We also report the corresponding data from four representative wafers "full-flow" wafers from a lot that underwent the entire flow including all back-end metals and interlayer dielectrics.

To experimentally evaluate the incremental cascaded rings, a new CMOS mask set was designed with four-ring mux/demux devices, as per Fig. 5. Two separate 1 $\times$ 4 designs with nominal ring radii of 7.5 μm and 10 μm were chosen. In each case, the cascaded rings had incrementally increasing radii (on the order of 10–15 nm) which was set by design requirements (for 1.6-nm spacing at a wavelength of 1550 nm) as well as minimum CMOS design grid size allocations. The microrings in this case were spaced 45 μm apart—at a pitch over 10$\times$ smaller than the earlier experiment reported above. As before, grating couplers were used for direct, wafer-scale optical access to the optical devices without requiring any wafer dicing or chip-level polishing. We use a

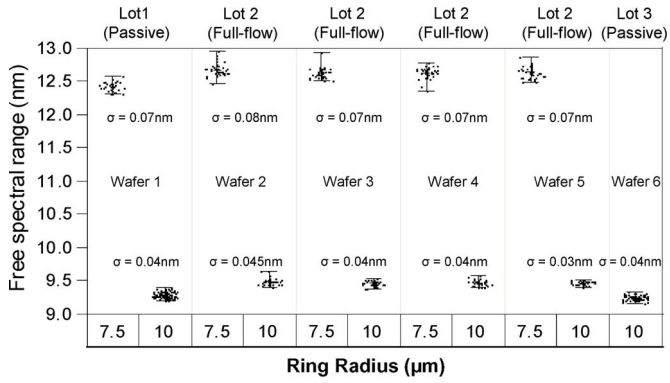

Fig. 6. Variability chart for the average free spectral range of 1 × 4 cascaded ring arrays across six wafers from three lots and for ring radii of 7.5 μm and 10 μm, respectively. The calculated intrawafer variance σ is shown for each dataset.

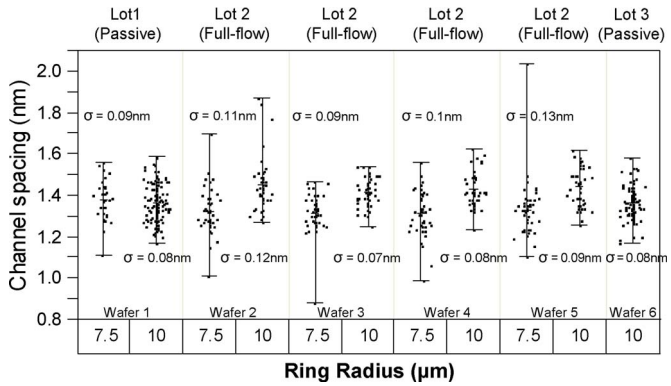

Fig. 7. Variability chart for the channel spacing of 1 × 4 cascaded ring arrays across six wafers from three lots and for ring radii of 7.5 μm and 10 μm, respectively. The calculated intrawafer variance σ is shown for each dataset.

derived GC envelop from the through port spectrum as a reference to normalize the spectrum for the 1 × 4 ring Mux/DeMux devices. This method helped to derive reliable channel BW and isolation. Example results of the 1 × 4 cascaded rings are plotted in Fig. 5, which shows a superposition of three representative arrays from three separate reticles on a wafer with drop port loss calibrated to the through port (shown as zero loss). We measured and analyzed the spectra and report the variation in FSR, channel spacing, and center wavelength of microrings of ~7.5 μm and ~10 μm nominal radii, respectively, across 48 reticles on each of six 8-in wafers from three wafer lots processed with a common mask set.

The variability chart of the FSR of microrings with nominal radii of 7.5 μm and 10 μm, respectively, across the six wafers from two passive lots and one full-flow lot is presented in Fig. 6. One wafer was measured from each passive lot and four wafers were measured from the full-flow lot. Each data point corresponds to a unique 1 × 4 cascaded microring array on a unique reticle corresponding to the same coupling gap. In each array, the microrings were designed to create a four-channel filter with a spacing of 1.6 nm (200 GHz). The first observation was that the intrawafer and wafer-to-wafer variation in FSR was very small across all lots. The 7.5 μm radius microrings achieved 6σ intrawafer variation below 0.48 nm for all passive and full-flow wafers (Fig. 6) and a 6σ wafer-to-wafer variation below 0.66 nm [see Fig. 8(a)]. Likewise, the 10 μm radius microrings achieved 6σ intrawafer variation below 0.27 nm for all passive and full-flow wafers and a 6σ wafer-to-wafer variation below 0.6 nm. Other measurements (not shown here) verified that devices with slightly larger or smaller coupling

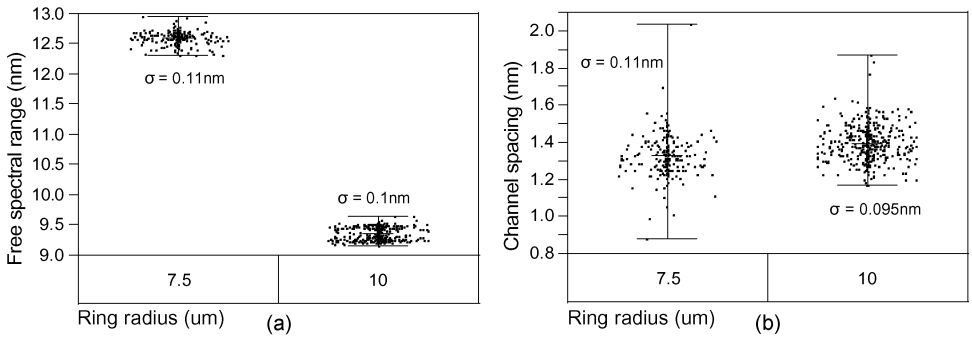

Fig. 8. Variability chart for (a) free-spectral range and (b) average channel spacing of 1 × 4 cascaded ring arrays across all measured wafers from three lots and for ring radii of 7.5 μm and 10 μm, respectively. Each point represents one reticle. The calculated wafer-to-wafer variance σ is shown for each dataset.

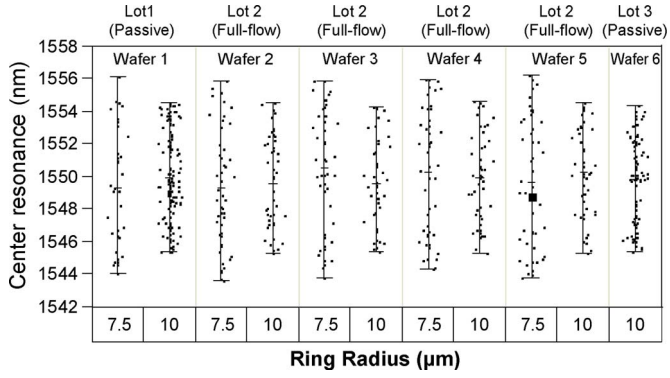

Fig. 9. Variability chart for the center resonance of 1 × 4 cascaded ring arrays across six wafers from three lots and for ring radii of 7.5 μm and 10 μm, respectively.

gaps also showed excellent consistency in the FSR of the devices across both passive and full-flow wafers.

Fig. 7 shows the variability chart across six 8″ CMOS wafers of the channel separation of the 1 × 4 cascaded microrings. We note that the mean channel spacing was approximately 1.36 nm in every case versus the design target of 1.6 nm. We attribute this to a systematic error that affected all our designs, and assume that this is correctable in future runs. The next observation was that the channel spacing could be controlled to within a 6σ intrawafer variation of 0.54–0.78 nm (70–100 GHz) for the 7.5-μm radius rings and 0.42–0.72 nm (50–90 GHz) for the 10-μm radius rings (see Fig. 7). The corresponding 6σ wafer-to-wafer variation in spacing for the microring arrays of 7.5 μm and 10 μm nominal radii was 0.66 nm (83 GHz) and 0.57 nm (72 GHz), respectively [see Fig. 8(b)]. Part of this latter variation is due to the variation in the ring FSR. Finally, we note that the center wavelength of the four-channel add/drop filter varied randomly across the entire FSR for the 7.5-μm and the 10-μm radius microrings on all measured wafers, confirming our earlier analysis that such devices can have more than 10 nm absolute resonance wavelength shift relative to design target due to substrate thickness nonuniformity and fabrication tolerances (see Fig. 9).

The next question was whether there was a systematic pattern of resonance shift across the wafers that perhaps could be compensated with broad binning and/or by associating with the position of the reticle on the wafer. To investigate the variation across a given wafer and between wafers, we plotted the position of the center resonance of the 1 × 4 Mux/DeMux devices with both 7.5-μm rings and 10-μm rings as a function of position across several separate wafers (aligned on a common direction). Results are plotted in Fig. 10. From these results, the conclusion is that there is

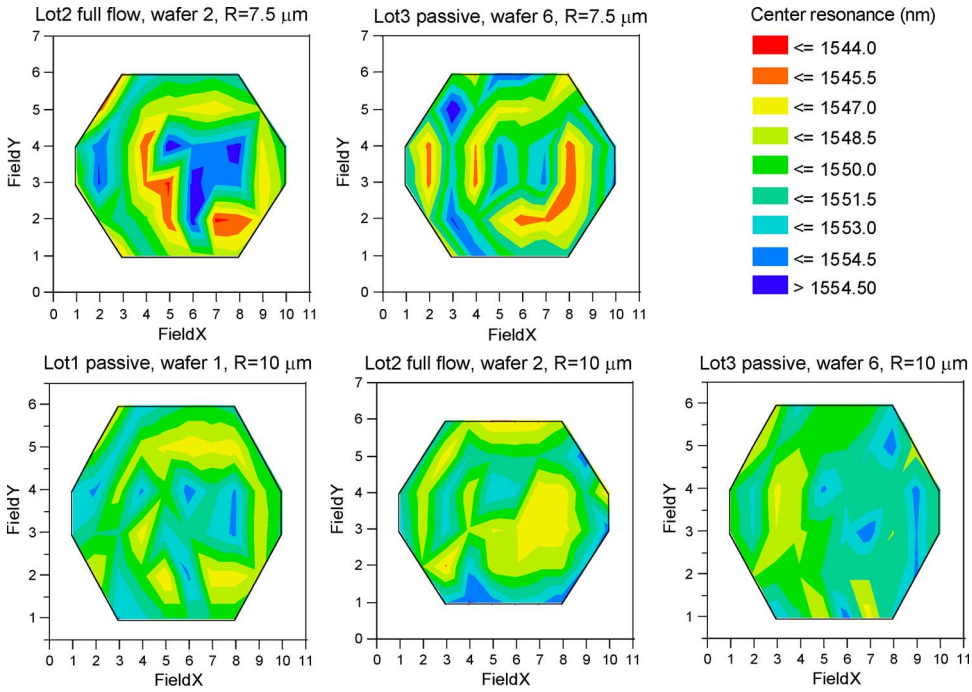

Fig. 10. Color-coded wafer-scale map from 48 reticles per wafer plotting the distribution of the center resonance of 1 $\times$ 4 arrays of cascaded rings with nominal radius of 7.5 μm and 10 μm on passive and full-flow wafers.

not only a broad variation of resonance centers across the FSR on a given wafer, but also that there does not seem to be a systematic *a priori* method of binning the reticles to preassigned wavelengths across a wafer or between wafers. The use of binning only seems possible after testing the devices. We seek a more effective method of reducing *a posteriori* tuning for microring arrays.

4. Exploiting Local Resonance Uniformities in a Multichannel WDM Link

The effective center wavelength of the microring arrays as discussed above can shift significantly. To minimize the tuning range, one may be inclined to reduce the resonator FSR. However, reducing the FSR requires an increase in ring size, which, in turn, reduces the thermal tuning efficiency in terms of wavelength shift per unit power. Furthermore, if one combines modulation plus multiplexing into a single device, then smaller modulators are preferred from a modulation energy perspective. Hence, a smaller device with a large FSR is preferable for a cascaded modulator or a multichannel mux/demux filter even though it may require a larger tuning range. However, too small a ring (with unnecessarily large FSR) may neither be optimal. In our example above, we had four channels spaced at 1.6 nm (200 GHz), whereas the FSR was approximately 12.5 nm. The average tuning per channel could have been reduced if the FSR was smaller or if there were more channels. At a channel spacing of 1.6 nm, an efficient wavelength-division multiplexed link requires each ring to have a FSR—preferably about N times the channel spacing to accommodate N wavelengths and simplify wavelength assignment.

In the following, we present a systematic method to significantly reduce the tuning range using cascaded rings by exploiting the properties that the FSR of the microrings can be accurately controlled and that microrings placed together on a localized area on the wafer have controlled spacing. We assume a generalized link with N wavelengths, N microring transmitters on a common bus, a 1 $\times$ N wavelength demultiplexer, and N receivers. As shown in Fig. 11, for an 8-wavelength link system, each ring device is set to have FSR approximately equal to $N * \delta\lambda$; and the mth order of the rings resonances are aligned with the predefined wavelengths $\lambda_1, \lambda_2, \ldots, \lambda_8$. The *combined* spectrum of these cascaded rings will have resonances filling the entire spectral space, creating a

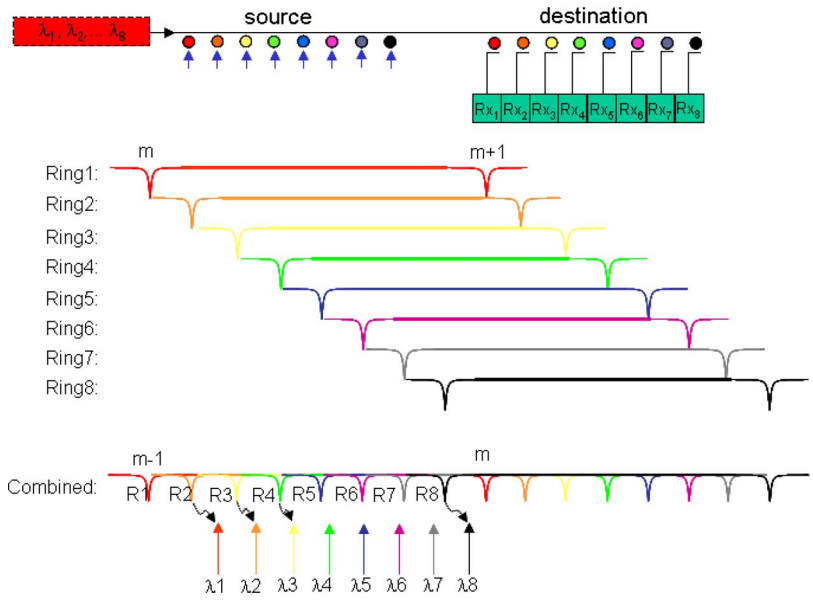

Fig. 11. The synthetic resonant comb design spreads the ring resonances across the FSR with evenly spaced channels to create a periodic comb spectrum and reduces postmanufacturing static tuning required to compensate for manufacturing-related phase errors.

synthetic resonant comb as shown in the bottom of Fig. 11. By appropriately assigning wavelengths at the transmitter and receiver (which must be done once at system startup), a WDM link can be effectively achieved while minimizing tuning range to a fraction of the FSR.

Because of the uncertain post-manufacture comb center position and the random relative channel resonance shift, tuning will be needed to realign the ring resonances with the laser (data) wavelengths. To minimize the tuning energy, as shown in Fig. 11, instead of tuning the mth order of the ring device 1 (R1) to its designed wavelength $\lambda 1$, one can tune another resonance that is the closest to $\lambda 1$, the (m-1)th order resonance of ring device 2 (R2) in this case. Applying the same approach to the rest of wavelength channels, the tuning range of the WDM link is reduced to be on the order of the channel spacing instead of the whole FSR. This wavelength registration process only needs to be done once the system is initialized. In the following, we quantify the tuning requirements of a WDM link using this synthetic resonant comb approach.

5. Minimizing Tuning Requirements Using a Synthetic Resonant Comb Spectrum: Simulations and Experiment

As described above, an approximate, rule-of-thumb design rule between the microring FSR, number of wavelengths (N), and the channel spacing $(\delta\lambda)$ of FSR $\approx N * \delta\lambda$ creates a synthetic resonant comb that can be used to exploit local uniformities and minimize static link tuning energy requirements to a fixed wavelength grid. We assume that we are able to shift a resonance peak by heating the ring locally, but that there is no ability to locally cool the device. Hence, any thermal corrections to the resonant peaks are strictly unidirectional. As shown in Fig. 11, a typical case would require a given device to be tuned less than one channel spacing. However, a pathological (worst) case occurs when one resonance is maximally blue-shifted, while all others are maximally red-shifted, causing the worst-case tuning to be about twice the channel spacing. To evaluate the wafer-level yield of this approach and investigate the average versus worst-case tuning requirements, Monte Carlo simulations seeded with the findings of the manufacturing tolerance studies were used to determine the average tuning range required per channel to a fixed wavelength grid versus confidence level for the cascaded microrings in a resonant comb configuration. We ran

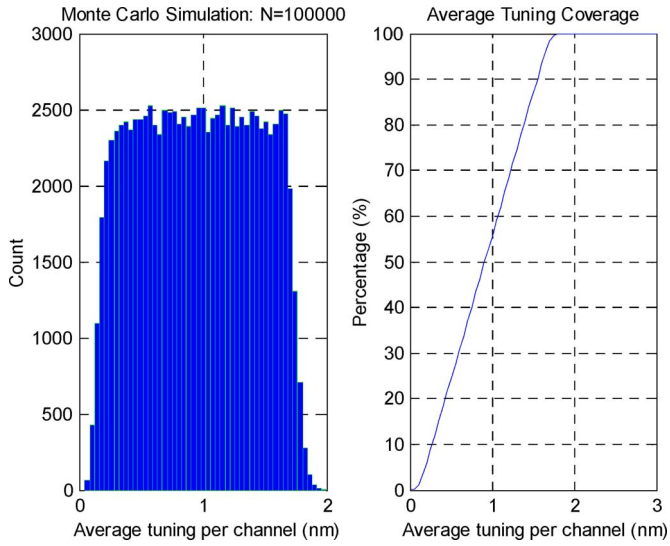

Fig. 12. Monte Carlo simulations are used to calculate the average tuning per channel, assuming unidirectional tuning, for 8-wavelength channels spaced 1.6 nm apart for comb group center variations (uniformly distributed between -0.8 nm and $+0.8$ nm) and individual ring resonance shifts relative to their designed centers (6σ of 0.66 nm).

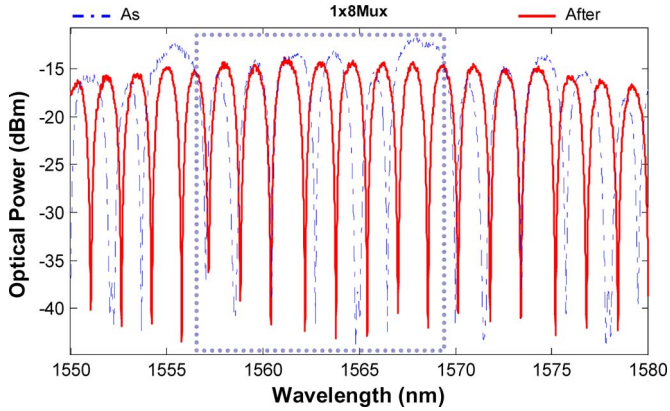

Fig. 13. Through spectra of the cascaded microring mux/demux as manufactured (dashed lines) and after tuning using integrated heaters (solid lines) to create a resonant comb with a channel spacing of 1.6 nm (200 GHz) at 1560 nm. An average tuning of only 1.2 nm (150 GHz) was required to align the channels to a 200 GHz ITU grid.

simulations with 100 000 samples to gather statistics for a practical system with eight wavelength channels. The assumptions were that comb group centers would vary randomly (uniformly distributed between -0.8 nm to $+0.8$ nm) and individual ring resonance would shift relative to their designed centers (6σ of 0.66 nm). A histogram of average tuning requirements and corresponding percentage coverage (wafer-level yield) of this approach is shown in Fig. 12.

The plots indicate that an average tuning of below 1 nm is required. Furthermore, 99% of the cases require less than 1.72 nm of tuning per channel for the given 8-wavelength device with a FSR of 12.8 nm, a wavelength spacing of 1.6 nm, and a 6σ local variation of ± 0.66 nm. Based on this design, we demonstrated a thermally tunable 8-channel resonant comb with $\delta\lambda = 200$ GHz (1.6 nm) and an FSR of 12.8 nm. Each ring has a built-in silicon resistor heater and is aligned to a 200 GHz grid spacing in the C-band with an average tuning requirement below 1.2 nm/channel. Fig. 13 shows the measured spectra as manufactured and after tuning was applied to the 1×8 microring array.

6. Calculation of Average and Maximum Tuning Power

The calculation of average tuning power required for a link comprised of the cascaded incremental rings follows directly from the tuning requirements observed in Section 5. Tuning efficiencies as high as 3.9 mW per FSR [38] and 2.4 mW per FSR [39] have been demonstrated for back-etched rib-waveguide and undercut-etched wire-waveguide based devices, respectively. Assuming an average tuning of approximately 1.7 nm will be required for tightly spaced 1 $\times$ 8 Mux/DeMux devices on a 1.6-nm channel spacing (95% confidence level from Fig. 12), this corresponds to a tuning power of $\sim$0.3 mW for the wire-waveguide device or, equivalently, 0.52 mW for the rib-waveguide device. Equivalently, this equates to a static tuning energy of 15 fJ/bit at a bit rate of 20 Gb/s for the 8-channel wire-waveguide microring array and, likewise, of 26 fJ/bit for the 8-channel rib-waveguide device. A link as in Fig. 11 would require one of each component (modulator/Mux and DeMux) to give a static link tuning energy budget of 41 fJ/bit. This is consistent with the expectations for an ultralow power budget link [7]. The use of a tighter wavelength grid with 16 channels spaced at 0.8 nm (100 GHz) can potentially reduce this further.

7. Summary and Conclusions

It has been suggested that silicon CMOS provides "Cheap Manufacturing of Optical Subsystems" [40]. In this paper, we have explored this potential and quantified the effect of manufacturing tolerances of cascaded ring resonators fabricated in a commercial 130-nm CMOS foundry using 193-nm lithography by providing and analyzing statistics gathered over multiple reticles, wafers, and fabrication lots. We have confirmed prior predictions that the absolute resonance wavelengths of individual devices cannot be controlled across wafers or even across reticles or fields within a wafer. However, we have shown for the first time that the FSR of the microrings can be accurately controlled across wafers. Tighter control of the FSR is available for a given effective index fluctuation since $|\Delta\text{FSR/FSR}| \approx 2|\Delta\lambda/\lambda|$ and FSR $\ll \lambda$. We have also shown that local uniformity in the relative position and spacing of resonance wavelengths can be achieved with a 130 nm CMOS process and have quantified this empirically. We have proposed a design guideline between the microring FSR, number of wavelengths (N), and the channel spacing $(\delta\lambda)$ of FSR $\approx N * \delta\lambda$, together with a nearest neighbor wavelength-assignment method. The design results in a synthetic resonant comb that can minimize static link tuning energy requirements for a link consisting of a cascaded, wavelength-division multiplexed, transmitter, and a corresponding demultiplexing receiver. We have demonstrated through Monte Carlo simulation that the uniformity of the microring FSR in conjunction with this control of local uniformity, occurring on the length scale of millimeters and less, can be exploited across wafers and lots through the use of this synthetic resonant comb. We have experimentally verified the resonant comb configuration and proved that it can result in low postmanufacture tuning requirements. Based on the experiments, empirical findings and Monte Carlo simulation results, we have derived that the tuning energy per bit may be controlled to as low as 15 fJ/bit for undercut wire-waveguide rings and 26 fJ/bit for back-etched rib-waveguide rings using thermal tuning. This ultralow tuning power is a key requirement for dense inter and intrachip silicon photonic links that can significantly enhance their use in energy-sensitive applications. Finally, we note that this paper has not addressed additional dynamic tuning requirements that may be required for the link—which will be the subject of future work.

Acknowledgment

The authors gratefully acknowledge H. Sidhom for mask layouts related to the CMOS photonic rings.

References

[1] R. A. Soref, "The past, present and future of silicon photonics," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1678–1687, Nov./Dec. 2006.

[2] D. A. B. Miller, "Rationale and challenges for optical interconnects to electronic chips," *Proc. IEEE*, vol. 88, no. 6, pp. 728–749, Jun. 2000.
[3] L. C. Kimerling, D. Ahn, A. B. Apsel, M. Beals, D. Carothers, Y.-K. Chen, T. Conway, D. M. Gill, M. Grove, C.-Y. Hong, M. Lipson, J. Liu, J. Michel, D. Pan, S. S. Patel, A. T. Pomerene, M. Rasras, D. K. Sparacin, K.-Y. Tu, A. E. White, and C. W. Wong, "Electronic–photonic integrated circuits on the CMOS platform," in *Proc. SPIE*, 2006, vol. 6125, pp. 6–15.
[4] B. Jalali, M. Paniccia, and G. Reed, "Silicon photonics," *IEEE Microw. Mag.*, vol. 7, no. 3, pp. 56–68, Jun. 2006.
[5] J. Ahn, M. Fiorentino, R. G. Beausoleil, N. Binkert, A. Davis, D. Fattal, N. P. Jouppi, M. McLaren, C. M. Santori, R. S. Schreiber, S. M. Spillane, D. Vantrease, and Q. Xu, "Devices and architectures for photonic chip-scale integration," *Appl. Phys. A*, vol. 95, no. 4, pp. 989–997, Jun. 2009.
[6] C. Batten, A. Joshi, J. Orcutt, A. Khilo, B. Moss, C. W. Holzwarth, M. A. Popovic, H. Q. Li, H. I. Smith, J. L. Hoyt, F. X. Kartner, R. J. Ram, V. Stojanovic, and K. Asanovic, "Building many-core processor-to-DRAM networks with monolithic CMOS silicon photonics," *IEEE Micro*, vol. 29, no. 4, pp. 8–21, Jul./Aug. 2009.
[7] A. V. Krishnamoorthy, R. Ho, X. Zheng, H. Schwetman, J. Lexau, P. Koka, G. Li, I. Shubin, and J. E. Cunningham, "Computer systems based on silicon photonic interconnects," *Proc. IEEE*, vol. 97, no. 7, pp. 1337–1361, Jul. 2009.
[8] E. A. J. Marcatilli, "Bends in optical dielectric waveguides," *Bell Syst. Tech. J.*, vol. 48, no. 7, pp. 2103–2132, Sep. 1969.
[9] B. E. Little, J. S. Foresi, G. Steinmeyer, E. R. Thoen, S. T. Chu, H. A. Haus, E. P. Ippen, L. C. Kimerling, and W. Greene, "Ultra-compact Si-SiO_2 microring resonator optical channel dropping filters," *IEEE Photon. Technol. Lett.*, vol. 10, no. 4, pp. 549–551, Apr. 1998.
[10] T. Sadagopan, S. J. Choi, S. J. Choi, K. Djordjev, and P. D. Dapkus, "Carrier-induced refractive index changes in InP-based circular microresonators for low-voltage, high-speed modulation," *IEEE Photon. Technol. Lett.*, vol. 17, no. 2, pp. 414–416, Feb. 2005.
[11] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," *Nature*, vol. 435, no. 7040, pp. 325–327, May 2005.
[12] B. E. Little, H. A. Haus, J. S. Foresi, L. C. Kimerling, E. P. Ippen, and D. J. Ripin, "Wavelength switching and routing using absorption and resonance," *IEEE Photon. Technol. Lett.*, vol. 10, no. 6, pp. 816–818, Jun. 1998.
[13] E. J. Klein, D. H. Geuzebroek, H. Kelderman, G. Sengo, J. Baker, and A. Driessen, "Reconfigurable optical add-drop multiplexer using microring resonators," *IEEE Photon. Technol. Lett.*, vol. 17, no. 11, pp. 2358–2360, Nov. 2005.
[14] P. Dong, S. F. Preble, and M. Lipson, "All-optical compact silicon comb switch," *Opt. Exp.*, vol. 15, no. 15, pp. 9600–9605, Jul. 2007.
[15] Y. Vlasov, W. M. J. Green, and F. Xia, "Ultra-compact high-order ring resonator filters using submicron silicon photonic wires for onchip optical interconnects," *Opt. Exp.*, vol. 15, no. 19, pp. 11 934–11 941, Sep. 2007.
[16] S. Xiao, M. H. Khan, H. Shen, and M. Qi, "Multiple-channel silicon micro-resonator based filters for WDM applications," *Opt. Exp.*, vol. 15, no. 12, pp. 7489–7498, Jun. 2007.
[17] N. Sherwood-Droz, H. Wang, L. Chen, B. G. Lee, A. Biberman, K. Bergman, and M. Lipson, "Optical 4×4 hitless silicon router for optical Networks-on-Chip (NoC)," *Opt. Exp.*, vol. 16, no. 20, pp. 15 915–15 922, Sep. 2008.
[18] H.-Y. Ng, M. R. Wang, D. Li, X. Wang, J. Martinez, R. R. Panepucci, and K. Pathak, "4×4 wavelength-reconfigurable photonic switch based on thermally tuned silicon microring resonators," *Opt. Eng.*, vol. 47, no. 4, pp. 044601-1–044601-8, 2008.
[19] M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, "Ultralow power silicon microdisk modulators and switches," in *Proc. 5th IEEE Int. Conf. Group IV Photon.*, 2008, pp. 4–6.
[20] P. Dong, S. Liao, D. Feng, H. Liang, D. Zheng, R. Shafiiha, C.-C. Kung, W. Qian, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Low Vpp, ultralow-energy, compact, high-speed silicon electro-optic modulator," *Opt. Exp.*, vol. 17, no. 25, pp. 22 484–22 490, Dec. 2009.
[21] M. R. Watts, W. A. Zortman, D. C. Trotter, G. N. Nielson, D. L. Luck, and R. W. Young, "Adiabatic resonant microrings (ARMs) with directly integrated thermal microphotonics," in *Proc. CLEO/QELS*, 2009, pp. 1–2.
[22] M. Geng, L. Jia, L. Zhang, L. Yang, P. Chen, T. Wang, and Y. Liu, "Four-channel reconfigurable optical add-drop multiplexer based on photonic wire waveguide," *Opt. Exp.*, vol. 17, no. 7, pp. 5502–5516, Mar. 2009.
[23] W. A. Zortman, M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, "Low-power high-speed silicon microdisk modulators," presented at the Conf. Lasers Electro-Optics, San Jose, CA, 2010, Paper CThj4.
[24] P. Dong, W. Qian, H. Liang, R. Shafiiha, N.-N. Feng, D. Feng, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Low power and compact multiplexing devices based on silicon microring resonator," *Opt. Exp.*, vol. 18, no. 10, pp. 9852–9858, May 2010.
[25] C. Gunn, "CMOS photonics for high-speed interconnects," *IEEE Micro*, vol. 26, no. 2, pp. 58–66, Mar./Apr. 2006.
[26] X. Zheng, J. Lexau, Y. Luo, H. Thacker, T. Pinguet, A. Mekis, G. Li, J. Shi, P. Amberg, N. Pinckney, K. Raj, R. Ho, J. E. Cunningham, and A. V. Krishnamoorthy, "Ultra-low energy all-CMOS modulator integrated with driver," *Opt. Exp.*, vol. 18, no. 3, pp. 3059–3070, Feb. 2010.
[27] X. Zheng, I. Shubin, G. Li, T. Pinguet, A. Mekis, J. Yao, H. Thacker, Y. Luo, J. Costa, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "A tunable 1×4 silicon CMOS photonic wavelength multiplexer/demultiplexer for dense optical interconnects," *Opt. Exp.*, vol. 18, no. 5, pp. 5151–5160, Mar. 2010.
[28] P. Dong, R. Shafiiha, S. Liao, H. Liang, N.-N. Feng, D. Feng, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Wavelength-tunable silicon microring modulator," *Opt. Exp.*, vol. 18, no. 11, pp. 10 941–10 946, May 2010.
[29] D. Delprat, F. Boedt, C. David, P. Reynaud, A. Alami-Idrissi, D. Landru, C. Girard, and C. Maleville, "SOI substrate readiness for 22/20 nm and for fully-depleted planar device architectures," in *Proc. IEEE Int. SOI Conf.*, Foster City, CA, 2009, pp. 1–4.
[30] S. T. Chu, B. E. Little, W. Pan, T. Kaneko, S. Sato, and Y. Kokubun, "An eight-channel add-drop filter using vertically-coupled microring resonators over a cross grid," *IEEE Photon. Technol. Lett.*, vol. 11, no. 6, pp. 691–693, Jun. 1999.
[31] C. W. Holzwarth, T. Barwicz, M. A. Popovic, P. T. Rakich, E. P. Ippen, F. X. Kartner, and H. I. Smith, "Accurate resonant frequency spacing of microring filters without postfabrication trimming," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 24, no. 6, pp. 3244–3247, Nov. 2006.

[32] Q. Xu, B. Schmidt, J. Shakya, and M. Lipson, "Cascaded silicon micro-ring modulators for WDM optical interconnection," *Opt. Exp.*, vol. 14, no. 20, pp. 9431–9435, Oct. 2006.
[33] S. Xiao, M. H. Khan, H. Shen, and M. Qi, "Multiple-channel micro-resonator based filters for WDM applications," *Opt. Exp.*, vol. 15, no. 12, pp. 7489–7498, Jun. 2007.
[34] M. S. Dahlem, C. W. Holzwarth, A. Khilo, F. X. Kartner, H. I. Smith, and E. P. Ippen, "Reconfigurable multi-channel second-order silicon microring-resonator filterbanks for on-chip WDM systems," *Opt. Exp.*, vol. 19, no. 1, pp. 306–316, Jan. 2011.
[35] F. Xia, E. L. Sekaric, and Y. A. Vlasov, "Ultracompact optical buffers on a silicon chip," *Nat. Photon.*, vol. 1, no. 1, pp. 65–71, 2007.
[36] S. K. Selvaraja, W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, "Subnanometer linewidth uniformity in silicon nanophotonic waveguide devices using CMOS fabrication technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 16, no. 1, pp. 316–324, Jan./Feb. 2010.
[37] W. A. Zortman, D. C. Trotter, and M. R. Watts, "Silicon photonics manufacturing," *Opt. Exp.*, vol. 18, no. 23, pp. 23 598–23 607, Nov. 2010.
[38] J. E. Cunningham, I. Shubin, X. Zheng, T. Pinguet, A. Mekis, and A. V. Krishnamoorthy, "Highly-efficient thermally-tuned resonant filters," *Opt. Exp.*, vol. 18, no. 18, pp. 19055–19063, Aug. 2010.
[39] P. Dong, W. Qian, H. Liang, R. Shafiiha, D. Feng, G. Li, J. E. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "Thermally tunable silicon racetrack resonators with ultralow tuning power," *Opt. Exp.*, vol. 18, no. 19, pp. 20 298–20 304, Sep. 2010.
[40] T. Li [private communication].