

# Design Space Exploration of Power Delivery For Advanced Packaging Technologies

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**Abstract**—In this paper, a design space exploration of power delivery networks is performed for multi-chip 2.5-D and 3-D IC technologies. The focus of the paper is the effective placement of the voltage regulator modules (VRMs) for power supply noise (PSN) suppression. Multiple on-package VRM configurations have been analyzed and compared. Additionally, 3D IC chip-on-VRM and backside-of-the-package VRM configurations are studied. From the PSN perspective, the 3D IC chip-on-VRM case suppresses the PSN the most even with high current density hotspots. The paper also studies the impact of different parameters such as VRM-chip distance on the package, on-chip decoupling capacitor density, etc. on the PSN.

**Index Terms**—2.5-D and 3-D integration, power integrity, interconnect, modeling, IR drop,  $\frac{dI}{dt}$  noise, decoupling capacitor.

## I. INTRODUCTION

**P**OWER requirements in modern high performance computing systems are becoming increasingly stringent. Traditionally, the power supplies are placed off-chip to provide necessary load currents to the on-chip active circuitry. These systems typically have resistive and parasitic losses from the interconnects and metal pads. Large passive components (i.e., capacitors) are placed to somewhat compensate these effects. However, the power delivery challenges are becoming increasingly prominent as more and more transistors are being packed into a single chip. As a result, number of bumps/pads, on-chip wires, etc. is also increasing. These added components contribute to the parasitics of the power delivery path. Recently, on-chip regulators have gained significant attention because of their fine grain voltage control, increased availability of power, increased performance, decreased inductor size, etc. [1]–[4]. These technologies eliminate the need for multiple VRs in the case of multiple supply voltage systems while reducing the parasitic length of the power delivery path, enabling active power management required by high performance computing devices. In short, these are efforts to bring the power supply circuitry closer to the active circuits.

Power supply noise (PSN) modeling has been under extensive research over the last couple of decades [5]–[9]. The power supply is assumed ideal in the prior studies. Moreover, there are VRM parasitics which impact the PSN of the system. Also, a distributed package level PDN along with the distributed decoupling capacitors are important in accurately

characterizing the PSN of any given architecture. Therefore, in this paper, based on prior Power Delivery Network (PDN) modeling efforts [7], [9], [10], different voltage regulator module (VRM) placement methodologies e.g., on-package, 3D stacked VRM-chip, VRM placed on the backside of the package, etc. have been explored. First, the benchmark architectures for analysis are described in Section II. Section III shows the DC IR drop results for different architectures. Transient noise of different configurations is analyzed and compared in Section IV. Finally, in Section V, the concluding remarks are stated.

## II. PDN MODELING AND SPECIFICATIONS

Several benchmark configurations have been analyzed in this paper. In Fig. 1(a), the VRM chip is placed next to the active chip on the same package and thus, the long interconnect distance from the power supply to the chip is reduced. The configuration shown in Fig. 1(b) considers a VRM chip placed on the backside of the package. Fig. 1(c) shows the 3D IC stacking of a processor chip on top of the VRM chip.

TABLE I: PDN parameters

TSV resistivity [11]	$80 \times 10^{-9} \Omega\text{m}$
Package wire thickness (metal planes)	10 P/G metal layers, 0.010 mm per layer
On-chip PDN wire dimensions	5 $\mu\text{m}$ thick, 3.3 $\mu\text{m}$ wide, 30 $\mu\text{m}$ pitch
On-chip PDN wire resistivity	$17.1 \times 10^{-9} \Omega\text{m}$
On-chip decoupling capacitor	5.3 nF/mm <sup>2</sup>
C4 bump diameter/pitch	40 $\mu\text{m}$ /100 $\mu\text{m}$

The overall analysis flow is as described in the prior work [7], [9]. Throughout this paper, a 1 cm  $\times$  1 cm chip is considered. The active chip is assumed to have a 1 V supply voltage rail and a total power of 100 W. VRM parasitic resistance and inductance are extracted from the literature [12], [13]. The equivalent series resistance ( $C_{\text{esr}}$ ) and inductance ( $C_{\text{esl}}$ ) of the capacitors are also incorporated in the model. The second region is the board-level lumped parameters along with their decoupling capacitance. Bump parasitics have two sources: solder bumps between the package and the board, and C4 bumps between the package and the chip. Discrete decoupling capacitors have equivalent series resistance (ESR), equivalent series inductance (ESL), and equivalent series capacitance (ESC). These decoupling capacitors are then distributed throughout the package. The overall specifications of

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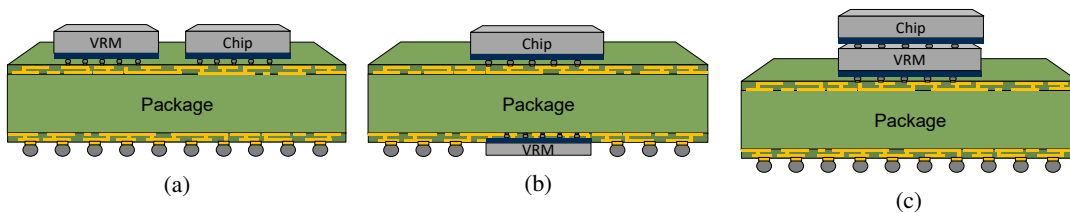


Fig. 1: Benchmark architectures: (a) On-package VRM configuration, (b) Backside-of-the-package VRM Configuration, and (c) 3D IC Chip-on-VRM Configuration

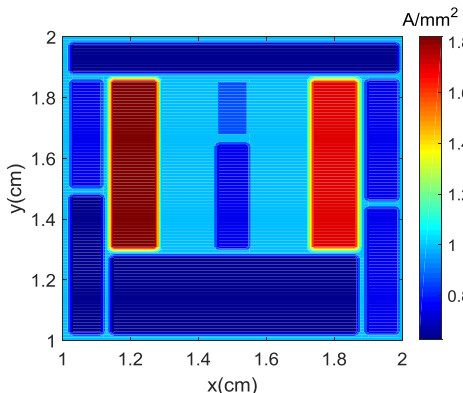


Fig. 2: The non-uniform current density map used for the analysis

different parameters are described in Table I. Non-uniform current density map with distinct high power blocks is used for the simulations. The power map (or current density map) is as specified in [14], but is modified according to [15], [16].

### III. DC IR DROP COMPARISON OF DIFFERENT BENCHMARK CONFIGURATIONS

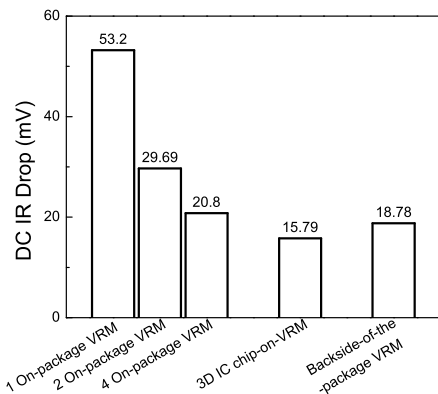


Fig. 3: Comparison of DC IR drop for different configurations

In this section, the DC IR drop for different configurations i.e., on-package VRM, 3D IC chip-on-VRM, and the backside-of-the-package VRM, etc. have been analyzed. In each configuration, adding additional VRMs to the system reduces DC IR drop. The impact of multiple VRMs on PSN suppression is more pronounced if there are hotspots in the chip. Fig. 3 summarizes the results for different VRM-processor configurations. In the backside-of-the-package VRM

and 3D IC chip-on-VRM cases, owing to the shorter distance, the IR drop is smaller compared to the prior on-package VRM cases. In the backside-of-the-package configuration, the through package vias and metal layers in the package PDN are important components of the power delivery path. In the 3D IC case, however, due to the dense bumps between the chips, the TSVs in the VRM chip and the microbumps between the VRM and the active chip are the only contributors of the parasitics in the PDN path. As a result, the IR drop for the 3D IC case is 24% and 15.9% smaller than that with four on-package VRMs, and backside of the package VRM cases, respectively.

Since the multiple on-package VRMs case brings the regulator circuit closer to the active chip, there are different trade-off analyses which determine how close we can bring these chips. Fig. 4 shows the DC IR drop results for three different distances between the chips. In the baseline model,

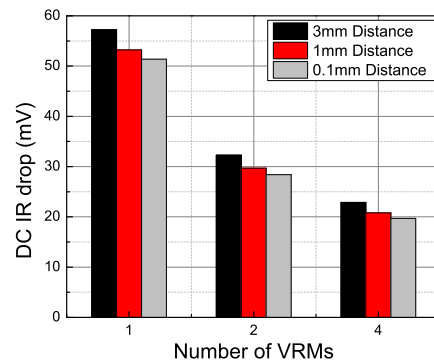


Fig. 4: Comparison of maximum IR drop for different VRM-chip gaps in the on-package VRM configurations

the distance between the VRM and the processor chip was fixed to 1 mm. To investigate the impact of this on power delivery performance, the distance was varied from 3 mm to 0.1 mm. Fig. 4 summarizes the results for 3 mm, 1 mm and 0.1 mm distances. As expected, if the distance is increased, the interconnect length for power supply increases, which eventually increases the IR drop.

### IV. COMPARISON OF TRANSIENT NOISE FOR DIFFERENT CONFIGURATIONS

The PDN of a system typically contains many inductive elements. Evaluating the transient i.e.,  $L \frac{di}{dt}$  noise of a system is thus important for verifying the noise levels. In this section, for different configurations, step response of the system will

be shown. The supply voltage rises from 0 V to 1 V with a rise time of 1 ns. Fig. 5 shows the transient noise profile for multiple on-package VRMs. As expected, with increased number of VRMs surrounding the chip, there is less PSN. In all the cases, the transient noises generated from the interaction of capacitive and inductive (mainly package) elements oscillate and settle down to the DC IR drop value of the corresponding case. The second droop is suppressed by the discrete decaps placed on the package. That is why the most dominant transient droop in all the cases is the first droop noise. The four on-package VRMs case achieves almost 24.45% improvement in PSN compared to the single on-package VRM case. When

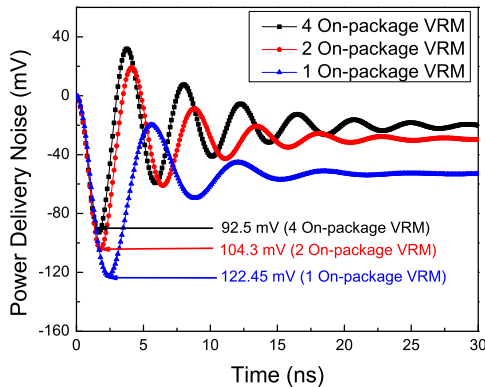


Fig. 5: Comparison of transient noise for different on-package VRM configurations

the VRM chip is placed on the backside of the package, VRM-to-chip PDN is mostly dominated by package vias and bumps. Package vias typically have low aspect ratio compared to TSVs; these TSVs contribute less to the resistance and more to the inductance of the system. Solder bumps between the package and the board play a similar role compared to the microbumps. Also, the number of microbumps is higher than the number of solder bumps. In the 3D IC chip-on-VRM case, the VRM is directly supplying power from the bottom of the chip. Hence, the inductive components are the TSVs in the VRM chip, and the microbumps between the VRM and the active chip. These are minimal compared to the inductive components in the other cases described in this study. In both of the cases, the package is less involved, which reduces the overall package parasitics in the PDN. Fig. 6 compares the best case from the on-package VRM cases with the backside-of-the-package and 3D IC chip-on-VRM configurations. For the backside-of-the-package VRM case, the maximum PSN is 82.64 mV. This itself is 10.65% improvement compared to the four on-package VRMs case. The 3D IC chip-on-VRM case provides a maximum PSN of 58.8 mV.

Throughout the paper, we observe that the transient noise is dominated by the first droop noise. This noise is dependent on the on-chip decap allocation. Throughout this paper, a decap density of 5.3 nF/mm<sup>2</sup> has been used for the analysis. Typically, on-die decap can take 20-30% area depending on the available space [17]. Moreover, depending on the type of capacitors used, the decap density can vary [18]. Typically using MOS capacitors, a decap density of 10-20 nF/mm<sup>2</sup> can be achieved. The four on-package VRMs case, the 3D

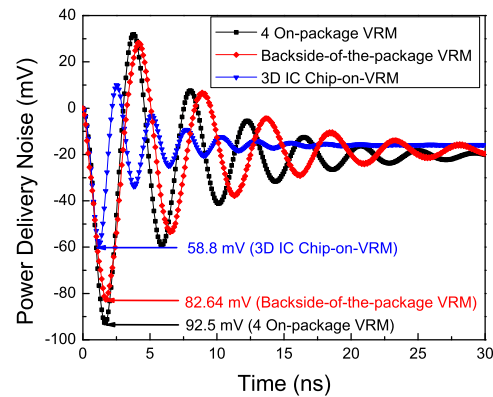


Fig. 6: PSN comparison for different key benchmarks

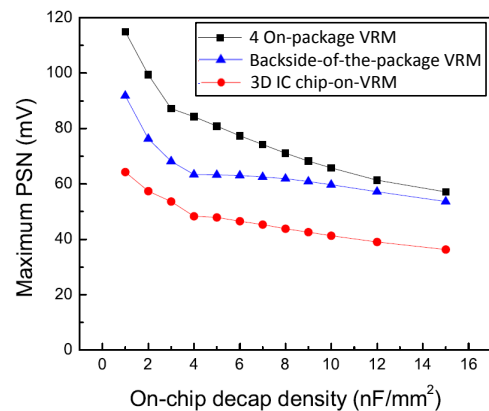


Fig. 7: Maximum PSN of some key configurations for different on-chip decap density

IC chip-on-VRM case, and the backside-of-the-package VRM case have been simulated for a varying decap density. The density is varied from 1 nF/mm<sup>2</sup> to 15 nF/mm<sup>2</sup>. To simplify the analysis, uniform power density has been considered. Fig. 7 summarizes the results from this study. As expected, with increased decap allocation, the PSN decreases. For the 3D IC case, the maximum PSN reduced from 64 mV for 1 nF/mm<sup>2</sup> to 36 mV for 15 nF/mm<sup>2</sup>. The other two cases follow a trend similar to this.

## V. CONCLUSION

This paper performs a power delivery network analysis for different benchmark configurations including voltage regulator modules. Multiple on-package VRMs, 3-D IC chip-on-VRM, and backside-of-the-package VRM cases are studied. The latter two cases enable supplying power directly from the bottom of the chip. Because of the proximity from the power supply to the active circuitry, the power delivery noise of the 3D IC chip-on-VRM case and the backside-of-the-package VRM case are the least. With distributed on-chip decoupling capacitor and package level discrete decaps, the PSN is minimized in all the configurations. The impact of on-chip decap density variation is also quantified. For 3D IC chip-on-VRM case with uniform current density, 25% improvement in PSN is possible if three times more decap is used compared to the one used for this analysis.

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