Ultralow-Power High-Performance Si Photonic Transmitter

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Abstract: We report a 320fJ/bit transmitter made of a Si microring modulator flip-chip bonded to a CMOS driver. The transmitter consumes only 1.6mW power, and exhibits a wide open eye with extinction ratio >7dB at 5Gb/s.

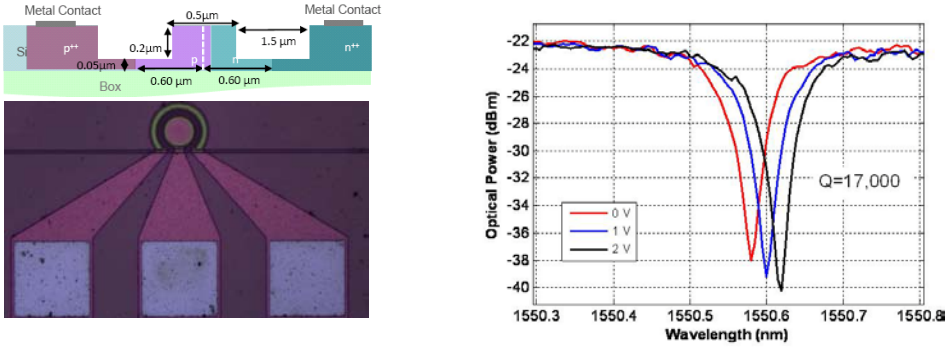
OCIS codes: (250.7360) Modulators; (200.4650) Optical interconnects; (130.6622) Subsystems integration and techniques

1. Introduction

Silicon photonic links are a promising solution to removing the communication bottleneck in future many-core, multi-chip high-performance computing systems, owing to its potential advantages of low latency, high bandwidth, high density, and low power consumption [1]. A key task for the Si photonics community is to aggressively scale down the on-chip power consumption for the entire link, including all the electronic circuits, from currently ~10 pJ/bit to ~100 fJ/bit in the near future. This not only calls for innovative optical devices [2] and system architectures [1], but also demands novel circuit designs and integration techniques to enable high-speed interconnects with extremely low power. In this paper we report a 320fJ/bit transmitter that combines a Si ring modulator that employs reverse-biased PN junction modulation with only 50fF junction capacitance, a 90nm CMOS driver that provides 2V voltage swing, and a flip-chip bonding technique that integrates the modulator and the driver with very low electrical parasitics. With only 1.6mW power consumption, the integrated and digitally clocked transmitter operates at 5Gb/s with wide open eye and >7dB extinction ratio, and has achieved error-free transmission for over 2 hours without active resonator bias tuning.

2. The Si ring modulator

To achieve low power consumption for the transmitter, it is desirable to have an optical modulator with very low capacitance. There are several promising modulator candidates, including Si microdisk modulators (reported 85fJ/bit) [3], Franz-Keldysh effect GeSi modulators (reported 50fJ/bit) [4], carrier-injection Si ring modulators [5], GeSi quantum well modulators [6], and evanescently coupled III-V modulators [7]. Note that the prior reported energy/bit [3-4] were for switching energy of the device alone, and didn't include the static and dynamic energy consumed by the whole driver circuit. In this work we used a ring modulator with a reverse-biased PN junction modulation. Our previous simulation result [1] has indicated that Si ring modulators with reverse-biased PN junction can be designed for 15Gb/s modulation, with compact footprint (~100 μm^2), very small capacitance (~15fF), low voltage swing (~2V), high extinction ratio (~7dB) and low optical loss (~2dB at on-state). Our Si ring modulator chip was designed and fabricated at Kotura, Inc [8]. Fig. 1(a) shows a cross-sectional diagram of the phase modulation waveguide, and a top-view photo of the device. The radius of the ring modulator used in this work was 15μm.

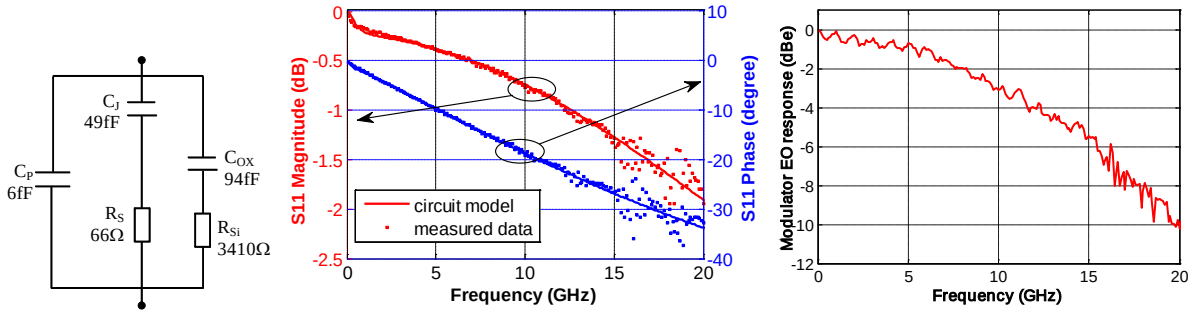


(a) (b)

Fig. 1. (a) Cross-sectional diagram of the phase modulation waveguide, and top-view photo of the microring modulator. (b) Resonance spectrum at different voltages (reverse bias to the PN junction) of the ring modulator.

DC characterization was performed on die using electrical probe and lensed fibers. Fig. 1(b) shows the resonance spectrum at different reverse bias voltages of 0V, 1V and 2V respectively. The measurement results indicate a quality (Q) factor of ~17000 for the ring resonator, and a voltage-induced wavelength shift of ~18pm/V. When operated around 1550.62nm wavelength and with a voltage swing from 0V to 2V, this ring modulator can achieve >10dB DC extinction ratio and ~2 dB insertion loss at on-state.

The high-speed behavior of the ring modulator has been carefully studied using a circuit model extracted by curve-fitting the measured S11 data. In this circuit model shown in Fig. 2(a), C_P represents the capacitance between the electrodes (mostly due to the contact pads) through the top dielectrics and the air, C_J denotes the capacitance in the reverse-biased diode junction, R_S denotes the diode series resistance, C_{OX} denotes the capacitance through the dielectric and Si layers, and R_{Si} is the resistance in Si layer. The parameter values in Fig. 2(a) were extracted at 0V, indicating a junction capacitance of 49fF. The curve fitting result is shown in Fig. 2(b). The same data analysis at 1V and 2V bias indicated a slightly smaller junction capacitance, consistent with our expectation. Using the extracted circuit model, we calculated a switching energy of the ring modulator at ~100fJ/bit when modulated by a pseudo-random data with a 2V swing at 5Gb/s (note that C_{OX} can be partially charged and discharged during the modulation). This switching energy can be readily lowered by reducing the ring modulator size.



(a) (b) (c)

Fig. 2. (a) Small-signal circuit model for reverse-biased ring modulators built on SOI substrate. The marked parameter values are for 0V bias. (b) Curve-fitting of the measured S11 at 0V using the circuit model in (a). (c) Measured modulator frequency response at 0V.

Small-signal modulation bandwidth has also been measured for the ring modulator using a microwave network analyzer and a reference detector with known frequency response. The measured result in Fig. 2(c) indicates a 3dB bandwidth of 10 GHz at 0V, with the wavelength set at ~1550.6nm in the resonance spectrum shown in Fig. 1(b). The modulation bandwidth of the device is subject to both the RC limit, which is ~24GHz estimated from the circuit model (with a 50Ω source), and the photon lifetime limit, which is ~11.4GHz based on the measured quality factor. Clearly, the photon lifetime represents the primary limit to the modulation bandwidth for this device.

3. The integrated transmitter

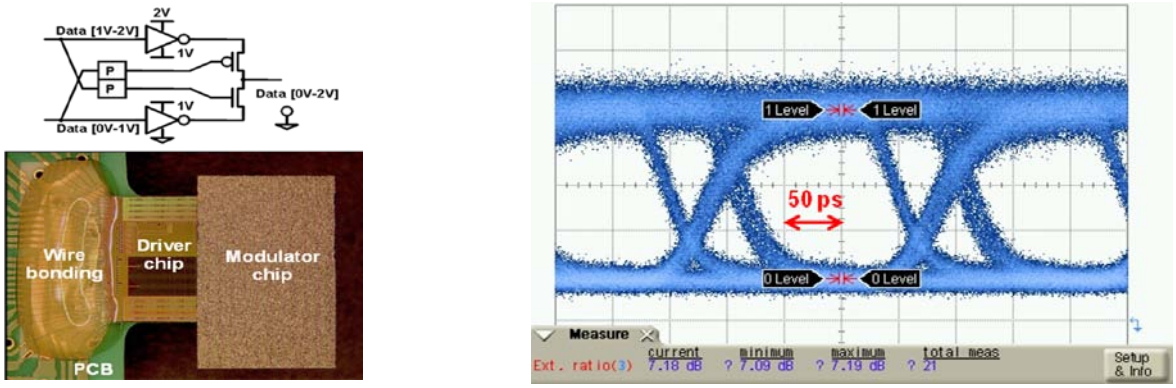
Si photonic devices and VLSI circuits can potentially be integrated on the same chip to minimize electrical parasitics and lower manufacturing cost. However, state-of-the-art CMOS circuits are now popularly built on bulk Si substrates; while photonic devices normally require SOI substrates for optical waveguides. While this monolithic integration challenge is being actively tackled [9], here we use a flip-chip bonding technique [1], which allows best-of-the-breed performance for both the photonic devices and the VLSI circuits.

Our modulator driver was fabricated using TSMC 90nm CMOS technology. A simplified circuit diagram is shown in Fig. 3(a). To achieve 2V swing with 1V transistors, a cascode driver circuit was designed [10]. The input signal is fed into two inverters with different voltage references, which in turn drive the rails of a final driver. With proper timing, each transistor sees only 1V even though the circuit provides an output swing of 2V across the device.

To bond the modulator chip with the VLSI driver chip, both chips were first processed to add under-bump-metallization (UBM) to the bonding pads using electroless plating to serve as both strong adhesion layer and diffusion barrier, and to enable microsolder bumps for low-resistance contact to the pads. Low profile and small footprint microsolder bumps were then added to the pads on the modulator chip with a few microns of vertical compliance. The two post-processed chips were then flip-chip bonded together by thermocompression. The microsolder connections were measured to have <1Ω resistance; and the parasitic capacitance due to bonding pads and microsolder bumps is estimated to be ~20fF.

The clocked hybrid transmitter chip was die-attached and wire-bonded to a test PCB board for power, control, and high speed digital I/O connections. A photo of the complete assembly is shown in Fig. 3(a). With the on-chip digital buffers and the clock distribution turned on, the VLSI chip generates ~1W heat, which may cause difficulty

to the high-speed testing since ring resonators can be very sensitive to temperature change. To combat this problem, the photonic chip was closely contacted with a copper heat sink. The resulted optical output eye of the transmitter is shown in Fig. 3(b), tested with 5Gb/s PRBS31 data. The double falling edge is due to a timing error related to non-optimal clock loading, which can be easily corrected with timing and layout optimizations. The optical eye is wide open, with >7dB extinction ratio. Using an EDFA (to compensate for the large fiber coupling loss) and a reference receiver, we achieved stable error-free transmission at 5Gb/s for over 2 hours without active resonator bias tuning or temperature control, indicating a bit-error-rate $<10^{-13}$. The total transmitter power consumption was measured as 1.6mW from the power supply voltages and currents. This corresponds to 320fJ/bit for the entire transmitter including the ring modulator and its CMOS driver, as well as any excess power required to drive circuit parasitics including internal wiring and flip-chip pads.



(a) (b)

Fig. 3. (a) A simplified circuit diagram for the modulator driver, and a photo of the hybrid-bonded transmitter wire-bonded to a test PCB board. (b) Eye diagram of the integrated transmitter tested with 5Gb/s PRBS31 data showing an extinction ratio of >7dB.

4. Conclusions

An ultralow-power (320fJ/bit) hybrid integrated transmitter with >7dB optical extinction ratio at 5Gb/s has been demonstrated. The transmitter includes a small (15μm radius) Si microring modulator flip-chip bonded to a 90nm CMOS driver. With a simple heat sink and enclosed testing environment, we have achieved error-free transmission at 5Gb/s for over 2 hours without active resonator bias tuning or temperature control. Lower power and higher data rate can be readily achieved by improvements based on the demonstrated technology. This is a significant step towards a complete optical link with a few hundreds of fJ/bit power, which is critical for future high-performance computing systems. This work is supported by DARPA MTO office under UNIC program supervised by Dr. Jagdeep Shah under the Agreement No. HR0011-08-09-0001.

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