10 Gbps, 530 fJ/b optical transceiver circuits in 40 nm CMOS

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This paper describes 10 Gbps optical modulator and receiver circuits designed for high energy efficiency in a 40 nm process. The transmitter consumes 135 fJ/b when bonded to an external silicon photonic ring modulator. The receiver, at -15 dBm sensitivity, consumes 395 fJ/b when bonded to an external photodiode.

Introduction

As silicon nano-photonic links continue to improve in both energy efficiency and areal density, they represent new opportunities for system designers. For example, silicon photonics could connect together VLSI chips on an optically-enabled silicon wafer substrate, creating a densely coupled high-performance processing and memory platform [1].

Here we present work on circuits for silicon photonic links. In our systems, we bond VLSI chips using fine-pitch solder to silicon photonic chips [2]. This "hybrid" approach, using 1.5 μm external lasers, obviates the need to integrate optical devices into a CMOS logic foundry, and allows the circuits to be built in a suitably advanced process technology.

Transmitter

To a driver, silicon photonic ring modulators present a reverse-biased diode capacitive load, and require 2 V of swing to achieve a sufficient extinction ratio. Figure 1 shows the parasitics for a 12 μm radius oval ring driven by a cascoded driver circuit [3], which uses a capacitor and keeper (with adjustable supplies) to copy the data stream with a +1 V shift. Pulse generators (as in [4]) limit overvoltage stress on the output devices. Figure 2 shows a measured optical eye for 10 Gbps PRBS data. No errors were observed in over 10^{13} bits sent, and measured power (excluding tuning) was 1.35 mW.

The resonant rings, with a measured Q > 10K at 1.5 μm, are highly sensitive to process and temperature variability. To compensate for these effects, the transmitter includes a thermal tuner that drives a fixed 0-4 mA current into a 400 Ω metal resistor on the optical chip (anticipated required current is < 0.5 mA). The tuner uses a 12-b DAC to adjust the tuning current: four bits divide the 4 mA current into sixteen steps of 0.25 mA each, and an 8-b sigma-delta converter running at 300 MHz dithers between two consecutive current steps. Figure 3 shows measured output current, leading to several hundred pico-meters of measured resonance wavelength shift.

Receiver

Figure 4 shows a photodiode driving a trans-impedance amplifier (TIA), whose output voltage is sliced using two interleaved clocked StrongArm sense-amplifiers, each running at 5 Gbps. A DLL based on current-starved inverters places the sense-amplifier clock in the middle of the TIA output data eye. The sense-amplifier outputs feed a one-bit FIFO/phase buffer that synchronizes them to a system datapath clock.

DACs: The receiver uses four 8-bit resistor ladder DACs to define critical voltages: two set the voltage references for the sense-amplifiers; one sets the DLL delay; and one shunts an average signal current from the single-ended photodiode current, thus setting the TIA bias to its nominal zero input high gain state. A digital finite state machine (FSM) adjusts each of the DACs periodically. Two separate supply regulators provide 1 V from a 1.3 V supply to the TIA, DACs, and DLL with 18 dB worst-case noise rejection, and help to isolate the single-ended TIA from any power supply noise.

TIA: Allowing for a combined photodiode and hybrid bond capacitance of 60 fF (worst-case), and assuming a photodiode responsivity of 0.7 A/W, the three-stage inverter-based TIA (Figure 5, [5]) is designed for a trans-impedance gain of 4 kΩ, a 7 GHz bandwidth, and is sized to achieve a BER of 10^{-12}.

Calibration: All links are calibrated simultaneously through a global "re-calibrate" signal, leveraging the compact and mesochronous nature of the total system [6]. The calibration FSM consists of an adder and four 8-bit registers, each driving one DAC. During calibration, all transmitters send a 0101… clock pattern, and the receiver goes through four steps:

1. Disconnect photodiode from TIA, so TIA output sits at its nominal high-gain bias (at zero input current). Adjust voltage reference DACs to minimize sense-amps offsets.
2. Reconnect photodiode; average the TIA output through a *RC* filter. Using the RX comparators, set input shunt to pull the average current from the TIA input, thus driving the TIA output back to its nominal high-gain bias.
3. Remove low-pass *RC* filter and adjust DLL delay: first, shift sense-amp clock into quadrature, and gradually increase DLL delay until output dithers, signaling the transition edge. Remove the clock quadrature shift.
4. Selectively insert a latch in the 1-bit FIFO to synchronize the DLL clock with the system datapath clock.

This four-step calibration avoids the power, bandwidth, and latency overhead of encodings such as 8b10b. The calibration runs every 1 ms, and presents less than 1% overhead.

Isolation switch: Using a simple MOS switch for step 1 above would severely degrade operational bandwidth due to its high on-resistance. Instead we employ a three device switch shown in Figure 5. During calibration, a small Mp1 closes the feedback loop. In normal operation, Mn1 and Mn3 form the TIA feedback resistance and enclose the on-resistance of Mn2. This adds a high frequency input pole to the amplifier, and produces slight peaking at the first stage output due to increased feedback phase shift.

RC filter: A mux (Figure 5) allows TIA output averaging for step 2. The chosen *RC* value attenuates ripple >20 dB at 5 GHz and allows settling in one calibration clock period. The mux on-resistance negligibly affects the bandwidth, as the TIA output pole is not dominant. However, the limited ability of the NMOS switches to pass high voltages slightly hinders the TIA bias calibration by injecting a small voltage offset.

Figure 6 shows the eye diagram at the TIA output, when

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using a photodiode that produced a signal at -15 dBm with a 10 dB extinction ratio. Because the TIA output is not accessible from test equipment, this eye diagram used the sense-amp reference input to sweep voltage, and the DLL settings to sweep time. The TIA, DLL and DACs together consume 2.53 mA from a 1.25 V supply regulated to 0.95 V. The sense-amps and FIFO phase buffer added another 0.8 mA from a 1.0 V supply, resulting in a total receiver power of 3.95 mW. For these measurements, the receiver was bonded to a evanescently coupled Ge-PIN waveguide photodetector, using epitaxial Ge grown atop a silicon waveguide [2].

References

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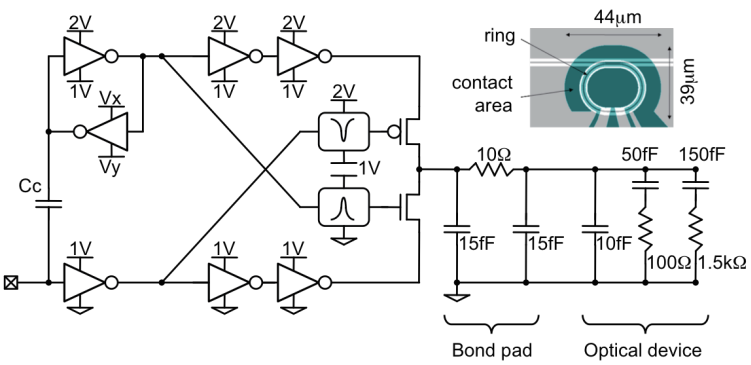

Figure 1: Driver with modulator load

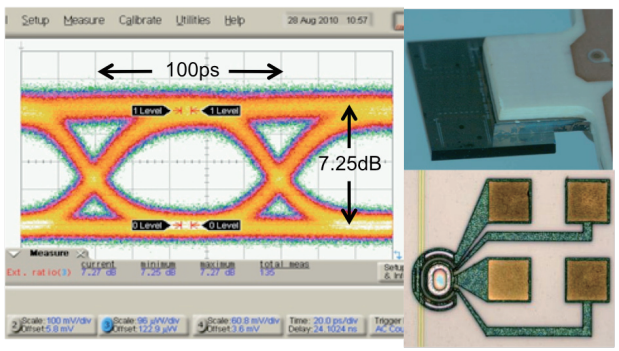

Figure 2: Measured eye diagram (left), hybrid bonded chips (right)

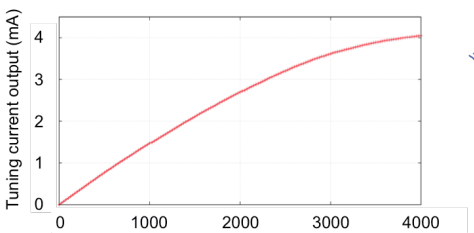

Figure 3: Measured tuning current into 400 Ω versus control code

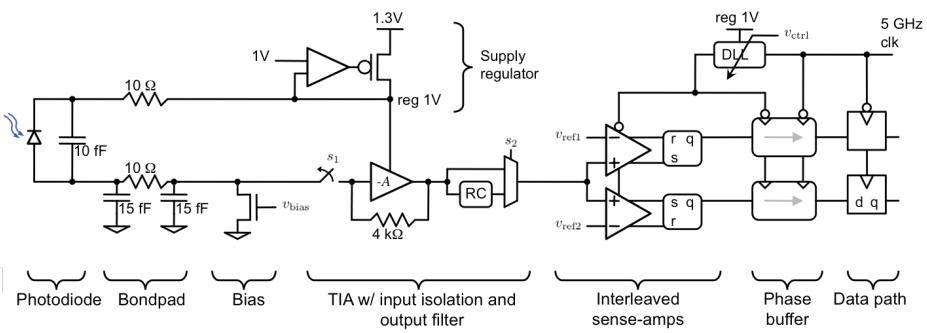

Figure 4: Block diagram of receiver bonded to photodiode. Four 8b DACs and a finite state machine (not shown) control the two calibration controls (s_1 and s_2), the two sense-amp reference voltages (v_{ref1} and v_{ref2}), the DLL delay (v_{ctrl}), and the TIA bias (v_{bias})

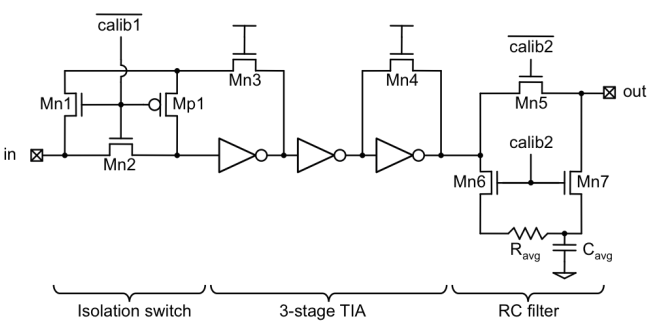

Figure 5: Detail of isolation switch, TIA, and RC filter

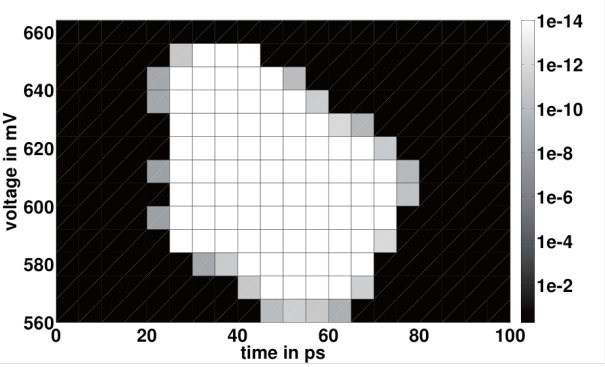

Figure 6: Measured eye opening after TIA