Flying and Decoupling Capacitance Optimization for Area-Constrained On-Chip Switched-Capacitor Voltage Regulators

***Abstract*— Switched-capacitor (SC) voltage regulators are widely used in on-chip power management, due to the high efficiency at integer-ratio step-down and feasibility of integration. Theoretical analysis and optimization for SC DC-DC converters have been presented in prior works, however optimization of different capacitors, namely flying and input/output decoupling capacitors, in SC voltage regulators (SCVRs) under an area constraint has not been addressed. In this work, we propose a methodology to optimize flying and decoupling capacitance for area-constrained on-chip SCVRs to achieve the highest system-level power efficiency. Considering both conversion efficiency and droop voltage against fast load transients, the proposed model determines the optimal ratio between flying and decoupling capacitance for fixed total area. These models are validated with integrated 2:1 SCVR implementations in both 65nm and 32nm CMOS. Experiments show high model accuracy on efficiency and droop modeling for a broad range of flying and decoupling capacitance. The maximum and average error of the predicted optimal ratio between flying and decoupling capacitance is 5% and 1.7%, respectively.**

Keywords— Switched-capacitor voltage converter; integrated voltage regulator; power conversion efficiency; voltage droop; capacitance optimization; area-constrained power management.

I. INTRODUCTION

On-chip power management has become increasingly important in modern processor designs for the pursuit of fine-grain dynamic voltage scaling, efficient power delivery, fast load regulation, and simpler package/board design. In order to address the challenges in power supply design, various power conversion circuits and regulation schemes have been proposed. Buck converters with high-quality off-chip or package-integrated inductors have been widely used in portable devices for their high power efficiency [1], but are limited by their on-chip integration capability due to a lack of high-quality on-chip inductors [2]. Linear regulators or low dropout regulators (LDO) with digital, analog, or mixed-mode schemes have also been well presented in recent years [3][4]; however, the linear dependence of efficiency on the input and output voltage values makes LDO an unfavorable choice for high step-down conversion. In comparison, SC voltage converters can offer a fully integrated solution with high-quality on-chip capacitors at integer conversion ratios [5-8]. Furthermore, recently proposed SC converter designs with binary and rational conversion ratios have largely enhanced the efficiency for a wide range of output voltages [9].

Theoretical analysis on efficiency and optimization of SC voltage converters have been conducted in several prior works [10-14]. The output impedance models of fast switching loss and slow switching loss conditions for different conversion topologies was proposed in [10] to analyze the finite conductance of switches and the charging/discharging operations. In [11], the gate capacitance loss, CMOS capacitor bottom-plate loss, and the interleaving ripple-reduction technique were analyzed and optimized. The authors of [12] derived the converter output resistance and analyzed the switch width and switching frequency to achieve optimal efficiencies in SC converters. Regulation analysis of high-power SC converters is performed in [13] using a charge-balance transient-calculation modeling method, however closed-form analysis of droop voltage against abrupt load transients has not been presented. The trade-off of using flying capacitance and decoupling capacitance was analyzed in [14], but an integrated analysis considering both efficiency and droop is not presented.

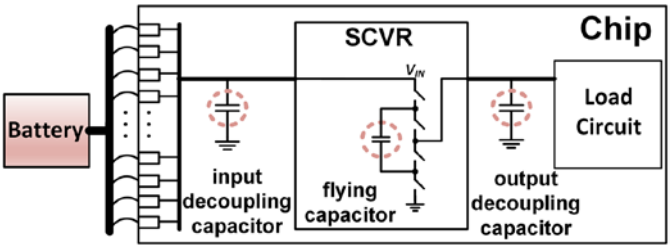

Figure 1. Illustration of the flying and decoupling capacitors in an on-chip SCVR that is connected from a battery.

Most standalone SCVRs in the literature are not designed with specific area constraints. While power densities are reported, more often than not, decoupling capacitance is not included in the overall area. However, in practical scenarios of SCVRs being employed in processors or embedded systems, strict area constraint usually exists, and the area of the SCVR plus the area of input/output decoupling capacitance need to fit in the given real estate. Considering that most of the SCVR area is devoted to capacitance [5-6], selection of appropriate flying capacitance versus decoupling capacitance directly affects the conversion efficiency, output current, and output droop voltage against load transients. The capacitors in SCVRs that will be investigated in this work are illustrated in Figure 1. Integrating the effects of both conversion efficiency and output droop into system-level power, we present an area-constrained analysis and optimization of flying and decoupling capacitors in on-chip SCVRs. The proposed modeling, analysis, and optimization work has the following contributions:

- SC converter efficiency over a wide range of flying capacitance as well as output voltage droop over a wide range of decoupling capacitance are modeled.
- We propose a new figure-of-merit for system-level power efficiency considering both conversion efficiency and minimum supply voltage of load circuits, to optimize the

flying capacitance versus decoupling capacitance ratio of SCVRs under fixed area constraints.

- The proposed models and figure-of-merit are validated for various load current values with an area constraint, in both 32nm and 65nm CMOS process, which show well-matched results with high accuracy.

The remainder of this paper is organized as follows. Section II presents the theoretical analysis of SCVR, and discusses the proposed figure-of-merit to optimize system-level power efficiency. The validation of the proposed analysis with 65nm and 32nm CMOS simulations and design optimization is shown in Section III. Section IV concludes the paper.

II. ANALYSIS AND OPTIMIZATION OF AREA-CONSTRAINED SCVR

In this section, the loss analysis and modeling on the efficiency and droop voltage of SCVRs is provided.

A. Analysis of Conversion Efficiency and Output Current

The efficiency and power density of an integrated SC voltage converter is directly influenced by the capacitor technology of the CMOS process, besides the conversion ratio and topology. Different capacitor technologies, such as MIM (metal-insulator-metal), MOS (metal-oxide-semiconductor), and DT (deep trench) offer different efficiency and current density options for SC converter design, while a trade-off exists between these two design objectives for each capacitor technology. The sources of power loss in SC voltage converters include the following [10-12]:

(1) charging and discharging behavior of the flying capacitor causes slow switching loss (SSL) due to the voltage ripple at the output, which is inversely proportional to the switching frequency and flying capacitance and is set by:

$$P_{SSL} = \frac{I_L^2}{N_{SSL} f_{sw} C_{fly}}, \tag{1}$$

where I_L is the load current of the SC converter, f_{sw} is the switching frequency, and C_{fly} is the flying capacitance. N_{SSL} is the coefficient depending on SC converter topology and $N_{SSL} = 4$ for 2:1 SC converter.

(2) current through the on-resistance of the non-ideal switches gives fast switching loss (FSL), which is proportional to the switch width and is set by

$$P_{FSL} = I_L^2 \frac{R_{on}}{W_{sw}} N_{FSL}, \tag{2}$$

where W_{sw} is the switch width of the SC converter, and R_{on} is the on-resistance of the switch determined by the CMOS process. N_{FSL} is the coefficient depending on SC converter topology and $N_{FSL} = 2$ for 2:1 SC converter.

(3) parasitic capacitance of the flying capacitor causes bottom-plate loss, because it is charged from the supply in one phase, and discharged to ground in the other phase. Such loss is proportional to the total bottom plate capacitance as well as the switching frequency and is set by:

$$P_{bott} = N_{bott} V_o^2 C_{bott} f_{sw}, \tag{3}$$

where N_{bott} is the number of bottom plates, C_{bott} is the bottom-plate capacitance, and V_o is the SC converter output voltage.

(4) the parasitic capacitance of the SC switches causes switching loss due to its charging and discharging behavior, which is proportional to both the switch width and frequency and is set by:

$$P_{sw} = k_{drive} N_{sw} C_{sw} V_{sw}^2 f_{sw}, \tag{4}$$

where k_{drive} is the constant of proportionality accounting for the pre-drivers, C_{sw} is the parasitic capacitance of the switch, N_{sw} is the number of switches that is conducting, V_{sw} is the supply voltage of the driver stages.

The total power loss of a SC converter is the sum of the four aforementioned loss terms:

$$P_{loss} = \frac{I_L^2}{N_{SSL} f_{sw} C_{fly}} + I_L^2 \frac{R_{on}}{W_{sw}} N_{FSL} + V_o^2 C_{bott} f_{sw} + k_{drive} N_{sw} C_{sw} V_{sw}^2 f_{sw} \tag{5}$$

The optimal conversion efficiency for different load currents with a given flying capacitance can be determined with the minimization of P_{loss} by varying switching frequency and switch width of the SC converter:

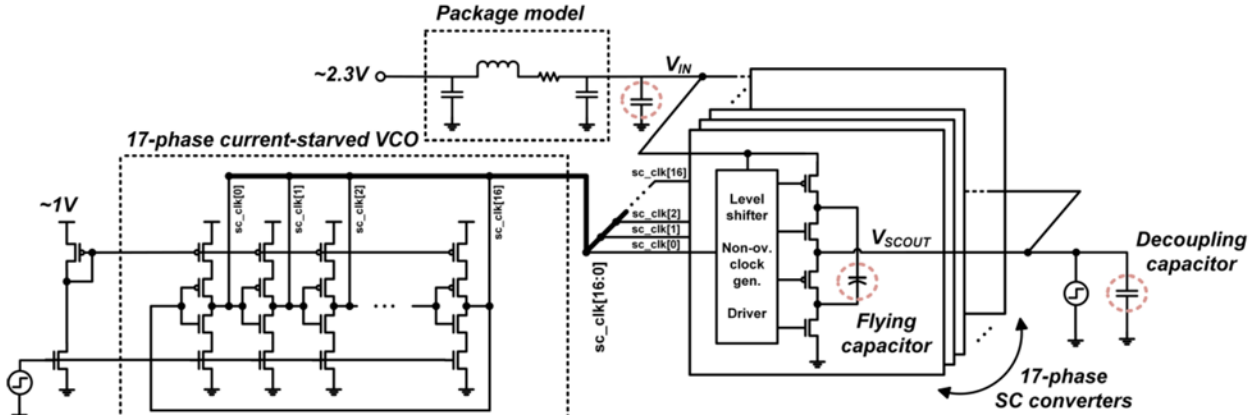

Figure 2. Schematic of SC voltage regulator used for droop analysis against load transients.

$$\eta_{opt} = \left(1 + \frac{P_{loss\_min}}{P_{load}}\right)^{-1}, \quad (6)$$

where P_{loss_min} is the minimum value of P_{loss} for a given load current and flying capacitance, and P_{load} is the output power of the SC converter and is set by:

$$P_{load} = V_o I_L \quad (7)$$

Using Matlab 'fmincon' optimization functions, the minimum power loss P_{loss} is determined with interior-point algorithm for various load current and flying capacitance values and the optimal efficiencies for 2:1 SC converter are thereby obtained according to Eq. (6).

B. Analysis of Droop Voltage against Load Transients

The load transient behavior of a SC voltage regulator is determined by the operation of the SC converter, the input/output decoupling capacitance and the closed-loop regulation scheme. To analyze the effect of decoupling capacitance on SCVR output droop, we performed droop simulations in 65nm CMOS with MIM capacitors used for input and output decoupling capacitance. As shown in Figure 2, the 17-phase interleaved SC converters are driven by a VCO that provides a frequency modulation scheme against a load transient from 102mA to 1.02A in 10ns. The droop voltage simulation results for 1nF-13nF of input and output decoupling capacitors are shown in Figure 3. As can be seen, for the same amount of capacitance (and thus area), the effect of input decoupling capacitance on the output droop is considerably weaker than that of the output decoupling capacitance. In addition, for certain types of high-density capacitors, such as DTCAP, there could be reliability issues when a very high voltage is applied across the capacitors, such as the input voltage. Due to these reasons, the input decoupling capacitance is not considered in this work.

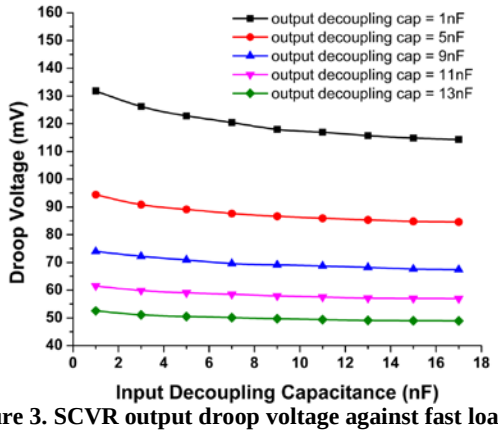

Figure 3. SCVR output droop voltage against fast load transients with MIM input and output decoupling capacitances from regulator simulation (Figure 2) in 65nm.

In the operation of the SC regulator, the load current is equivalent to the sum of the SC output current and the current through the decoupling capacitance. During the steady state of the SCVR, when the current, switching frequency, switch width and other modulated parameters are kept constant, the load current is mainly provided by the flying capacitor. The minimum output voltage value in continuous cycles of the switching clocks is set by [11]

$$V_o(t) = \frac{Vi}{2} - \frac{i_{sc}(t)}{4C_{fly} \cdot f_{sw}} \quad (8)$$

During a load transient response, however, the portion of current supplied by the output decoupling capacitor first abruptly increases and then decreases as the SC converter outputs more current with a particular regulation scheme. The decoupling capacitor current $i_{cp}(t)$ is set by:

$$i_{cp}(t) = C_{cp} \cdot \frac{d\,V_o(t)}{dt}, \quad (9)$$

where C_{cp} is the decoupling capacitance. At the output node of the SCVR, three current paths exist: the SC converter current, the decoupling capacitor current and the load current. According to Kirchhoff's current law (KCL), the three current values have the following relationship during the load response:

$$N \cdot i_{SC}(t) + i_{cp}(t) = N \cdot i_L(t), \quad (10)$$

where N is the number of interleaved phases in the SCVR, $i_{SC}(t)$ is the single-phase SC converter output current and $i_L(t)$ is the load current.

With a specific regulator scheme, SC input voltage Vi, flying capacitance C_{fly}, switching frequency f_{sw}, decoupling capacitance C_{cp}, the number of interleaving phases N and load current step $i_L(t)$ are already known. Then, using Eqs. (6)-(8), a differential equation set is formed that has $V_o(t)$, $i_{SC}(t)$ and $i_{cp}(t)$ as unknown variables. Assuming that the load current increases from I_0 to I_1 in a time period of Δt, starting at time 0, the time-domain single-phase load current is expressed as:

$$I_L(t) = \frac{I_1 - I_0}{\Delta t} \cdot t + I_0 \quad (11)$$

The regulation scheme of the SCVR is modeled as a sudden increase of switching frequency from f_{sw0} to f_{sw1} at $\Delta t/2$, without losing generality. Substituting Eq. (11) into the differential equation set above leads to a single-variable differential equation that is obtained as follows:

$$\frac{K_0 V_i}{2} - K_0 \cdot V_o(t) - C_{cp}\frac{d\,V_o(t)}{dt} = \frac{I_1 - I_0}{\Delta t} \cdot t + I_0, \quad (12)$$

where $K_0 = 4C_{fly} \cdot f_{sw0}$ is a constant, and the initial condition is:

$$V_o(0) = \frac{Vi}{2} - \frac{I_0}{K_0} \quad (13)$$

By solving the differential equation above, the output voltage as a function of time can be derived as:

$$V_o(t) = \frac{C_{cp}(I_1 - I_0)}{N \cdot \Delta t \cdot {K_0}^2} \cdot \left(1 - e^{-\frac{K_0}{C_{cp}} \cdot t}\right) - \frac{I_1 - I_0}{K_0 \cdot \Delta t} \cdot t + \frac{V_i}{2} - \frac{I_0}{K_0}, \quad (14)$$

As the output voltage before the load response is given by Eq. (11), the droop voltage caused by the SCVR at time $\Delta t/2$ is set by:

$$V_{droop\_sc} = -\frac{C_{cp}(I_1 - I_0)}{N \cdot \Delta t \cdot {K_0}^2} \cdot \left(1 - e^{-\frac{K_0}{C_{cp}} \cdot t}\right) + \frac{I_1 - I_0}{K_0 \cdot \Delta t} \cdot t \quad (15)$$

The derivation above can be understood intuitively: the second term in Eq. (15) represents the output voltage decrease caused by the operation of the SC converter, and the first term

represents the droop voltage from the contribution of the output decoupling capacitance.

In realistic conditions, the SC input voltage Vi is not constant due to the voltage drop $L \cdot di/dt$ caused by the package inductor. The relation between the off-chip supply voltage and converter input is set by:

$$V_i(\mathrm{t}) = V_{supply} - \frac{L_{pck}}{2M} \cdot \frac{d\, i_{sc}(t)}{dt}, \tag{16}$$

where M is the number of I/O pins and L_{pck} is the inductance of each pin.

For a load step from I_{SC0} to I_{SC1} in a period of Δt, the additional amount of droop caused by the package inductor is set by:

$$V_{droop\_ind} = \frac{I_{sc1} - I_{sc0}}{2M} \cdot \frac{L_{pck}}{\Delta t} \cdot e^{-\frac{C_{cp}}{C_0}}, \tag{17}$$

where is C_0 a fitting parameter obtained from simulation data to characterize the influence of decoupling capacitance. The package resistance can affect the DC error between the steady states, but its influence on load-response droop voltage is negligible when the DC error is small, which is the case for all the transient simulations analyzed in this work

Overall, the droop voltage of the on-chip SCVR is modeled as:

$$V_{droop} = -\frac{C_{cp}\,(I_1 - I_0)}{N \cdot \Delta t \cdot {K_0}^2} \cdot (1 - e^{-\frac{K_0}{C_{cp}} t}) + \frac{I_1 - I_0}{\Delta t \cdot K_0} \cdot t + \frac{I_{sc1} - I_{sc0}}{2M} \cdot \frac{L_{pck}}{\Delta t} \cdot e^{-\frac{C_{cp}}{C_0}} \tag{18}$$

C. *Proposed Figure-of-Merit for System-Level Power Optimization*

In order to evaluate the proposed optimization for an area-constrained SCVR design, we hereby propose a figure-of-merit (FOM), as shown below:

$$FOM = \frac{P_{out}}{P_{out} + P_{loss} + V_{droop} \cdot I_{avg}}, \tag{19}$$

where P_{out} represents the output power at a target load current and P_{loss} is the corresponding conversion power loss. I_{avg} represents the average current of the processor load, which depends on the workloads of different applications. Without losing generality, in this work, we assume I_{avg} to be the average value of the maximum load current I_{max} and the minimum load current is $0.1 \cdot I_{max}$, which becomes $0.55 \cdot I_{max}$. The minimum load current is set as 1/10 of the maximum load considering leakage current of processors, and also serves as the initial current for the load step response.

A SCVR compares its output voltage to a target reference V_{ref} and continuously modulates the converter to keep the output voltage as close as possible to V_{ref}. When abrupt load transients occur, SCVR can experience worst-case droop V_{droop}, which will bring down the output voltage to $V_{ref} - V_{droop}$. Since it is very difficult to precisely predict when the load transients will occur, to avoid any timing failure even when the droop occurs, $V_{ref} - V_{droop}$ needs to be the minimum supply voltage V_{min} for the digital load circuits. This means that, in conditions without abrupt load transients, V_{ref} needs to be positioned at $V_{min} + V_{droop}$ to prevent any timing failures considering potential droop. To that end, V_{droop} becomes the supply voltage margin of the digital loads, and $V_{droop} \cdot I_{avg}$ represents the additional output power that needs to be provided to the load circuits considering the SCVR output droop that can occur.

Assuming that a fixed die area is allocated to the total area of flying capacitors and decoupling capacitors, the ratio between the areas of the two capacitors that results in the highest figure-of-merit (FOM) can be obtained, which offers an optimal solution for the SCVR design. The modeling of FOM can be carried out with a combination of the proposed efficiency model and droop voltage model as follows:

$$FOM_{cal} = \left(\frac{1}{\eta_{opt}} + \frac{0.55 V_{droop}}{I_{max}}\right)^{-1}, \tag{20}$$

where η_{opt} and V_{droop} are the efficiency and droop values modeled in Section II.A and II.B, respectively.

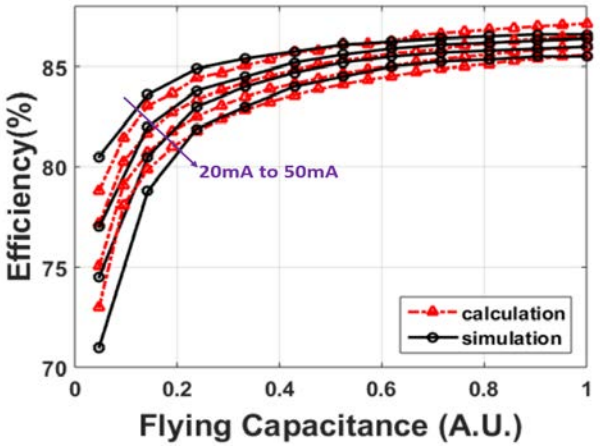

Figure 4. Simulated and calculated optimal efficiency with different flying capacitances at 20mA, 30mA, 40mA and 50mA load (per converter phase) cases in 65nm CMOS.

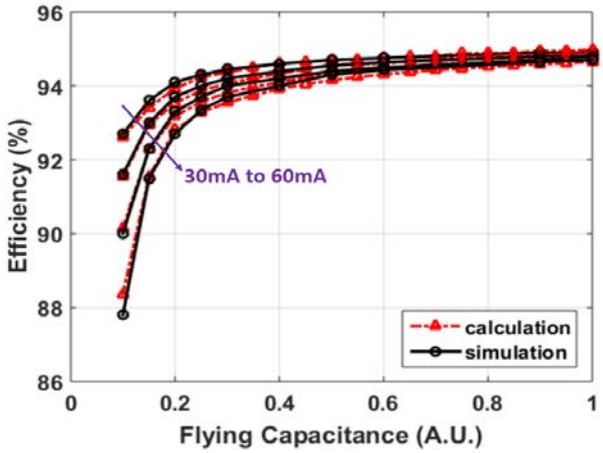

Figure 5. Simulated and calculated optimal efficiency with different flying capacitances at 30mA, 40mA, 50mA and 60mA load (per converter phase) cases in 32nm CMOS.

III. EXPERIMENTAL RESULTS

In this section, we provide experimental results obtained from circuit simulations in 65nm and 32nm CMOS, and show the comparison with the model predictions. The validation experiments are implemented with 2:1 SC converters due to its prevalence in high-efficiency SC converter designs [5, 8], and its application in rational-/binary-ratio SC converters [9].

A. Trade-Off between Efficiency and Current Density

In order to validate the efficiency and current density trade-off relation of 2:1 SC converters, a set of SC converter designs were implemented in 65nm CMOS with MIMCAP and 32nm CMOS with DTCAP, using the simulation setup in Figure 2. Each SC converter phase is driven by four ideal non-overlapping clocks with four-stage buffers. For each flying capacitance value, the switching frequency and width are swept as design variables to obtain the optimal efficiency for different output currents. Then, the flying capacitance value is swept to determine the optimal efficiencies for different flying capacitance values. The comparison of the model calculation with the simulated results in 65nm and 32nm are shown in Figure 4 and Figure 5, which includes multiple load current cases per SC converter phase, with a wide range of flying capacitance values. The results show that the model is reasonably accurate and the maximum efficiency error is less than 1.4% for a 21X range of flying capacitance in 65nm, and less than 0.4% for a 10X range of flying capacitance in 32nm.

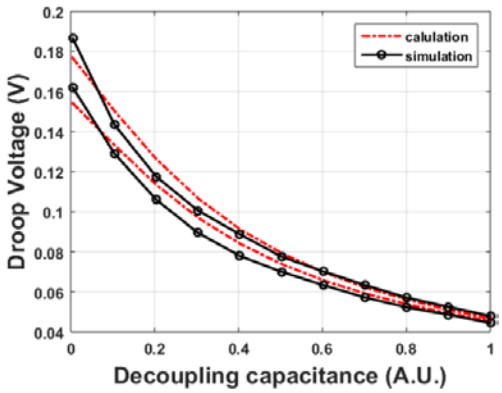

Figure 6. Simulated and calculated droop voltage of SCVR for 51-510mA, 10ns load step in 65nm CMOS for a 21X range of decoupling capacitance.

B. Droop Voltage Results with Output Decoupling Capacitance

To validate the accuracy of the droop voltage model for a wide range of decoupling capacitance, transistor-level simulations with regulation circuits are performed in both 65nm and 32nm CMOS. In the simulation setup (Figure 2), an output current source sets up a load step of 51mA to 510mA in 10ns and a decoupling capacitance is set as a design variable. The output voltage regulation is implemented with a control voltage step to provide an immediate increase of switching frequency so that the DC error of output voltage is minimized. By sweeping the output decoupling capacitance, different droop voltage values are obtained from simulations.

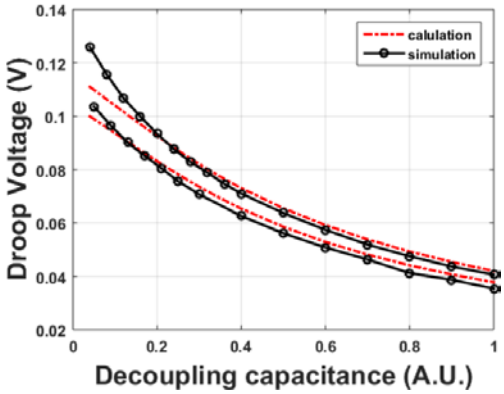

Figure 7. Simulated and calculated droop voltage of SCVR for 102-1020mA, 40ns load step in 32nm CMOS for a 10X range of decoupling capacitance.

The comparison of the model calculation and the simulation results in 65nm and 32nm CMOS are shown in Figure 6 and Figure 7, respectively, to show the accuracy of the model prediction. As shown in the prediction results, the proposed model for droop voltage against load transients with different decoupling capacitance achieved good accuracy. In 65nm (Figure 6), the maximum and average prediction droop errors for decoupling capacitance up to 10nF is 8.4mV (8.4%) and 3.7mV (3.5%), respectively. In 32nm (Figure 7), the maximum and average droop errors for decoupling capacitance up to 90nF are 11.6mV (14.9%) and 4.5mV (4.3%), respectively.

C. Flying and Decoupling Capacitance Optimization Based on Figure-of-Merit

Since the proposed figure-of-merit characterizes the performance of the SCVR, by varying the ratio between flying and decoupling capacitance with an area constraint, the FOM can be obtained through modeling calculation and simulations.

Validation simulations were performed in 65nm and 32nm CMOS. The flying capacitors and the decoupling capacitor are implemented with MIM capacitors in 65nm and with deep trench capacitors in 32nm. In the 65nm design, the total on-chip MIM capacitors occupy a fixed die area of 1.7mm^2. The total flying capacitance is divided by 17 for a 17-phase interleaved SC converter, and the rest of the area is occupied by the decoupling capacitance. In the 32nm process, the total area of the deep trench capacitors is 0.32mm^2. The design area overhead of the drivers and controlling circuits are relatively very small, thus omitted in this discussion. For different total output current of the SCVR, the optimal efficiencies with different flying capacitance percentages (P_{FC}) are obtained by sweeping the frequency and width of the SC converter. With the above optimal efficiency, frequency and width conditions for each flying capacitance percentage, a load step of 0.1X to 1X current in 10ns is set up correspondingly to simulate the droop voltage. The FOM for each different flying capacitance percentage is determined with Eq. (19) based on the simulation results. The modeled FOM is calculated with Eq. (20) according to the efficiency and droop voltage formulas. The comparison of simulated and calculated FOM versus flying capacitance percentage for 65nm and 32nm CMOS are shown in Figure 8 and Figure 9, respectively.

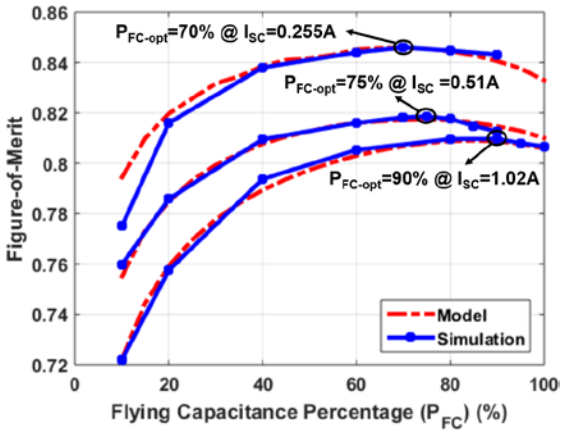

Figure 8. Simulated and calculated Figure-of-Merit for different flying capacitance percentage over total capacitance in 65nm CMOS at 0.255A, 0.51A and 1.02A SC current.

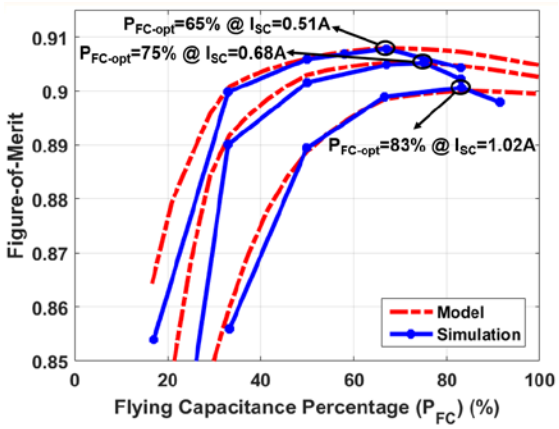

Figure 9. Simulated and calculated Figure-of-Merit for different flying capacitance percentage over total capacitance in 32nm CMOS with 0.51A, 0.68, and 1.02A SC current.

Table I shows the optimal flying capacitance percentage for different area and maximum SC output current cases, as well as the corresponding figure-of-merit, droop voltage and power efficiency for 65nm and 32nm, respectively. In 65nm CMOS, with 0.255A, 0.51A, 1.02A SC current, the simulated optimal-FOM flying capacitance percentage is 70%, 75%, 90%, respectively. In 32nm CMOS, with 0.51A, 0.68A, 1.02A SC current, the simulated optimal-FOM flying capacitance percentage is 67%, 75%, 83%, respectively. The calculated error values of the flying capacitance percentage are well below 5% compared to the simulated results.

IV. CONCLUSION

In this paper, we present an optimization methodology for flying and output decoupling capacitance of SCVRs under specific area constraints. The power efficiency and droop voltage against load transients are modeled with respect to flying capacitance and decoupling capacitance. Based on these models, we proposed a figure-of-merit that represents system-level power efficiency, capturing both efficiency and droop. The proposed FOM allowed us to optimize the flying and decoupling capacitance values for area-constrained on-chip SCVRs. The models are validated with SCVR circuit simulations in 65nm and 32nm CMOS, showing good prediction accuracy.

Table I. Optimal-FOM flying capacitance percentage and performance parameters in 65nm and 32nm CMOS from (m) modeling and (s) simulation results. Total area of flying and decoupling capacitance is 1.7mm^2 and 0.32mm^2, respectively, for both process technologies.

		65nm CMOS			32nm CMOS		
SC current (A)		***0.255***	***0.51***	***1.02***	***0.51***	***0.68***	***1.02***
Efficiency (%)	***m***	**86.0**	**84.5**	**83.0**	**94.0**	**93.7**	**93.3**
	s	**85.4**	**84.2**	**85.4**	**94.1**	**93.0**	**93.6**
Droop voltage (mV)	***m***	**40**	**48**	**83**	**34**	**45**	**69**
	s	**41**	**44**	**93**	**37**	**48**	**72**
Optimal FOM (%)	***m***	**0.846**	**0.817**	**0.809**	**0.908**	**0.905**	**0.900**
	s	**0.846**	**0.819**	**0.810**	**0.908**	**0.905**	**0.900**
Flying cap. percentage (%)	***m***	**70**	**75**	**85**	**67**	**70**	**83**
	s	**70**	**75**	**90**	**67**	**75**	**83**

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