defined by the photolithographic process. As the etching progresses, it reaches the silicon oxide layer which carries the silicon photonic device structures. The silicon oxide etch rate is also several orders of magnitude lower than the (100) silicon etch rate. In our demonstration the oxide thickness is 0.8 μm. A highly-selective hydroxide wet etch eliminates the need for precise timing. The cured front-side coating is stripped in O_2/CF_4 plasma without residue to regain original access to the SOI-CMOS front-side circuitry and optical input ports. The (111) facet sidewalls and the SiO_2 box then act as an effective stop-etch so that the handler substrate removal process can be accurately defined with photolithographic precision.

The silicon dioxide in the SOI platform is grown stress free. Limited residual intrinsic stress is expected at that interface. Once the substrate is removed from under the resonant optical device it is situated on and supported by this stress free layer. The device carrying the silicon oxide membrane is held by the remaining silicon substrate under the rest of the circuitry where the thermal isolation is not required. The devices isolated and suspended by the undercut remain mechanically supported and stable. The described process could be readily demonstrated on the wafer level in a batch process. It is tool-compatible and chemistry-compatible with conventional back-end MEMS manufacturing.

Figure 6 shows the tuning performance of a 200 μm diameter ring after selective removal of the handler substrate as described above. Upon comparing Fig. 3 and 6 it is clear the wavelength shift of the back-side pitted filter has dramatically increased per unit of applied power compared to the unetched filter. In Fig. 6 tuning with 3.9 mW of applied power is observed to produce a 2π phase shift which amounts to tuning of 4 mW/nm. We have recently demonstrated that identically designed and structured rings of different diameter would experience the same amount of resonant peak phase shift for a given applied thermal power [12]. Provided that this observed trend holds for substrate undercut rings scaled down to 10 μm in diameter for example, the amount of thermal power to shift their resonance by 2π would the same 3.9 mW as was measured for a 200 μm ring It would translate to a proportionally scaled up value in the range of 0.1-0.2mw/nm. The work on smaller rings is currently in progress. They show similar trends in improved tuning with substrate undercut but complete scaling of their tuning performance continues to be evaluated and will be described in a publication to follow.

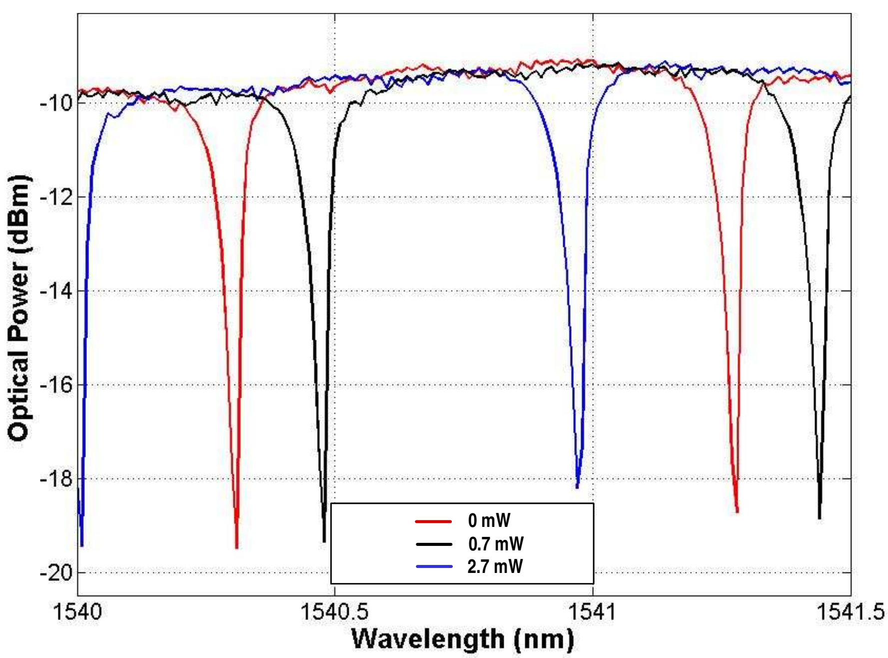

Fig. 6. Thermal tuning of the ring with a 100 μm radius.

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The response time for tuning a ring with removed undercut substrate was observed to slow down relative to the unetched devices. The time required to tune the device with locally etched substrate was observed to increase approximately three times compared to the unetched rings but still measured only several microseconds for a full 2π shift.

Furthermore, the ring's quality factor of Q = 9.6e4 remains unchanged after etching, at least to within the experimental resolution error. This implies that very little residual stress develops during the silicon handler removal process. Advantageously, due to the highly effective etch stop the internal stresses associated with non uniform and incomplete material removal can be alleviated in our fabrication approach. Otherwise these stress effects may cause strain induced inhomogeneity and local shape distortions in such a highly sensitive device with extremely high inherent Q.

The back-side etch pit can be expected to radically reduce tuning power because it disrupts heat flow spreading in the substrate of the device. This is supported by a simple analytic one-dimensional heat-flow analysis which also shows the thermal resistance of the device to decrease inversely with device diameter. A 20x reduction in the tuning has been experimentally verified and confirms expectations that thermal impedance has been drastically increased. When viewed with our simple model that scales the tuning with ring radius our result represents record performance compared with other results found in the literature [11].

5. Conclusion

We demonstrated spectral tunability of add-drop filters manufactured as ring resonators using commercial 130 nm SOI CMOS technology. Their thermal impedance has been dramatically increased by the selective removal of the SOI handler substrate under the device footprint by co-integration with bulk silicon micromachined structures. An overall ~20x increase in the tuning efficiency has been demonstrated with a post-processed 100 µm radius ring relative to its original performance with an intact substrate.

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