Ultra-efficient 10Gb/s hybrid integrated silicon photonic transmitter and receiver

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Abstract: Using low parasitic microsolder bumping, we hybrid integrated efficient photonic devices from different platforms with advanced 40 nm CMOS VLSI circuits to build ultra-low power silicon photonic transmitters and receivers for potential applications in high performance inter/intra-chip interconnects. We used a depletion racetrack ring modulator with improved electro-optic efficiency to allow stepper optical photo lithography for reduced fabrication complexity. Integrated with a low power cascode 2 V CMOS driver, the hybrid silicon photonic transmitter achieved better than 7 dB extinction ratio for 10 Gbps operation with a record low power consumption of 1.35 mW. A received power penalty of about 1 dB was measured for a BER of 10^{-12} compared to an off-the-shelf lightwave $LiNOb_3$ transmitter, which comes mostly from the non-perfect extinction ratio. Similarly, a Ge waveguide detector fabricated using 130 nm SOI CMOS process was integrated with low power VLSI circuits using hybrid bonding. The all CMOS hybrid silicon photonic receiver achieved sensitivity of −17 dBm for a BER of 10^{-12} at 10 Gbps, consuming an ultra-low power of 3.95 mW (or 395 fJ/bit in energy efficiency). The scalable hybrid integration enables continued photonic device improvements by leveraging advanced CMOS technologies with maximum flexibility, which is critical for developing ultra-low power high performance photonic interconnects for future computing systems.

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1. Introduction

Wavelength division multiplexing (WDM) silicon photonic communication links promise unprecedented aggregate bandwidth at high density for interconnects in future high performance computing systems [1–5]. Power limits at both package and system levels require the photonic links to be very efficient. Future intra/inter-chip applications expect an efficiency of approximately 300 fJ/bit at a bit rate of 20Gbps [5] which relates to extremely low-power transmitters, receivers, and WDM components.

The success of silicon photonic interconnect critically depends on high-speed energy-efficient transmitters and receivers. Monolithically integrated 4×10 Gb/s WDM silicon photonic transceivers [6] were reported previously. Owing to less advanced CMOS technology and power hungry Mach-Zehnder modulator (MZM), the transmitter and receiver consumed power of 575mW (not including the laser power) and 120 mW, respectively. Hybrid integrated 4×12.5 Gb/s WDM silicon photonics link has also been demonstrated recently [7]. It was, however, not optimized for energy efficiency either. The MZM used in this demonstration alone consumes a few tens to hundreds of mW [8,9].

Tremendous progress has also been made in efficient silicon photonic device development. On the transmit side, carrier-depletion microdisk [10] and microring [11,12] modulators have demonstrated an energy efficiency of a few 10s fJ/bit at 10 Gb/s. Optimized racetrack ring modulators with reduced voltage swing can further improve efficiency to about 10 fJ/bit [13]. On the receive side, very low parasitic Ge photodetectors have reported high responsivity and bandwidth [14–16].

In addition to efficient photonic devices, optical links also require low-power CMOS circuits to drive the modulator and to sense the photodetector current. Silicon photonics suggest monolithic integration with CMOS circuits and hence the possibility of minimized integration parasitics. However, special substrate requirements for optimized photonic device performance limit the choice of CMOS technology node; thus, CMOS platforms optimized for photonic devices are typically a few generations behind the state-of-the-art technology node. For optimized system energy efficiency, a better alternative is to decouple the photonic devices and CMOS circuits, and to take full advantage of low-power high-speed photonic devices and advanced circuit technologies simultaneously using hybrid integration.

Employing low-parasitic microsolder hybrid integration technology, we previously integrated 90 nm bulk CMOS circuits with photonic devices on a 130 nm SOI CMOS platform, and demonstrated 5 Gbps all-CMOS silicon photonic transmitters and receivers with energy efficiencies of 390 fJ/bit and 690 fJ/bit, respectively [17,18]. Later, using an improved depletion ring modulator with smaller bonding pads on the device side, we further demonstrated a silicon photonic transmitter with an energy efficiency of 320 fJ/bit at 5 Gbps [19]. In this work, to increase aggregate bandwidth and to improve energy efficiency, we integrated 40 nm bulk CMOS circuits with photonic devices from the same 130 nm SOI CMOS platform and CMOS compatible photonic foundry, using microsolder bumping with slightly reduced pad sizes. Through several circuit and photonic device improvements, the transmitters and receivers operate at 10 Gbps with more than 2X improvement in energy efficiency.

In the following sections, we discuss three key elements for building silicon photonic transmitter and receiver with new record-high energy efficiency. Section 2 introduces the energy efficient silicon photonic devices. Section 3 discusses the modulator driver and receiver circuit designs. Section 4 describes the low-parasitic hybrid integration using microsolder bumping on small bonding pads. Section 5 follows with performance results of the integrated photonic transmitter and receiver.

2. Energy efficient silicon photonic devices

Energy-efficient silicon photonic transmitters require high speed modulators with low parasitics that can achieve high extinction ratios with a low voltage swing. Similarly, energy-efficient receivers require high-speed photodetectors with low capacitance, low dark current, and high responsivity. In this section we describe ring modulators and Ge-based photo-detectors that achieve these qualities.

2.1 Racetrack ring modulator

Due to the high index contrast of silicon waveguides, ring resonator devices can confine optical fields in a very small volume, dramatically reducing device size and hence modulation power. High-speed modulation is achieved across a reverse-biased pn junction embedded in the ring waveguide. Using e-beam lithography to accurately define the micro ring structure, previous work demonstrated a ring modulator device with a quality factor of 15000 and an electro-optic (EO) efficiency of 18 pm/V in DC wavelength shift. Dynamically, the ring achieved a 6.5 dB extinction ratio with a 2 dB insertion loss under a 2 V (peak-to-peak) voltage modulation at 10 Gbps [11]. With measured junction capacitance of 50 fF for a 15 μm radius ring modulator, the integrated transmitter using a 90 nm bulk CMOS driver consumed 320 fJ/bit at 5 Gbps operation [19].

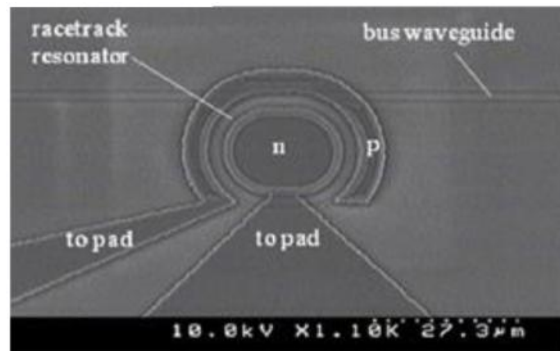

Fig. 1. Top view SEM picture of the racetrack ring modulator.

To reduce fabrication complexity and development cost, we eliminated e-beam lithography by employing racetrack resonators to enlarge the resonator-waveguide gap. All lithography steps were carried out by optical techniques using an i-line stepper with a resolution of 0.25 μm. To improve the EO efficiency, the pn junction was embedded along the whole circumference of the resonator, including the coupling region between the resonator and the bus waveguide. The modulator was fabricated using 0.25 μm SOI. The single mode ring waveguide was designed to have width of 0.5 μm and slab height of 50 nm. The pn junction has p doping concentration of 5×10^{17} cm^{-3} and an n doping concentration of 1×10^{18} cm^{-3}. Figure 1 shows a top-view scanning electron microscopy (SEM) image of a fully fabricated racetrack ring modulator. To compensate for higher junction capacitance due to increased modulation area, we designed the resonator with slightly reduced size. The racetrack ring has a bending radius of 10.4 μm and a straight coupling length of 5 μm, resulting in an effective radius of 12 μm. The critical coupling gap for the racetrack ring resonator is 0.28 μm. The fabricated racetrack ring modulator shows a quality factor of 15000 and improved EO efficiency of >25 pm/V in DC wavelength shift [13].

We characterized the high-speed behavior of the racetrack ring modulator using measured S_{11} data at 1.5 V bias. In a circuit model curve-fit to this data, shown in Fig. 2(a), C_P represents the capacitance between the electrodes (mostly due to the contact pads) through the top dielectrics and the air, C_J the capacitance of the reverse-biased diode junction, R_S the diode series resistance, C_{OX} the capacitance through the dielectric and Si layers, and R_{Si} the Si layer resistance. The junction capacitance of 49 fF is similar to that of the 15 μm radius e-beam ring modulator used for a previous 5 Gbps transmitter [19]. We further measured the racetrack ring small-signal modulation bandwidth using a microwave network analyzer and a reference detector with known frequency response. The measured result in Fig. 2(b) indicates a −3 dB bandwidth of 11.5 GHz, large enough for 10 Gbps data transmission.

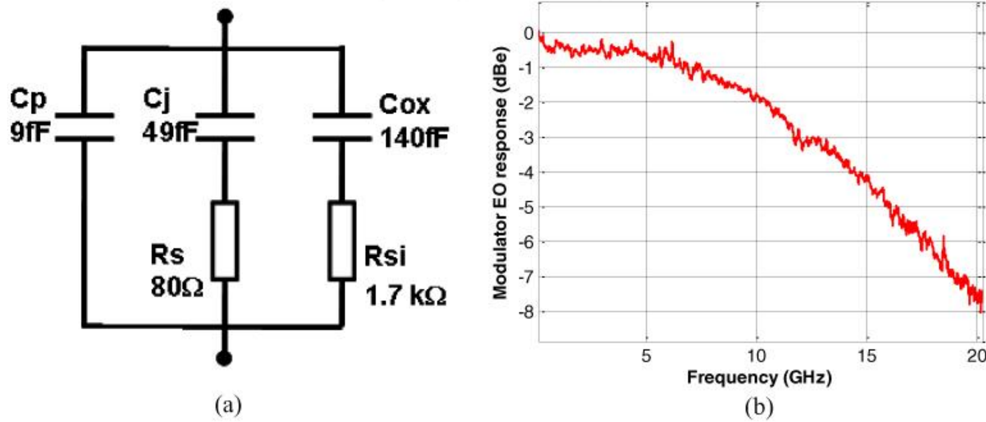

Fig. 2. Small signal high speed characteristics of the racetrack ring modulator. (a) Circuit model extracted by measured S_{11} data; (b) Measured frequency response for the 12 μm racetrack ring modulator.

2.2 Ge waveguide photodetector

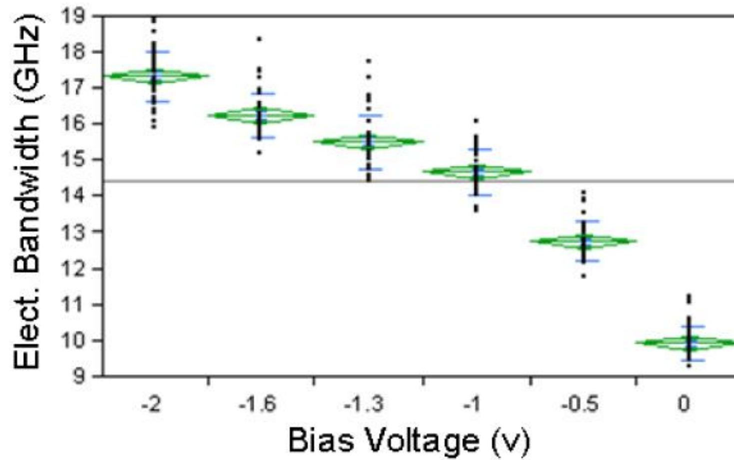

Fig. 3. The measured electrical bandwidth of the CMOS Ge waveguide PIN photodetector for different bias voltages.

Ge-PIN waveguide photodiodes were fabricated in Freescale's HIP7_SOI 130 nm CMOS technology with Luxtera's Ge-enabled optoelectronic process. It's an evanescent coupled Ge detector. 0.3 µm wide single mode waveguide was first tapered to wider multi-mode waveguide with width of 1.5 µm, and length of 15 µm. 200-300 nm of Ge was then grown onto the multimode section with a growth window width of 1.4 µm. Single-step low-temperature (350 °C) Ge growth was used to minimize the thermal impact on the transistors. With a dark current under 3 µA at 0.5 V reverse bias, diode capacitance of only 10 fF, and bandwidth exceeding 10 GHz [14,17] they had been quite suitable for our previous 5 Gbps receivers. In this work, we used the same Ge waveguide photodetector design with fabrication process refinements to improve performance slightly. Multi-wafer characterization across different lots indicates that at 0.5 V reverse bias, the Ge waveguide photodetector achieves a −3 dB bandwidth exceeding 12 GHz (as shown in Fig. 3), and improved responsivity of 0.8 A/W (as shown in Fig. 4).

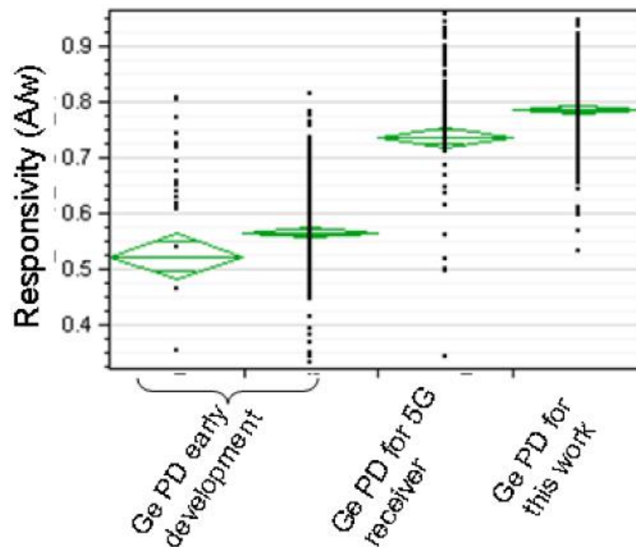

Fig. 4. The measured responsivity of the CMOS Ge waveguide PIN photodetector.

3 Low power CMOS circuits

3.1 2 V modulator driver

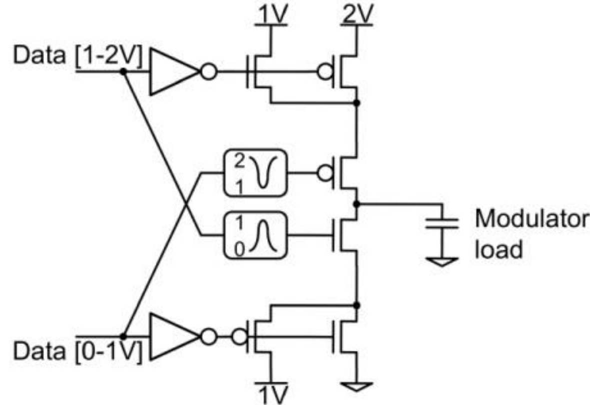

Fig. 5. Cascoded modulator driver circuit.

The circuit model in Fig. 2(a) shows that the depletion racetrack ring modulator appears largely as an RC load to the CMOS driver. Because a voltage swing of 2V is required to achieve an adequate extinction ratio, we use cascoded drivers [20] to drive 10 Gbps data on the racetrack rings as shown in Fig. 5. Pulse generators on the cascode devices activate them within a timing window designed to minimize Vgs and Vgd overstress during output transitions [21].

For testing purposes, the modulator drivers can take data from either an on-chip PRBS generator or from an off-chip pin. Because the data source is common to all modulator circuits on our test chip, the datapath can selectively invert and/or delay that data stream at each individual modulator experiment. This allows data bits at different experiments to be independent and thus enables more realistic device array testing. In order to simplify the on-chip digital circuitry, data is moved across the chip in two parallel “single-data-rate” 5 Gbps streams and converted at the modulator driver into one “double-data-rate” 10 Gbps stream.

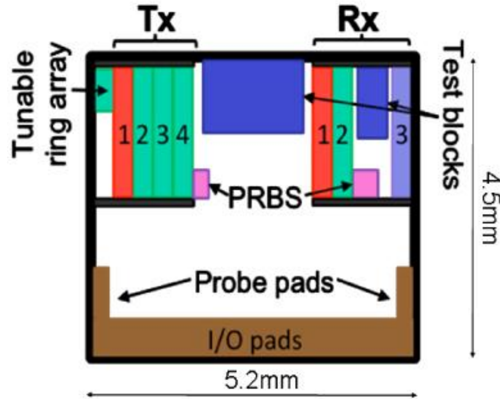

Fig. 6. VLSI chip floorplan showing multiple modulator drivers and receiver circuits integrated on the same chip.

The VLSI test chip was fabricated in TSMC’s 40 nm bulk CMOS technology. Its floorplan, in Fig. 6, shows four transmit (TX) columns of sixteen modulator drivers each, with each driver occupying 120 μm^2. Prior to hybrid integration with a photonics chip, the drivers were tested with direct probing to the bonding pads using single-point 26 GHz active probes;

the probe load of 50 fF matched the bonded racetrack ring modulator load. A typical eye diagram measured from the probes, for PRBS data (2^{15}-1) at 10 Gbps, is shown in Fig. 7.

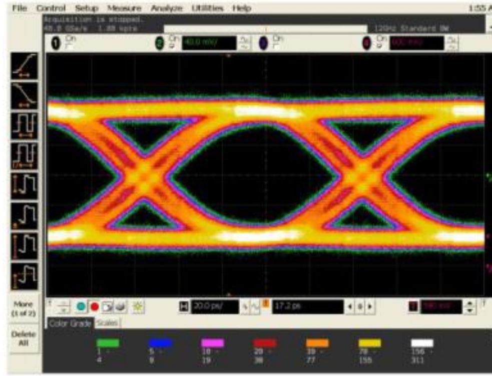

Fig. 7. Probed modulator driver data "eye," prior to hybrid integration, showing 2 V modulation at 10 Gbps.

3.2 Low power receiver

The low-power receiver, as the block diagram shown in Fig. 8, is based on a transimpedance amplifier that converts the input photo-diode current into a small-swing voltage signal. A strobed sense-amplifier [22] restores this signal to full CMOS voltage levels in a manner analogous to limiting amplifiers. The sense-amplifier (SA) is more efficient than limiting amplifiers, but its operation imposes three requirements on the receiver circuit. First, because the SA needs a clock input to tell it when to amplify, the receiver includes a clock-phase recovery circuit, based on a delay-locked loop (DLL). Second, because the SA needs to compare the input against a threshold reference voltage to determine whether the data was a "0" or a "1," the receiver includes a facility to adjust the input current so that the resulting SA input signal swings symmetrically around a preset voltage threshold. Finally, because sense-amplifiers suffer from intrinsic mismatch and comparison inaccuracy, the receiver implements circuits to compensate for this offset.

Setting the DLL for appropriate clocking of the SA, setting the input level to center the SA input around the voltage threshold, and setting two distinct offset compensation circuits requires a total of four digital-to-analog converters (DACs) in the receiver. Digital finite state machines drive and set these four DACs during periodic recalibration of the optical link.

The TIA is based on a three-inverter chain [23] and is designed for a gain of 4 kΩ at a bandwidth of 7 GHz, assuming an input capacitive load of 60 fF including both photodiode and hybrid bonding pads. This enables operation at −15 dBm input sensitivity with a worst-case extinction ratio of 3 dB and a photodiode responsivity of 0.7 A/W, and targeting a signal-to-noise ratio (SNR) sufficient for a bit error rate (BER) of 10^{-12}.

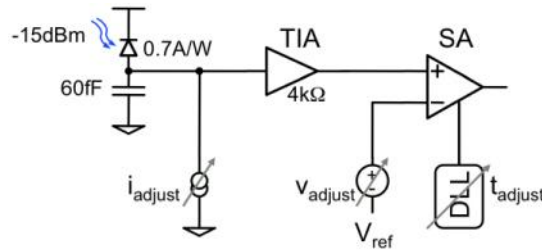

Fig. 8. Block diagram of the receiver, showing an adjustable shunt current, an adjustable offset voltage (one of two shown here), and an adjustable clock strobe. Not depicted are the finite state machines that control these adjustments.

For testing purposes, the test chip instantiated several special receivers whose inputs were connected not to bond pads but rather to special current sources designed to deliver a PRBS current sequence at an 20 μA average amplitude; this corresponds to a −15 dBm input with a responsivity of 0.7 A/W and an extinction ratio of 3 dB. These special receiver blocks allowed testing and characterization of the receivers prior to hybrid integration. All receivers were able to drive their CMOS-level output signals into an on-chip PRBS checker for verifying the correctness of the received data; the checker was designed to be compatible with not only the on-chip PRBS generator but also the standard PRBS sequences used in common laboratory testing equipment.

The receiver was fabricated as part of the test chip shown in Fig. 6. Not counting the hybrid bonding pads, each receiver consumed under 8000 μm^2. As shown in the floorplan, the chip instantiated three columns of 16, 16, and 10 receivers. These were positioned in order to mate with different photodetector chips.

4 Hybrid integration with ultra-low parasitics

Low-parasitic, hybrid integration is a key component for enabling optimal energy efficient links based on aggressive silicon photonic devices and very low power, high speed circuits. The implicit value of a hybrid approach is that photonics and electronics can be independently optimized on different technology nodes and thereby avoid compromises and tradeoffs that otherwise might develop during co-integration. A conceptual view of a silicon photonic chip and VLSI chip hybrid is shown in Fig. 9. The hybrid integration step involves micro-fabrication of micro bumps consisting of low parasitic conductive connections above top level metal on the VLSI chip, and an accurate flip-chip bonding attachment following procedures originally reported in [24]. In the current application we deploy thermo compression bonding as opposed to a reflow of eutectic solder typically used in the chip attach industry. This same procedure has previously demonstrated integration of dense arrays of optical modulators [25] and VCSELs [26] to CMOS drivers with very high yield (> three nines). Additionally, our hybrid integration module is highly compatible with our macrochip packaging platform [27] that facilitates building out dense multichip arrays interconnected with advanced chip to chip signaling [28].

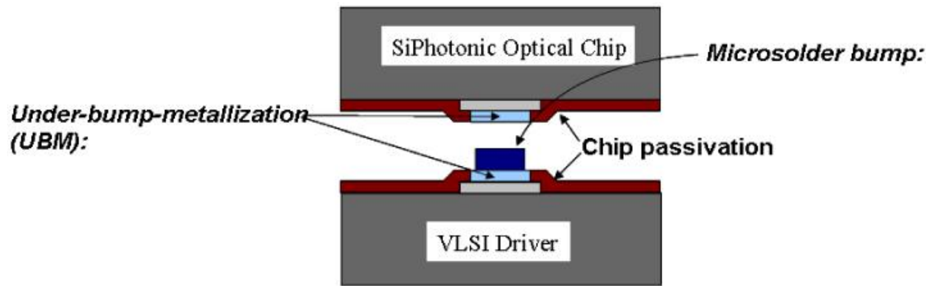

Fig. 9. Illustration of flip-chip hybrid-bonding technique using microsolder bumps.

Here we report very low energy photonic links by scaling our hybrid integration platform into the 40 nm CMOS node where the new ELK stackup poses serious mechanical and metallurgical impediments for any solder attachment approach. These new challenges could disrupt the historical scaling of our hybrid integration platform that had previously kept pace [29] with next generation Si linewidths and thereby limit reduction in bump parasitics. As such, it would represent a technology barrier that blocks continued scaling and reduction in energy per bit for links based on a hybrid approach.

Our solution begins with an under-bump-metallization (UBM) layer that was first deposited onto the bonding pads of both VLSI and photonic chips using electroless plating of Ni/Au at low temperature (<100°C) [30]. The UBM layer serves as a stable and low resistance

contact to the chip's I/O pads, a strong adhesion interface between the die bondpad and bump materials, and barrier prevents diffusion of the bump materials into the chip. It is the foundation on which the bump and therefore the hybrid bond stand. Following UBM deposition, microsolder bump are fabricated by a sequence of lithography, metal deposition, and liftoff [30]. Figure 10 shows a SEM image of an array of microsolder bumps.

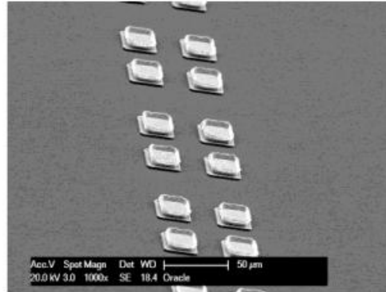

Fig. 10. SEM picture of an array of microsolder bumps on the 40 nm node VLSI driver chip. Circuitry and metal routing below the passivation layer is not visible. The flat pad just above the featureless grey background (passivation layer) is the top level Al pad that has been ELESS plated with UBM and above that is the "cup like" microsolder bump.

Chip-to-chip attachment in the hybrid integration technology is achieved via a thermo-compression bonding process under several pounds of loading pressure at modest temperature. The microsolder bump has a crown several micrometers tall which provide vertical compliance to absorb the effects of local topological variations, chip bow, and any tool-tilt during flip-chip bonding. In addition, the crown is compressed and embedded into the UBM pad of the opposing chip during the thermo-compression, resulting in extremely small resistance. We have measured < 1.0 ohm resistance to each bonding site. Since the parasitic capacitance due to bonding depends on the pad size, we used slightly reduced pad size of 25µm to have estimated capacitance of less than 20fF. Even with the new 40 nm ELK process for the VLSI chip the average resistance of our bumps is measured to be 0.3 ohms that further represents nearly a 2x lower parasitic that we reported for previous generation technology [29].

Figure 11(a) and Fig. 11(b) show images of the hybrid integrated transmitter and receiver chip assembly, respectively. Photonic chips are assembled in diving board configurations such that at least one edge of the photonic chip is sufficiently exposed to provide access for surface-normal or edge-coupling optical I/Os. The ring modulator chip has size of 6 mm × 7.5 mm, while the photo detector chip size is 3.5 mm × 7 mm.

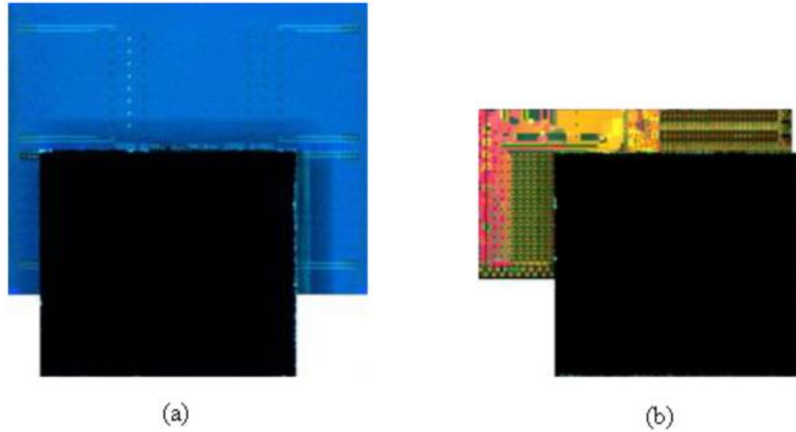

Fig. 11. Photonic devices hybrid integrated with VLSI chip. (a) Hybrid integrated transmitter chip assembly with the silicon photonic modulator chip facing up; (b) Hybrid integrated receiver chip assembly with the Ge waveguide PIN detector array chip facing up.

5 Integrated transmitter/receiver testing

The hybrid bonded chip assemblies were die attached and wire bonded to a printed circuit board (PCB) for performance characterization. To mimic an inter-chip communications application, we used the on-chip PRBS generator as the data source to drive the racetrack ring modulator, and the on-chip PRBS checker to measure the bit-error-rate for the data received by the receiver, while external clock sources were used to clock both transmitter and receiver.

5.1 Integrated transmitter

Figure 12 shows the test PCB (holding the integrated silicon photonic transmitter) mounted on a test station for performance characterization. The inset blow-up picture shows the VLSI/modulator hybrid chip assembly die attached and wire bonded onto the test PCB in a diving board configuration. Optical input and output to and from the chip is done through edge coupling using lensed fiber probes.

Continuous wave (CW) light from a tunable laser source is coupled to the hybrid bonded modulator chip through a polarization controller, followed by a lensed PM fiber mounted on a 6-axis alignment stage. Electrical data at 10 Gbps from the on-chip PRBS generator, clocked externally, drives the modulator. The modulated optical signal is then coupled to another lensed fiber on a separate 6-axis alignment stage. To compensate for the relatively large coupling loss from the lensed fiber to the sub-micron silicon waveguide, an EDFA was used to boost the modulated optical signal before it is fed to the optical receiver. The resulting O/E converted signal is then sent to either a scope or an error detector for BER measurements.

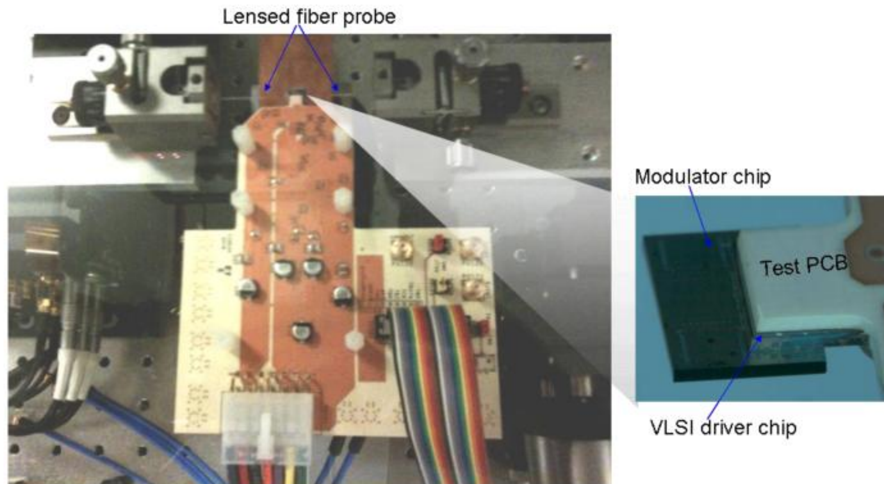

Fig. 12. Test setup for hybrid silicon photonic transmitter characterization with the inset blow-up picture showing the modulator/VLSI driver hybrid chip assembly die attached and wire bonded on a test PCB.

Figure 13(a) shows a measured optical "eye" diagram for 10 Gbps data transmission from the hybrid integrated silicon photonic transmitter using a racetrack ring modulator. The "ON" state loss was measured to be 3 dB. The eye is open with >7 dB extinction ratio. To better evaluate the quality of the silicon photonic transmitter, we compared it with an off-the-shelf $LiNOb_3$ lightwave transmitter using the same off-the-shelf lightwave receiver. The $LiNOb_3$ lightwave transmitter has an extinction ratio of 12 dB, and an "ON" state insertion loss of 6 dB. The BER at different received power levels for 2^{31}-1 PRBS data transmission at 10 Gbps were measured for both the lightwave transmitter and the silicon photonic transmitter. The results plotted in Fig. 13(b) show a received power penalty of about 1dB at a BER of 10^{-12}. This received power penalty is mainly from the relatively low extinction ratio (7 dB) of the silicon photonic transmitter.

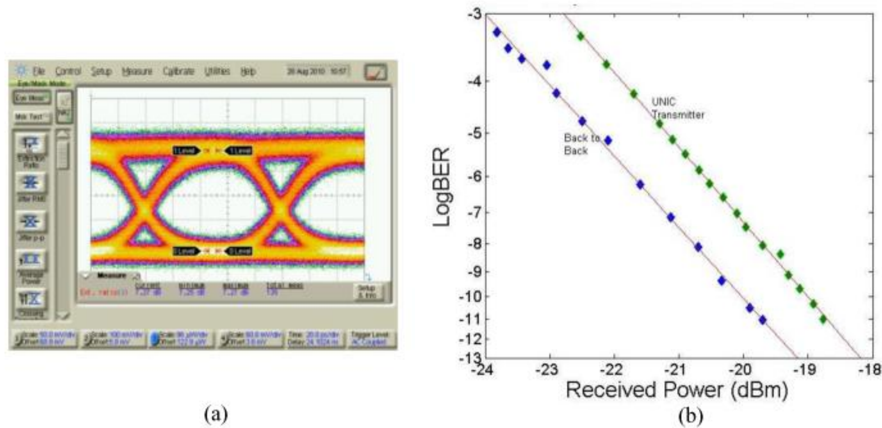

Fig. 13. Performance of the hybrid integrated silicon photonic transmitter at 10 Gbps. (a) Measured optical "eye" diagram at 10 Gbps with >7 dB extinction ratio; (b) Received power penalty measurement showing ~1 dB power penalty at a BER of 10^{-12} compared with an off-the-shelf $LiNOb_3$ lightwave transmitter with 12 dB extinction ratio.

The power consumption of the hybrid integrated transmitter was obtained by measuring the voltage and current of all the supplies of the driver circuits during 10 Gbps PRBS data

transmission. The transmitter consumes a record low power of 1.35mW, or an energy-efficiency of 135 fJ/bit, excluding the laser power.

5.2 Integrated receiver test results

The hybrid integrated silicon photonic receiver was tested on a station with a lensed fiber probe for optical input. Grating couplers were used to couple the fiber to on-chip waveguides. Figure 14 shows the test setup, with the inset blow-up pictures showing the VLSI/PD hybrid chip assembly die attached and wire bonded onto the test PCB in a diving board configuration, and also the lensed fiber probe aligned with grating couplers for surface normal optical coupling.

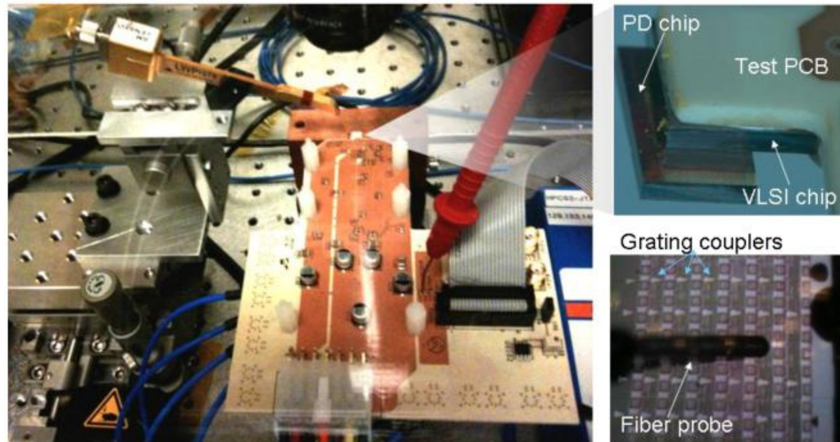

Fig. 14. Test setup for hybrid silicon photonic receiver characterization with the inset blow-up pictures showing the PD/VLSI circuits hybrid chip assembly die attached and wire bonded on a test PCB, and a lensed fiber aligned with grating coupler for optical input.

CW light from a tunable laser source was modulated by a lightwave transmitter (with 12 dB extinction ratio) using PRBS data from a pattern generator. The modulated optical signal was coupled to the hybrid bonded receiver chip through a polarization controller, and a lensed fiber mounted on a 6-axis alignment stage. The receiver converts the optical signal to electrical data, which is then sent to an on-chip PRBS checker for error detection. To characterize the receiver performance, we measured the BER at different input optical power levels. The on-chip PRBS checker and receiver are both clocked externally.

The receiver is designed with the capability of bringing out the photo-detector current to a monitoring port. The input optical power is calculated using the measured photo current and the nominal PD responsivity of 0.8 A/W (obtained from measurements across many wafer lots).

Using built-in test facilities, each receiver's sense-amplifier thresholds can be externally set, in 4 mV steps. This allows testing the receiver at different voltage references. Using similar facilities, the sense-amplifier's clock timing can be externally set by adjusting the DLL's output phase. This allows testing the receiver at different timing references. By scanning both voltage and time settings, and measuring the BER at each (voltage,time) tuple, we can measure a virtual "eye" opening at the receiver.

The top left plot in Fig. 15 shows the BER "eye" measurement result for an average photocurrent of 24 μA from the photodiode. The x-axis is the sampling timing (in ps), and the y-axis is the sense-amp decision threshold (in volts). The green area represents (voltage,time) tuples for which the BER was under 10^{-12}. To obtain the receiver sensitivity, we further reduce the input optical power level until the 10^{-12} BER "eye" is just open, as shown in the right plot of Fig. 15. We confirm the BER by setting the sampling point to the middle of the

scanned BER "eye", and measuring the BER for a long time. The receiver achieved 25 minutes of error free operation with only 16 μA of average photo current for 10 Gbps, 2^{31}-1 PRBS data, confirming a true BER of better than 10^{-12}. Given PD responsivity of 0.8 A/W, we obtain receiver sensitivity of better than −17 dBm for BER of 10^{-12} at 10 Gbps.

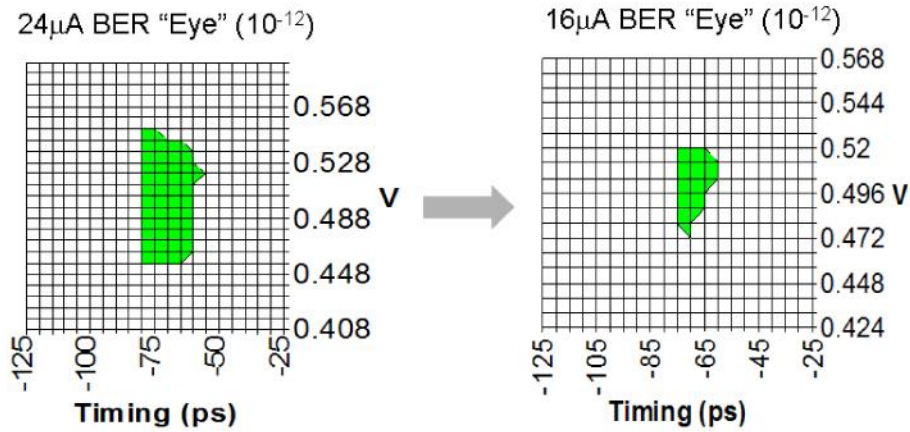

Fig. 15. Performance of the hybrid integrated silicon photonic receiver at 10 Gbps showing the measured BER "eye" at average input photo current of 24 μA (left plot) and 16 μA (right plot). Under 16 μA average photo current, the receiver was error-free for 25 minutes for PRBS 2^{31}-1 data.

The power consumption of the hybrid integrated silicon photonic receiver using Ge waveguide detectors is obtained by measuring the voltage and current of all the supplies of the receiver circuits during 10 Gbps operation. The TIA, DLL and DACs together consume 2.53 mA from a 1.25 V supply regulated to 0.95 V. The sense-amps and digital logic together take around 0.8 mA from a 1 V supply, resulting in a total of 3.95 mW. Thus the hybrid integrated receiver achieves a record high energy efficiency of 395 fJ/bit.

6 Conclusions

Low parasitic hybrid integration using microsolder bumping technology enables the decoupling of photonic device development and VLSI circuit design. This gives designers the freedom to use photonic devices from different platforms, and to take advantage of CMOS technology scaling to aggressively improve the integrated transmitter and receiver performance in both data rate and energy efficiency.

For transmitter development, we used a depletion racetrack ring modulator with greater than 25 pm/V EO efficiency from a CMOS compatible photonic foundry. We hybrid integrated this device to a cascoded 2 V modulator driver in an advanced 40 nm CMOS process using 25 μm bonding pads, and demonstrated 10 Gbps performance with better than 7 dB extinction ratio at a power consumption of 1.35 mW, or 135 pJ/bit in energy efficiency. This represents an improvement of about 2.4x over our previous demonstration using an e-beam ring modulator and a 90 nm CMOS driver [19]. Off-chip laser source were used for this demonstration whose power was not included in the transmitter power reported above. To support a complete WDM intra/inter-chip link, a few mW of optical power will be needed. Currently available WDM laser sources typically have low wall-plug-efficiency on the order of a few percent. Obviously the laser power will dominate the total link power consumption when considered at system level. More efficient WDM laser source needs to be developed for intra/inter-chip photonic interconnects. In addition, although multiple channels were integrated on the same chip with drivers bonded, we were only able to light up one channel at a time because of the high accuracy alignment required for edge coupled sub-micron waveguides. Simultaneous operation of multiple channels in parallel can be achieved by

integrating either mode converters for edge coupling [31,32], or grating couplers [33,34] for surface normal coupling to arrayed fibers.

Similarly, we hybrid integrated an SOI CMOS Ge waveguide PIN photodetector with 12 GHz bandwidth and 0.8 A/W responsivity with a low power receiver circuit in a 45 nm CMOS process to build an energy-efficient silicon photonic receiver. The resulting all-CMOS receiver achieved −17 dBm sensitivity for a BER of 10^{-12} at 10 Gbps. Careful sizing with accurate characterization of SNR resulted in a power consumption of 3.95 mW, or 395 fJ/bit. This represents about 1.8x improvement in energy efficiency compared to our previous demonstration using a similar detector and 90 nm CMOS receiver circuits [18].

Further improvements in energy efficiency can be achieved by scaling the footprint of microsolder bumps and the bonding pads to about 10 μm, resulting in a much smaller bonding capacitance on the order of a few fF. In conjunction with continued improvements in CMOS technology and silicon photonic devices, we expect to develop even more efficient transmitters and receivers leading to complete high speed silicon photonic WDM links with high bandwidth density for future inter/intra-chip applications. Although only single channel result was reported in this paper, the technologies developed are all scalable. The microsolder bumping technology demonstrated capability of integrating chips with thousands of bumps [25,26] at very fine pitch. In fact, it was used to integrate the optical devices and CMOS circuits designed and fabricated in array form in this work. With the compact silicon photonic devices, dense hybrid integration, and parallel optical IOs using optical proximity couplers [34,35], we expect to scale the hybrid integrated silicon photonic links with large bandwidth density beyond 1TB/mm^2.

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