An Asynchronous High-Throughput Control Circuit For Proximity Communication

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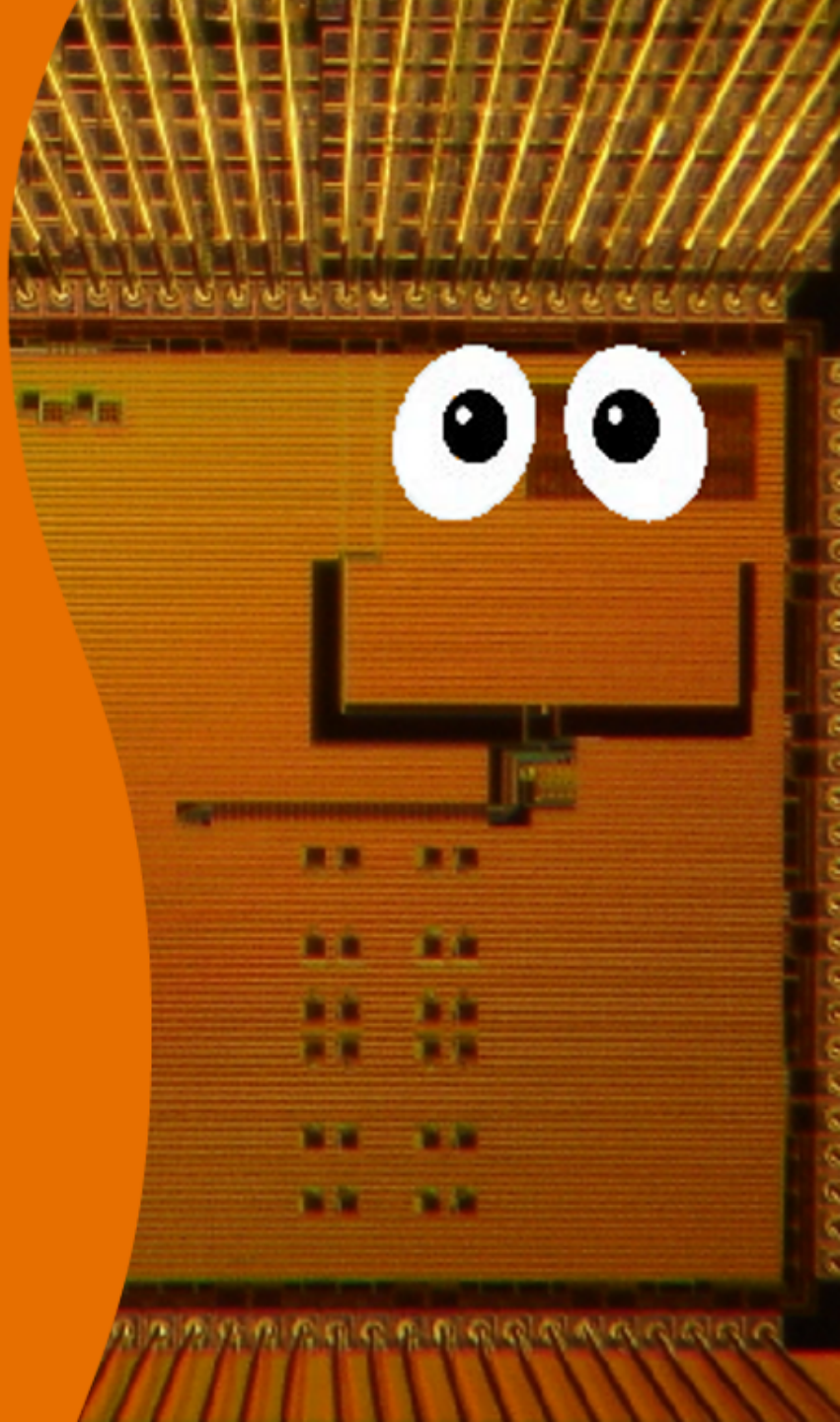
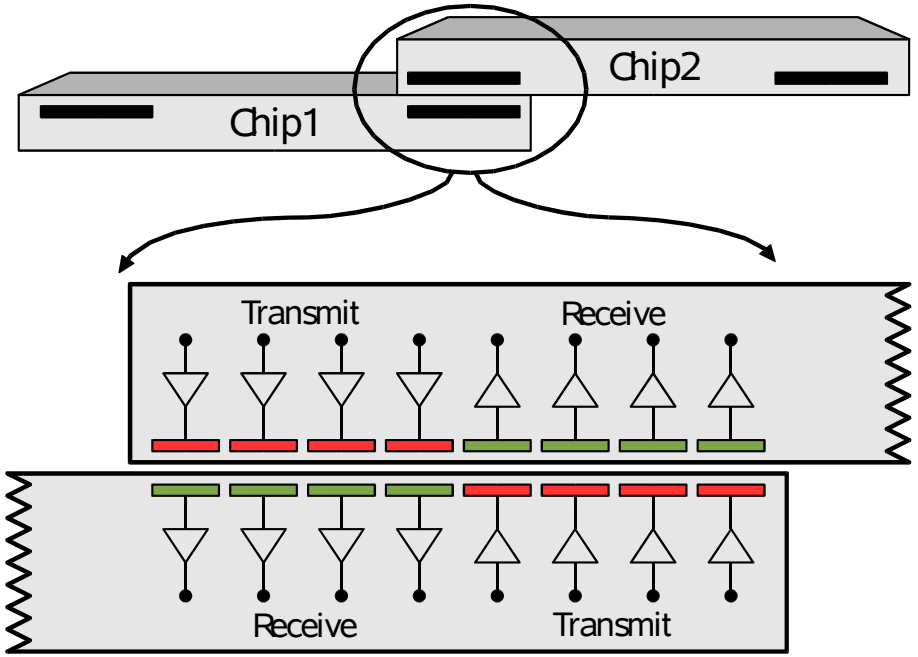


To Discuss:

- Proximity communication
- The timing challenge
- Our asynchronous solution
- Our test chip
- Future work
- Questions

Proximity Communication



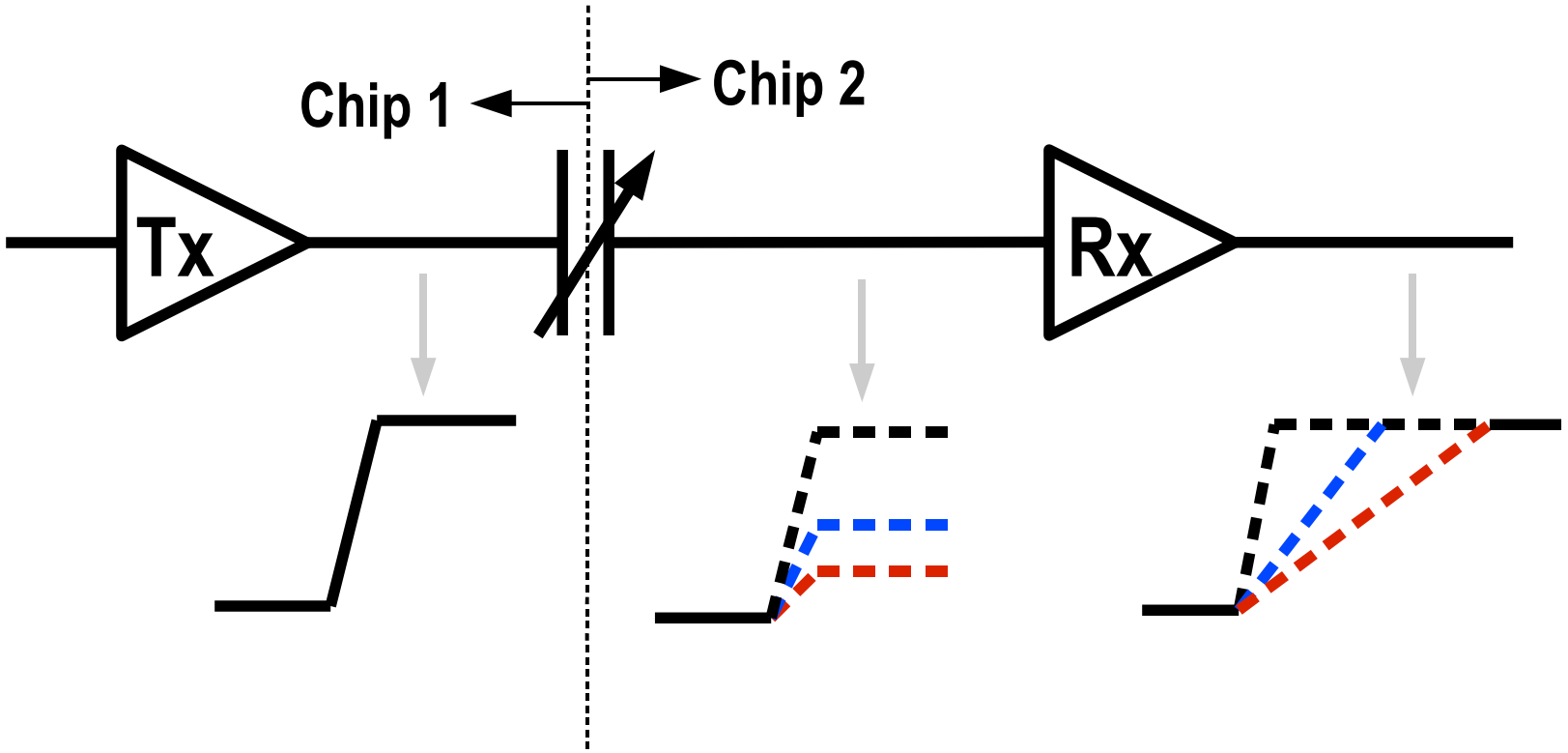
- Interconnect technology
  - > Low power, high density
- Developed by our group at Sun Labs

The Timing Challenge

- Traditional interconnect challenges
  - Timing
  - Flow control
  - Power consumption

- New challenges
  - Amplifying small signals
  - Chip alignment
  - Variable performance

Chip Alignment



- Typical channel delay ~ 5 gate delays
  - > Varies with chip alignment

The Timing Challenge

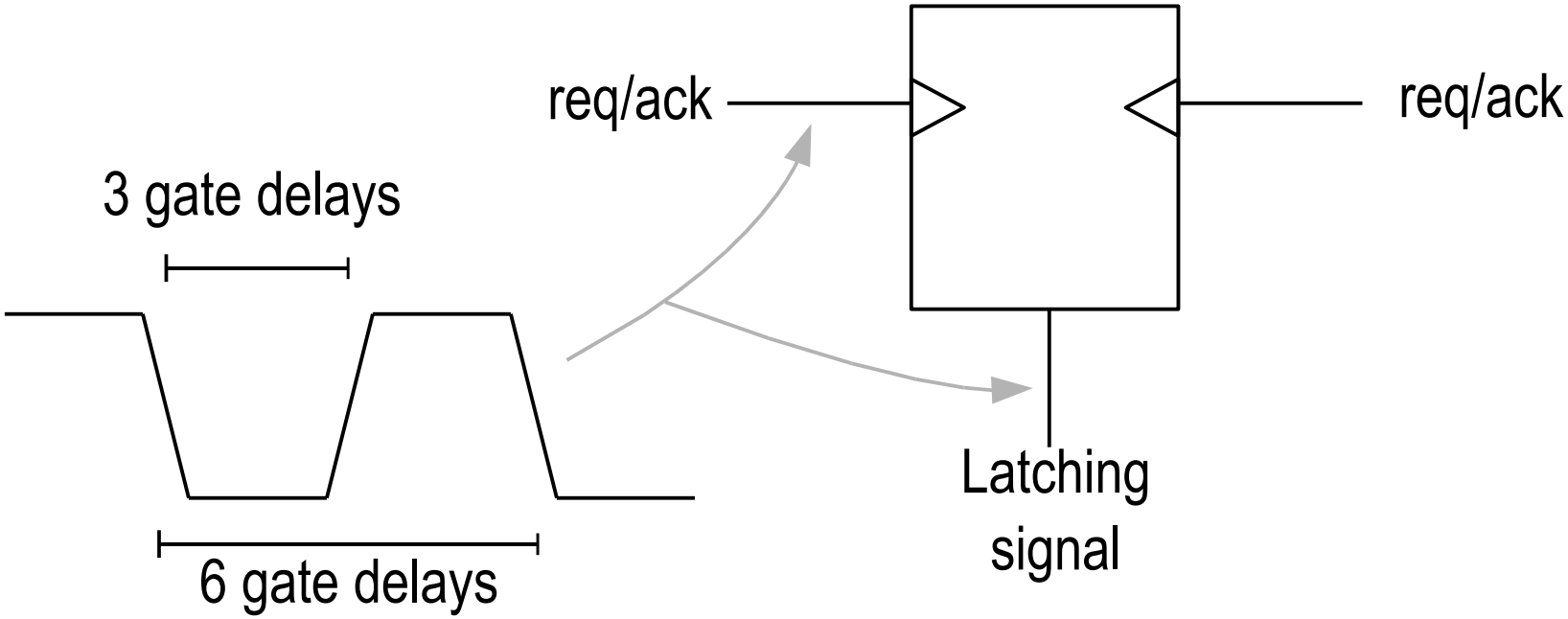
Our Solution

- Asynchronous timing protocol

- Performance goal:
  - One data item every GasP cycle (6 gate delays)
  - Around 3 Giga tokens per second (Gtps) in 180 nm

Our Asynchronous Solution

- Uses GasP circuit family
  - > Cycle time around 6 gate delays
  - > One shared signal wire for request and acknowledge
  - > Pulse signaling



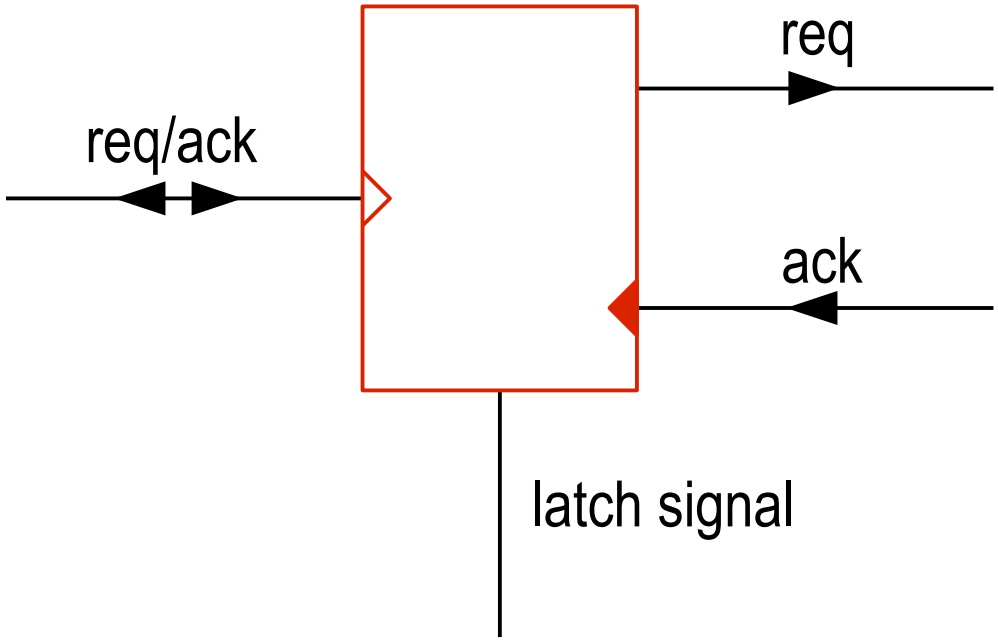
GasP: Challenges

- Proximity channel is unidirectional
  - GasP uses bidirectional state wires
- Chip-to-chip signal transitions are expensive
  - Pulse signaling requires two transitions per token
- Handshake requires two channel crossings plus overhead
  - Exceeds 6 gate delay GasP cycle time

GasP: Challenges

Bidirectional GasP State Wires

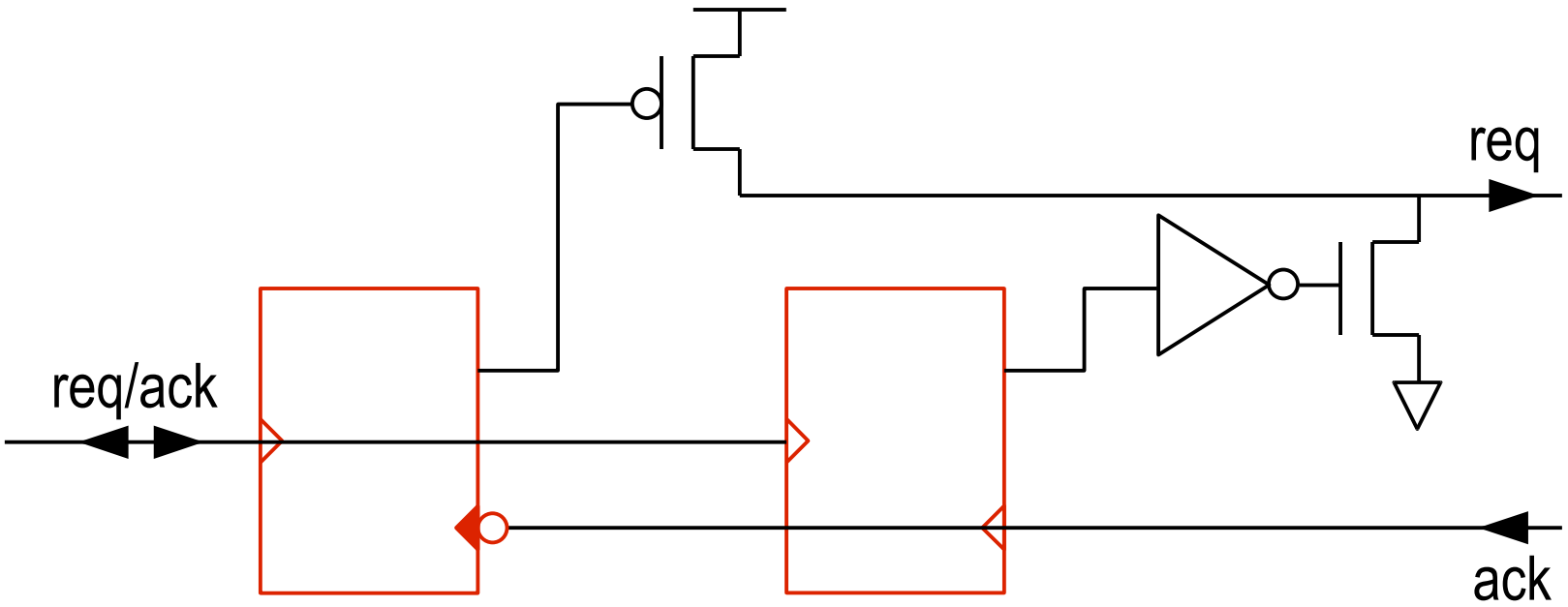
- Use separate request and acknowledge wires at proximity channel



GasP: Challenges

Pulse Signaling

- Convert pulse to transition signaling

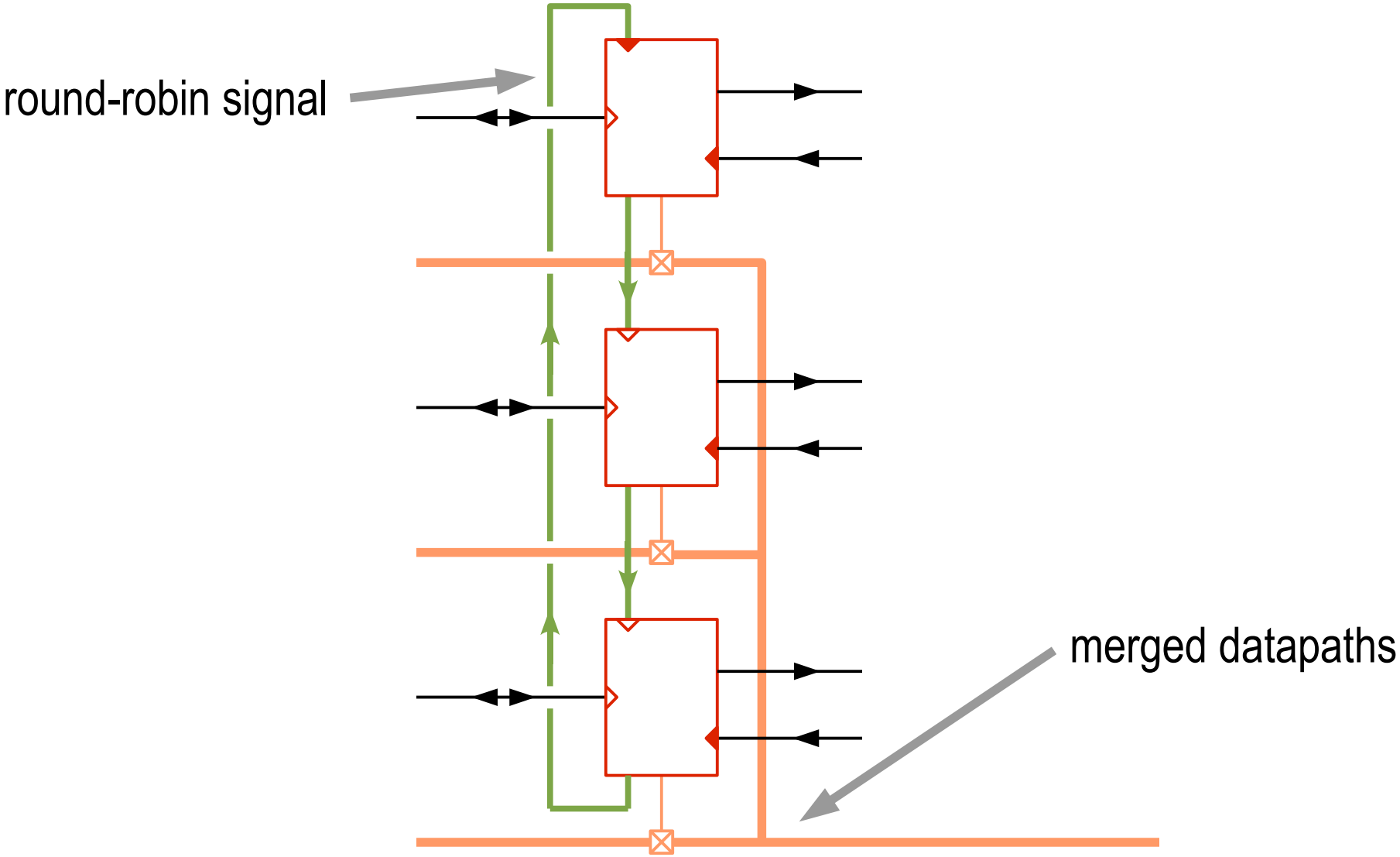


GasP: Challenges

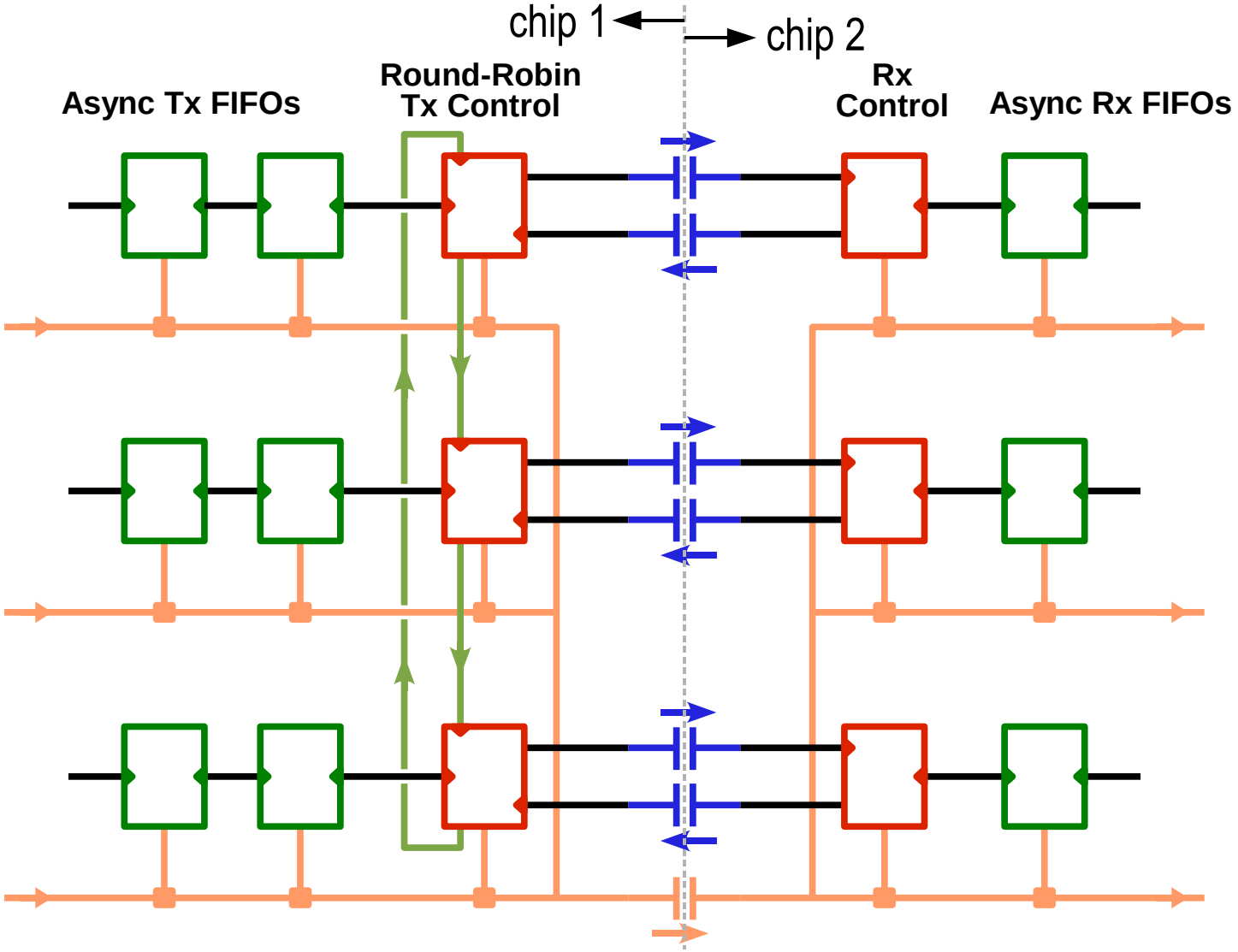
Control Latency

- Multiple concurrent control paths
- Single datapath channel
- Three-way round-robin scheme
  - > Sequences control
  - > Determines total throughput

Round-robin Control Paths



Our Asynchronous Solution

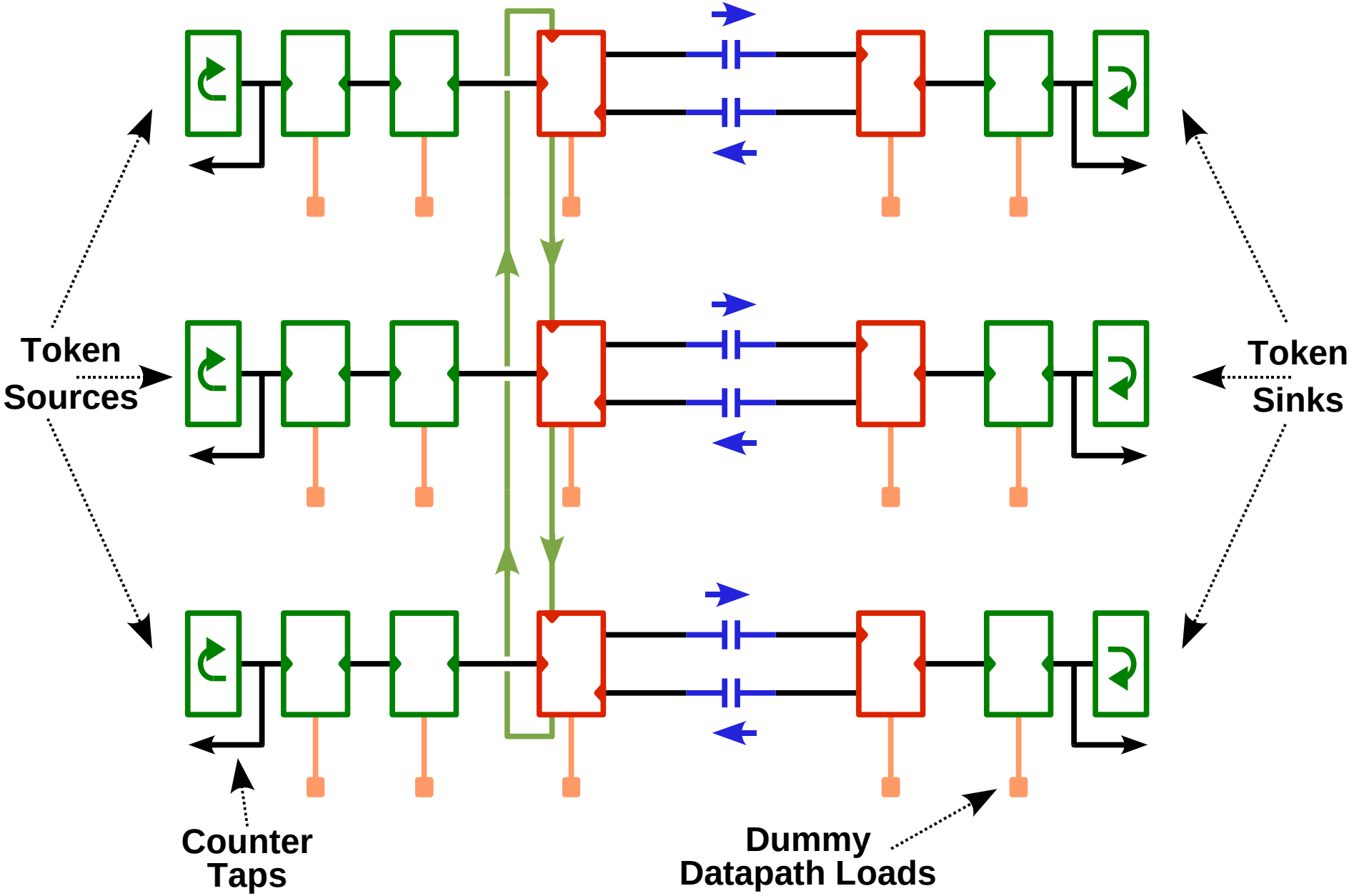


Our Test Chip

- Fabricated to test asynchronous control scheme
- Funded by DARPA as part of Sun's HPCS initiative
- Taped out November 2004 in the 1.8V,180 nm MOSIS TSMC process
- Demonstrated timing over a capacitively coupled interface for the first time

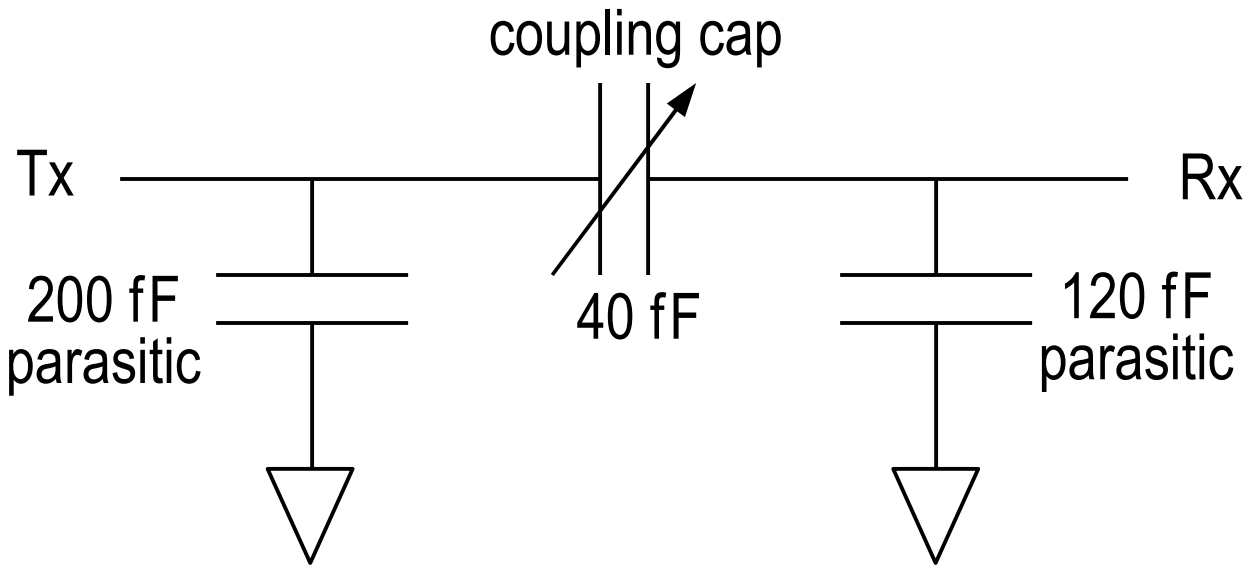
Test Chip Features

- On-chip varactors to emulate proximity interface
  - Only one chip needed for testing
- Dummy loads to represent 72-bit datapath
- Asynchronous GasP sources and sinks for tokens
- Counters at the sources, sinks, and on the round-robin path


Token
Sources
Token
Sinks
Counter
Taps
Dummy
Datapath Loads

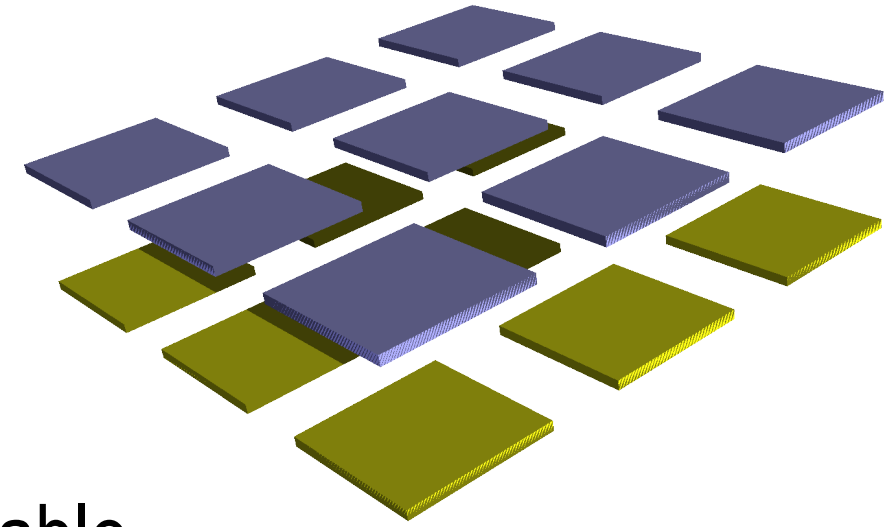
The Proximity Channel

- Emulates an inter-chip channel on a single chip
  - > 120 µm x 120 µm pad size
  - > Nominally 2.5 µm chip separation
- Varactors emulate chip misalignment



On-chip Varactors

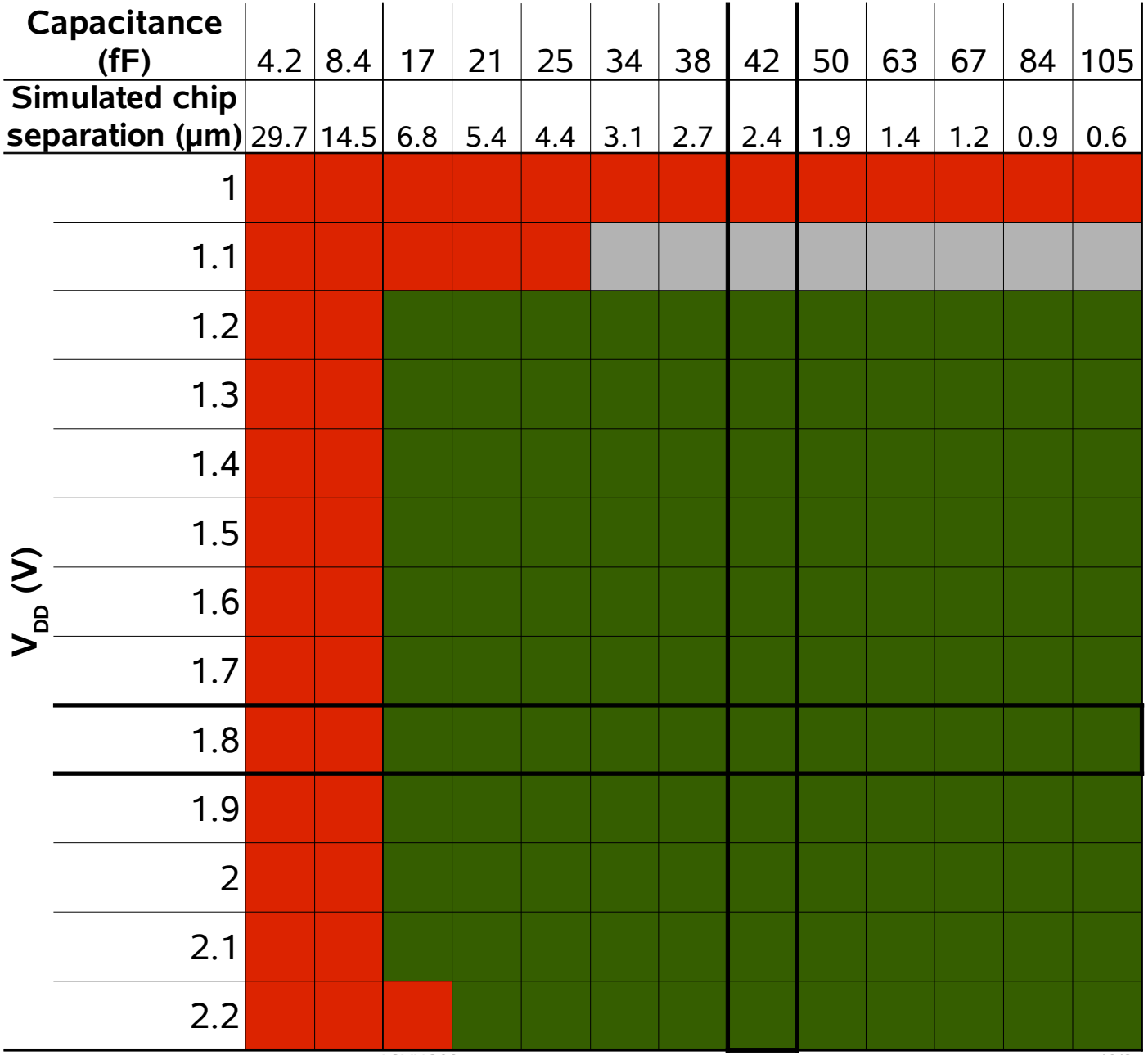
- 25 plates
- Emulates coupling caps from 4 – 105 fF
  - > Chip separation of 0 – 30 μm



- Independently programmable

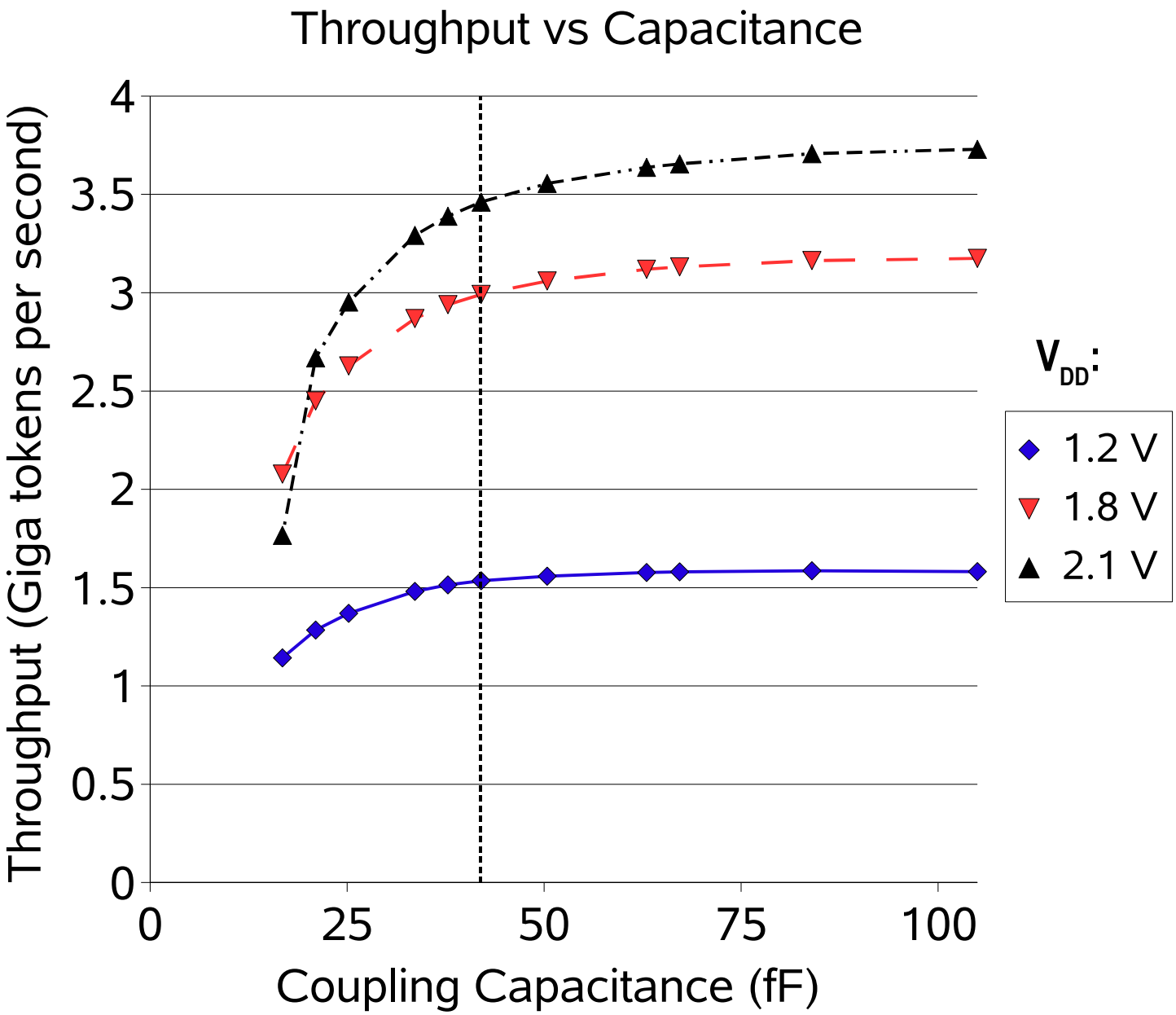
Testing

Schmoo Plot



Testing

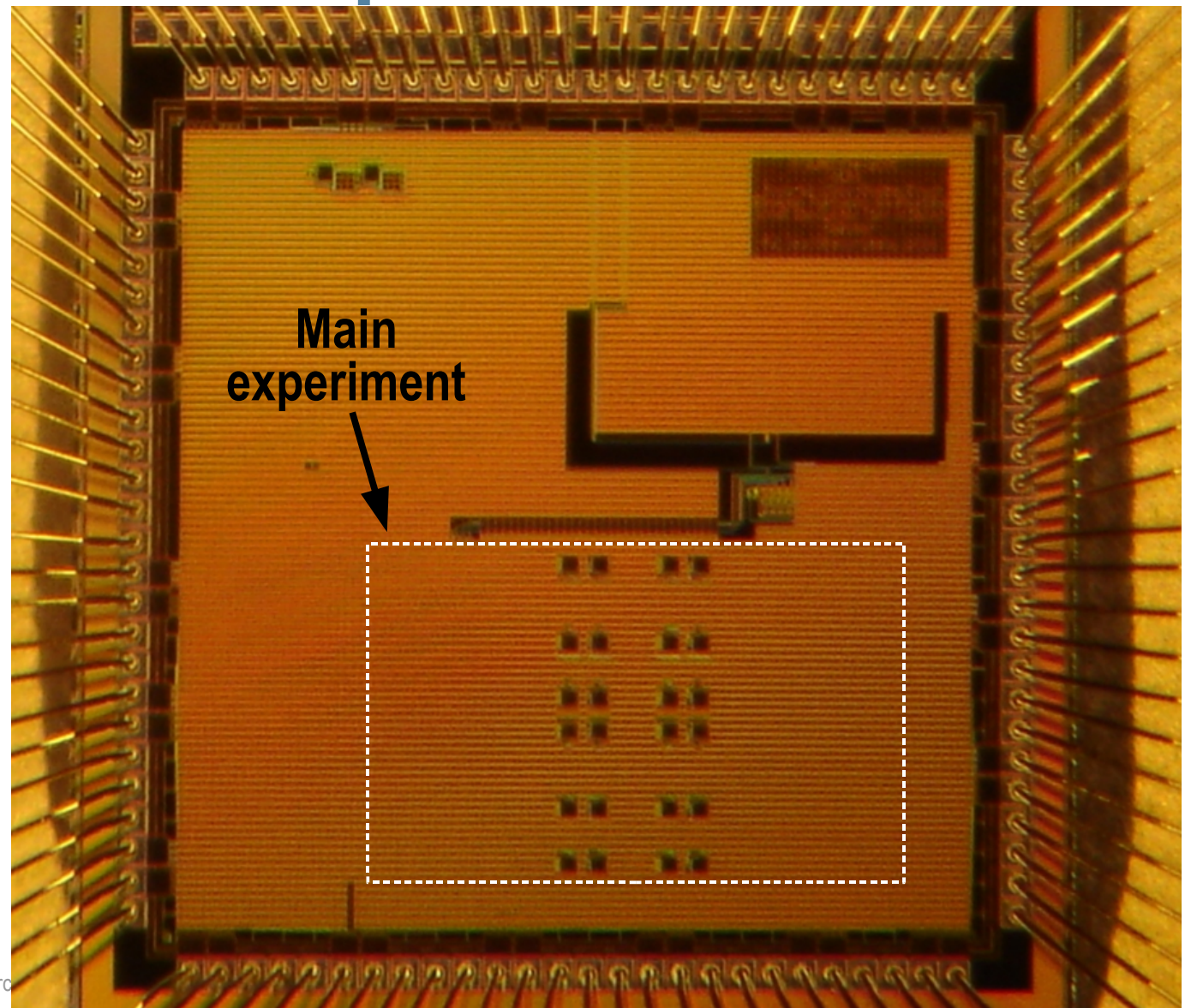
Performance



Testing Results

- Exemplified robustness of asynchronous design
  - Performs well (> 1 Gbps) from 1.2 to 2.1V and 17 fF up
- Met our performance goal
  - 3 Gtps at 42 fF
- Revealed that our counters are too slow

Our Test Chip



Future Work

- Attach a real datapath
- Increase performance and decrease power consumption
  - Differential signaling
  - Different asynchronous circuit family

Thanks!

- DARPA for funding us (Contract #NBCH3039002)
- Co-authors: Jo Ebergen, Alex Chow, Bill Coates, David Hopkins
- The rest of the VLSI Research Group and our contractors

Questions?

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