Lessons from Asynchronous Design

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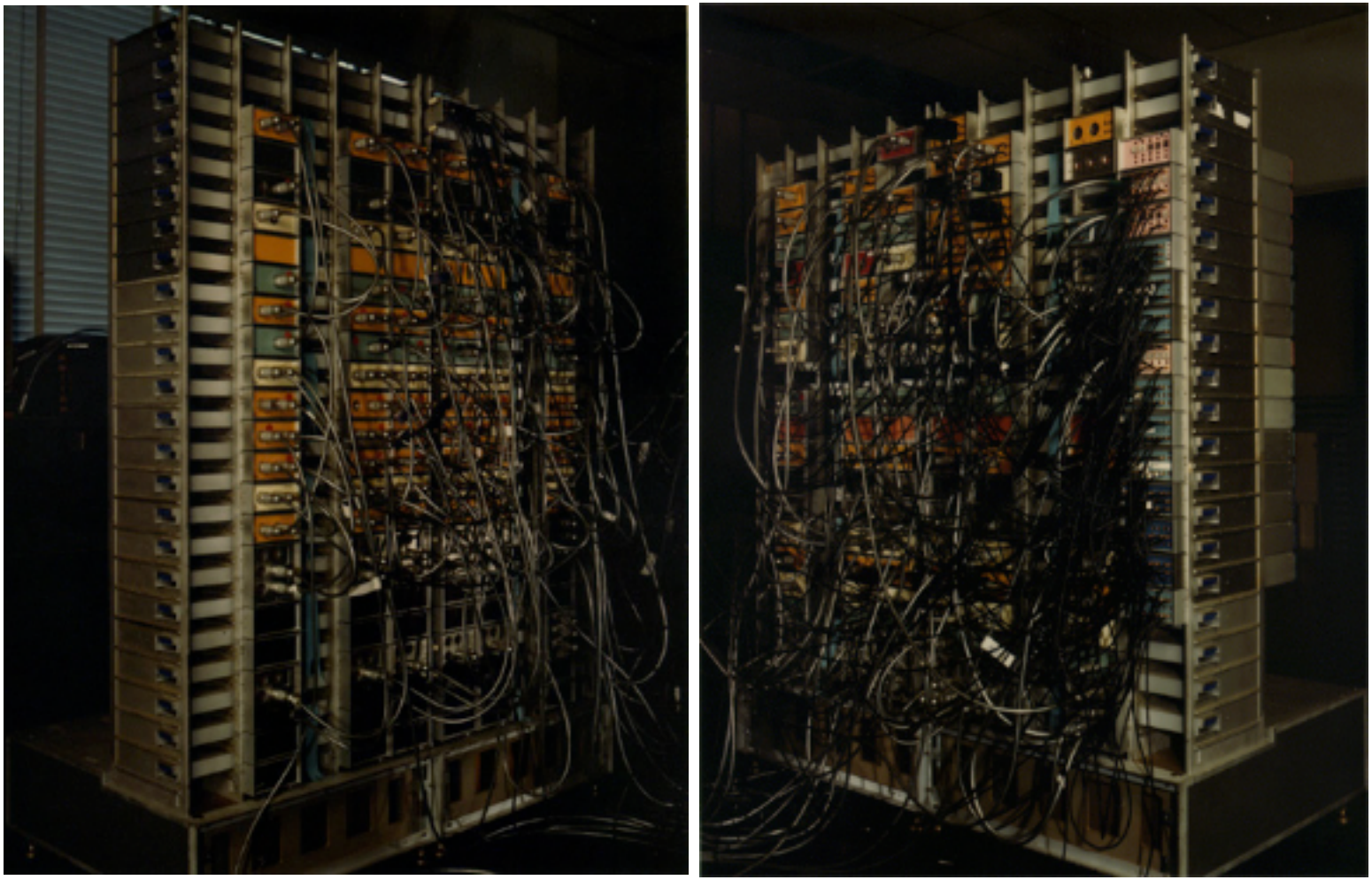
A Historical Perspective

- Clocked versus clockless
- The first computers: clocked or clockless?
- ENIAC('46), ACE('46), EDVAC ('46)
- Enablers: Switching Theory and FSMs
- A BIG problem: making reliable computers
- Clock is convenient in design and verification
- Terminology: non-synchronous, asynchronous, speed-independent, self-timed, delay-insensitive

Why No Clock?

- Speed
  - Average vs worst-case behavior
- Avoid timing problems related to clock
  - Synchronization problem
  - Clock distribution, skew, jitter
- Modularity
  - Reusability
  - Composability
  - Incremental improvement

An Example: Macromodules
('66–'74)



More: Why No Clock?

- Low power
  - Portable electronics
  - Budget constraint: total energy, not cycle time
- Architectural freedom
  - Concurrency at any grain size
- Robustness
  - Correct operation over a large range of process, voltage, and temperature variations
- Reduced electromagnetic radiation
  - Spread spectrum versus isolated peaks

Successes

- A strong Async Community (ASYNC conference)
  - # papers on async or GALS has increased since ‘94
- Interest from industry
  - SUN, Philips, Intel, IBM
  - Startups: Handshake Solutions, Fulcrum Microsystems, Theseus Logic, Mobius, Silistix, ...
  - Some products have reached the market (Philips pager, Philips smartcard, UltraSPARCIIIi, ...)

“Learning Experiences”

- Clocked design still rules
- Many startups have come and gone
  - A natural process...
- DARPA CLASS program
- My learning experiences at SUN
  - UltraSPARCIIIi
  - ROCK FGU
- Technology and Courage

More “Learning Experiences”

- CAD Tools
  - Synthesizer for clockless circuits
  - Performance analysis (timing and power analysis)
  - Functional verification
  - Test
- Education
  - Text books, courses, tutorials, ...

The Future

- Ubiquitous Systems on Chip
  - "To the tera chip and beyond.."
- Many IP blocks, each possibly with their own clock domain, and a network
  - Will the network be clocked or clockless?
- Power will become a severe constraint
  - Clock gating will help, but clock gating is essentially "async design" under a different name
  - Dynamic frequency and voltage scaling?

The Future, more

- Reliability will be essential
  - Variability will increase dramatically. How to cope with variable delays?
  - Components will fail over time. Create reliability through redundancy?
- Efficient Programming will become harder
  - How to use all these trillions of transistors efficiently?

Resources

- Async Design Group at Sun Labs
  - research.sun.com/vlsi/
- Async Logic Home Page
  - www.cs.man.ac.edu/async/
- Ivan Sutherland's Turing Award lecture 1989
- "Computers Without Clocks" Scientific American, Aug. 2002
- ASYNC conference series