ONEday03

Circuits Without a Clock: What Makes Them Tick?

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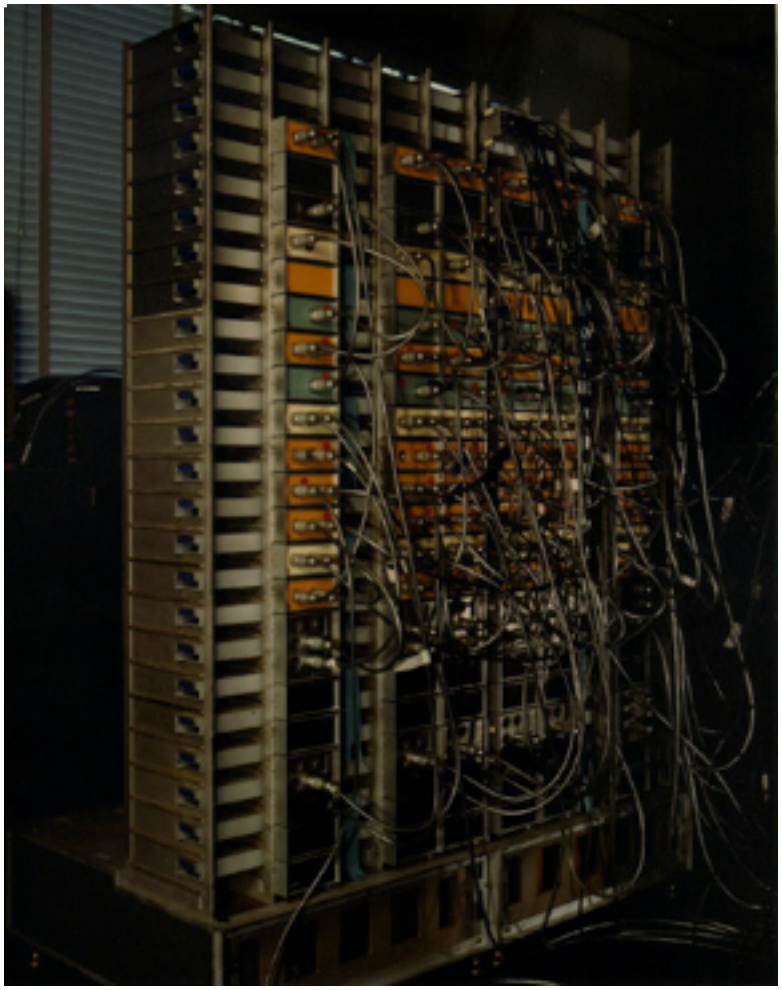
A Historical Perspective

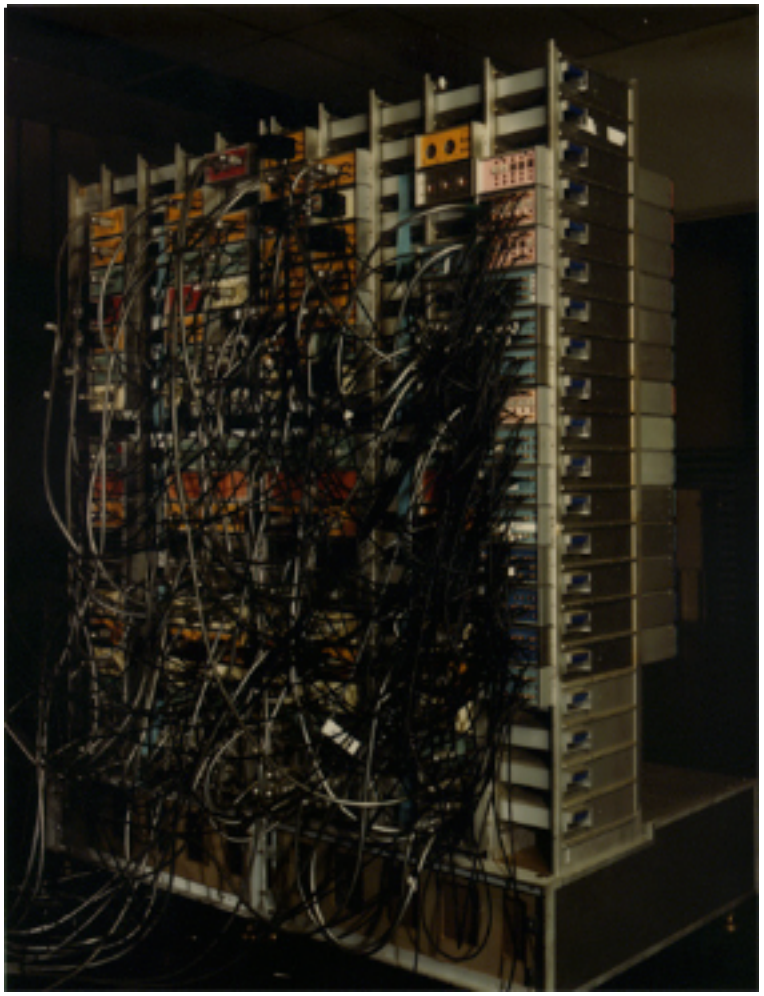
- Clocked versus clockless
- The first computers: clocked or clockless?
- ENIAC(’46), ACE(’46), EDVAC (’46)
- Enablers: Switching Theory and FSMs
- A BIG problem: making reliable computers
- Terminology: non-synchronous, asynchronous, speed-independent, self-timed, delay-insensitive

Why No Clock?

- Speed
  - Average vs worst-case behavior
- Avoid timing problems related to clock
  - Synchronization problem
  - Clock distribution, skew, jitter
- Modularity
  - Reusability
  - Composability
  - Incremental improvement

An Example: Macromodules ('66-'74)



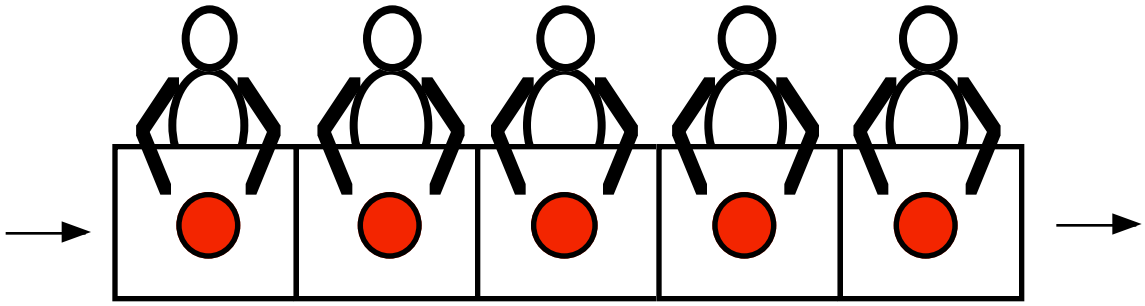


More: Why No Clock?

- Low power
  - Portable electronics
  - Budget constraint: total energy, not cycle time
- Architectural freedom
  - Concurrency at any grain size
- Robustness
  - Correct operation over a large range of process, voltage, and temperature variations
- Reduced electromagnetic radiation
  - Spread spectrum versus clock peaks

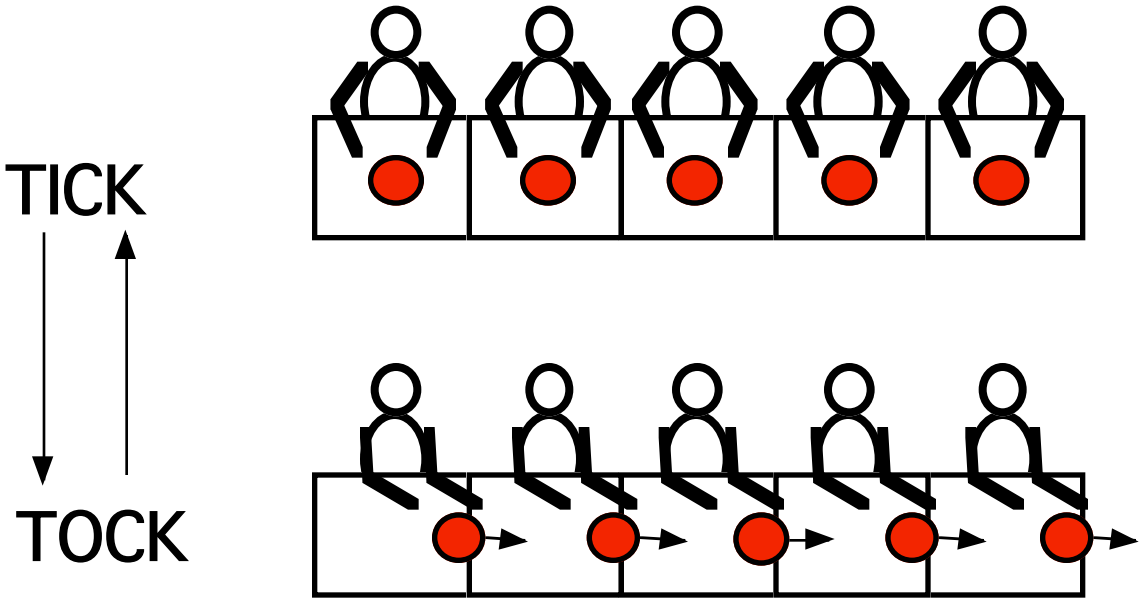
A Live Demo

- Pipelined “food” processing
- Clocked and clockless version



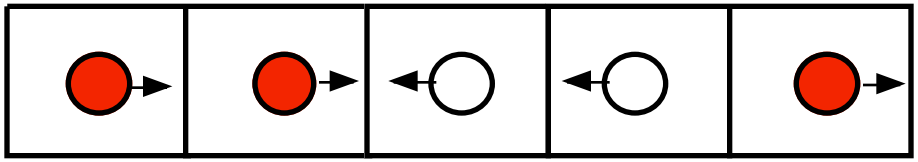
Clocked “Food Processing”

- TICK: process food
- TOCK: move plate to successor



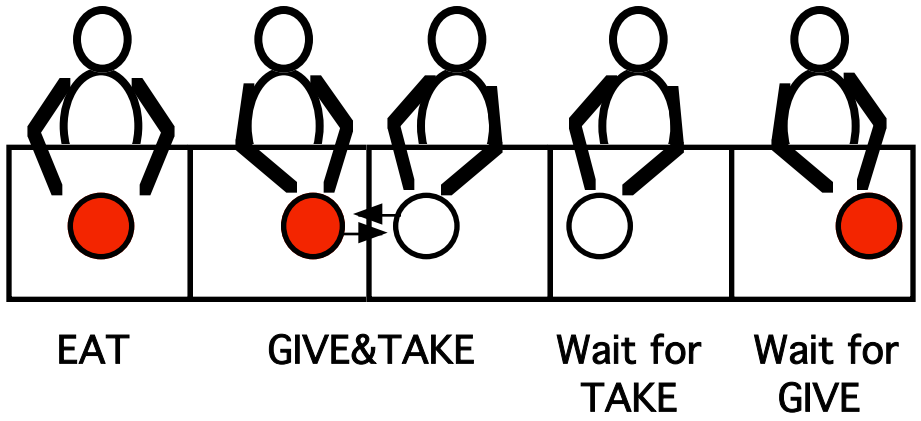
Clockless “Food Processing”

- Two types of plates
- Red plate = stage with data item
- White plate = empty stage
- Red plates move forward
- White plates move backward



Repeat These Rules

- **TAKE: If predecessor has RED plate, take RED plate (and give WHITE plate)**
- **EAT: Process food**
- **GIVE: If successor has WHITE plate, give RED plate (and give WHITE plate)**



To Notice

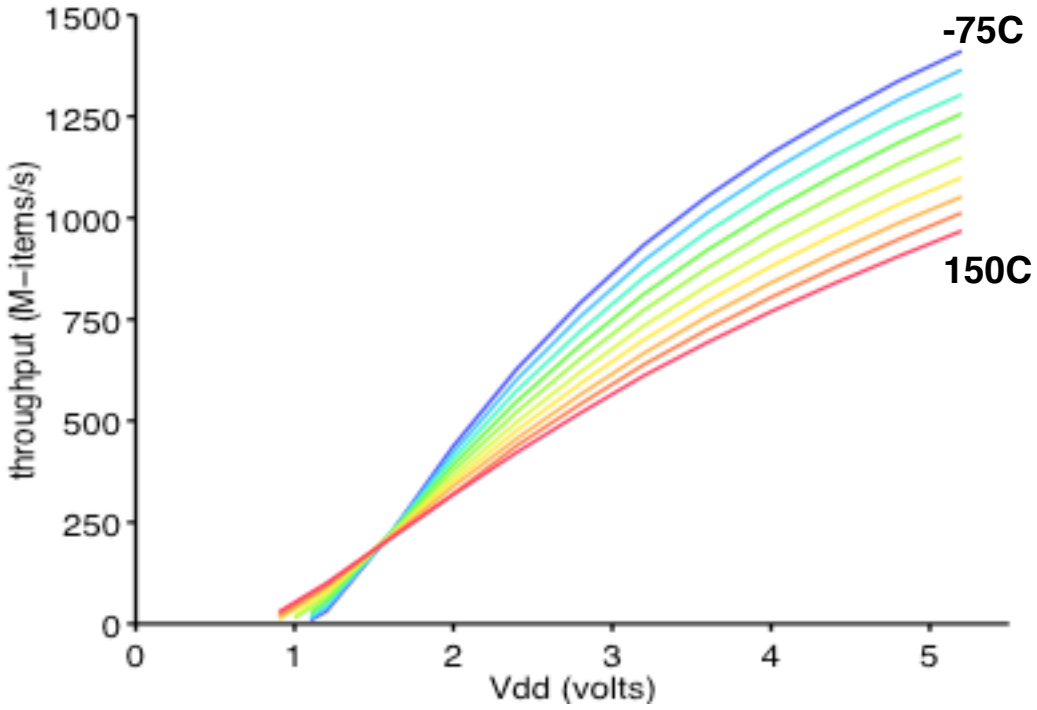
- Clock period must be longer for slowest person for worst food
- Clockless pipeline adjusts speed to person and food being processed
- Clocked pipeline spends energy with every tick or tock, even when there is no food on plate
- Clockless pipeline spends energy only when food must be processed

More To Notice

- Clocked pipeline must have the same frequency as the source and sink, to prevent overflow or underflow
- Clockless pipeline has automatic overflow and underflow protection

Results From Actual Chips

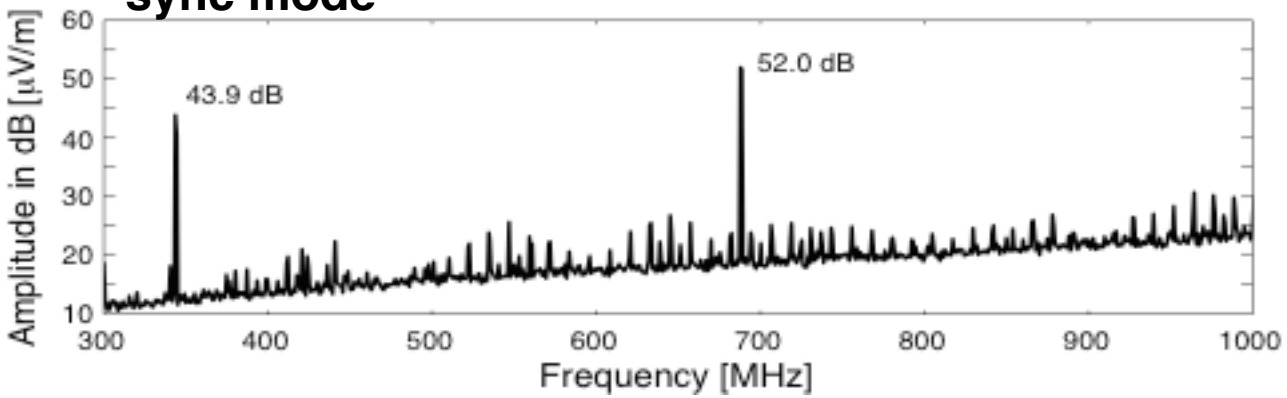
- Throughput vs supply voltage and temperature



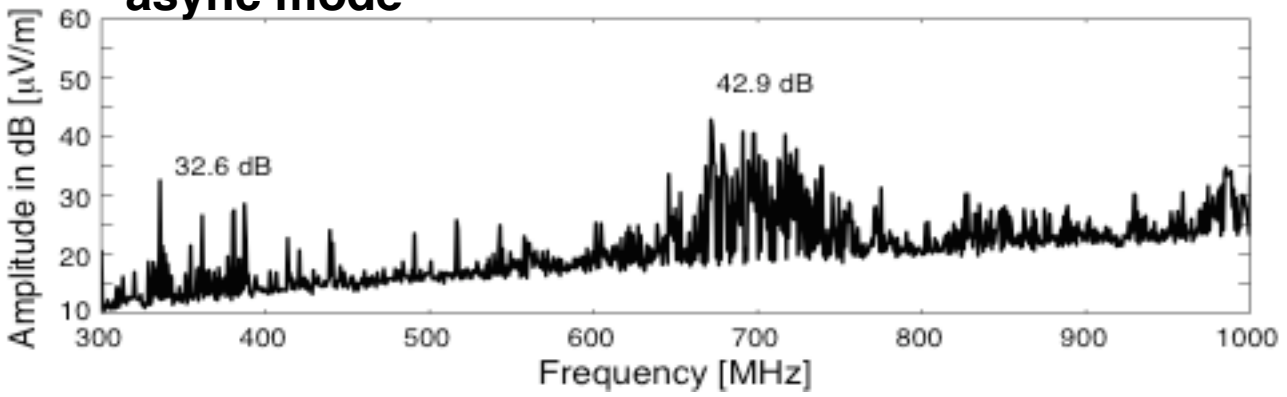
Reduced Radiation

- **Frequency spectrum of the same chip operating in sync and async mode**

sync mode

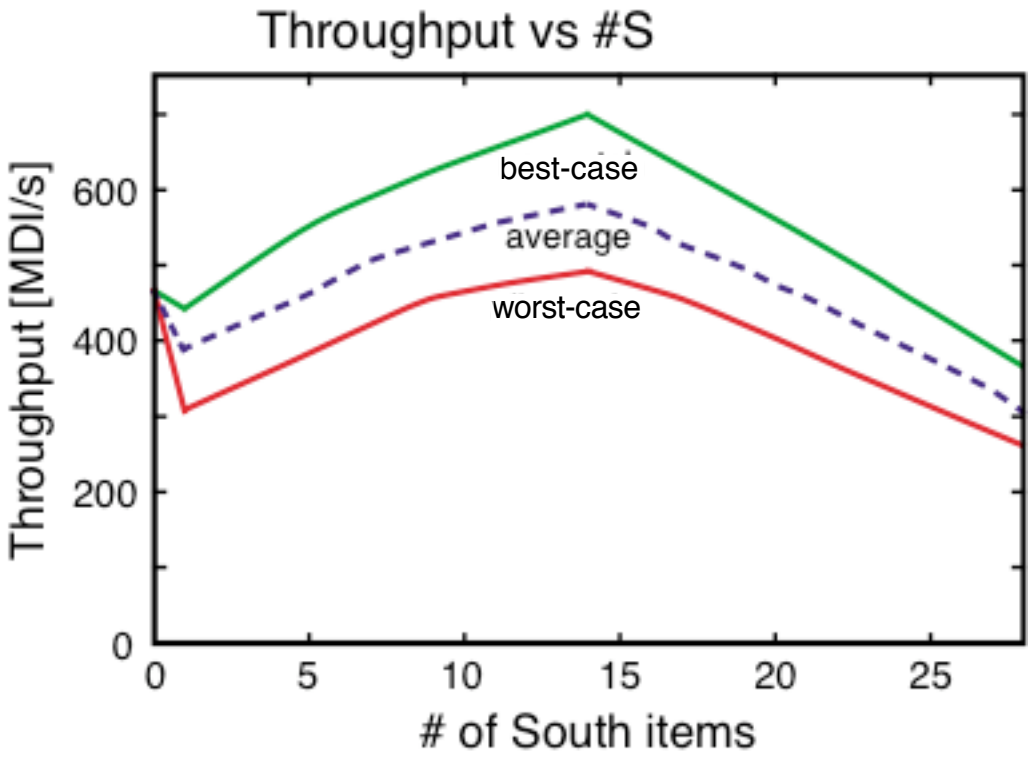


async mode



Average-Case Speed

- **From asP* counterflow pipeline chip**

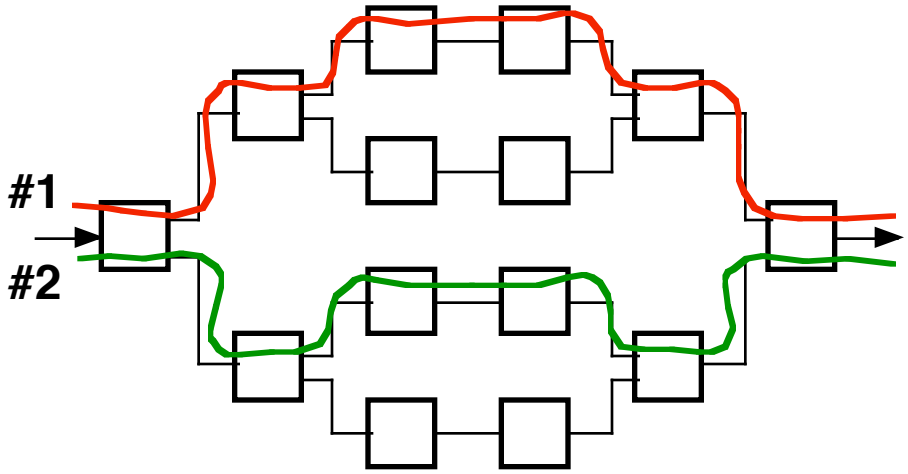


Architectural Freedom

- Can more freedom lead to better FIFOs?
- Better = lower power?
- Better = less latency?
- More concurrency?
- Different grain sizes (i.e. cycle times)?

A Non-Linear FIFO

- The idea:



- What is energy consumption?
- What is latency?
- What is cycle time of leaf cell (compared to root cell)?

Concluding Remarks

- Sun's UltraSPARCIIIi has async FIFOs
- Elsewhere..
  - Philips, IBM, Intel, ..
  - Academia
  - Start-ups
- Many challenges remain
  - CAD tools
  - Education