Circuits Without Clocks: What Makes Them Tick?

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Abstract

This document contains slides of a SunLabs Open House talk on 13 May 1998.

Circuits Without Clocks: What Makes Them Tick?

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Sun Microsystems Laboratories

A Historical Perspective

- Clocked versus unclocked circuits
- The first computers: clocked or unclocked?
- ENIAC ('46), ACE ('46), EDVAC ('46)
- Enabling Theory: Switching Theory ('38)
- A big problem: making *reliable* computers
- Non-synchronous, asynchronous, speed-independent, delay-insensitive, self-timed

Why No Clock?

- Speed

  average-case versus worst-case

- Avoid timing problems related to clock:

  Metastable behavior,
  Clock distribution, skew, jitter
  Scaling and its effects on delays

- Modularity:

  Re-usability
  Composability
  Incremental improvement

More: Why No Clock?

- Low Power

  Portable electronics.
  Budget constraint: total energy, not cycle time

- Architectural Freedom

  Concurrency at any grain size

- Robustness

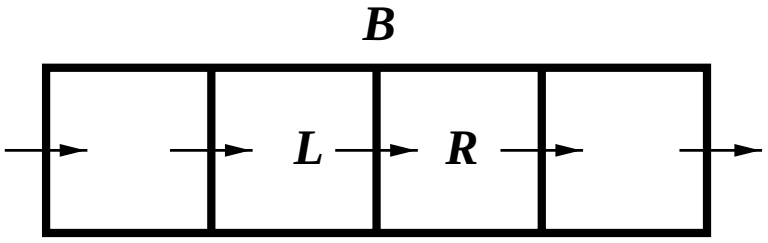
  Correct operation over a large range of supply voltages and temperatures

- Reduced electromagnetic radiation

  No clock harmonics in emission spectra

An Example: FIFOs

- FIFOs as basis for pipelines

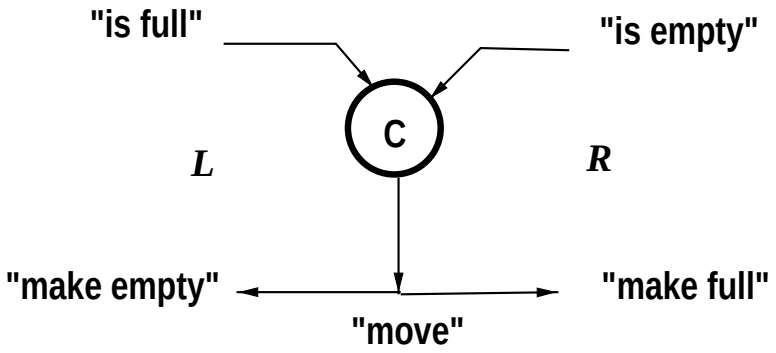


- Simple, local communication

- For each boundary B:
  If L is full AND R is empty, MOVE right

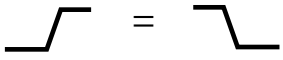
A MOVE In Control Path

- For each boundary B:
  If L is full AND R is empty, MOVE right.



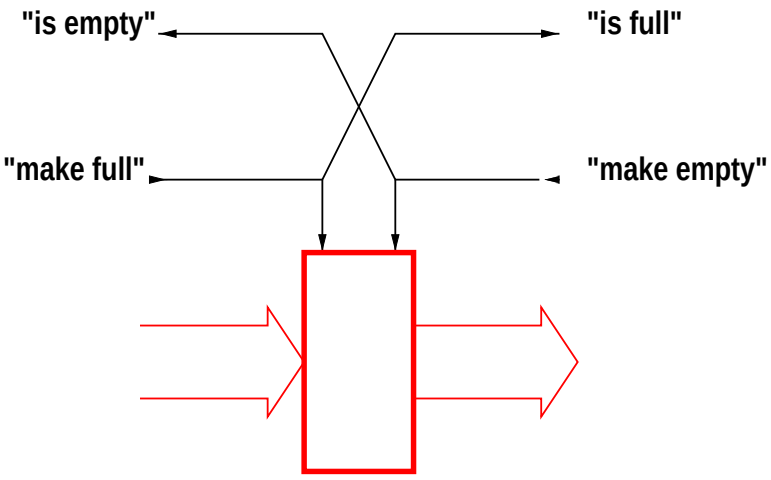
- C-Element = "AND" of events

- An event



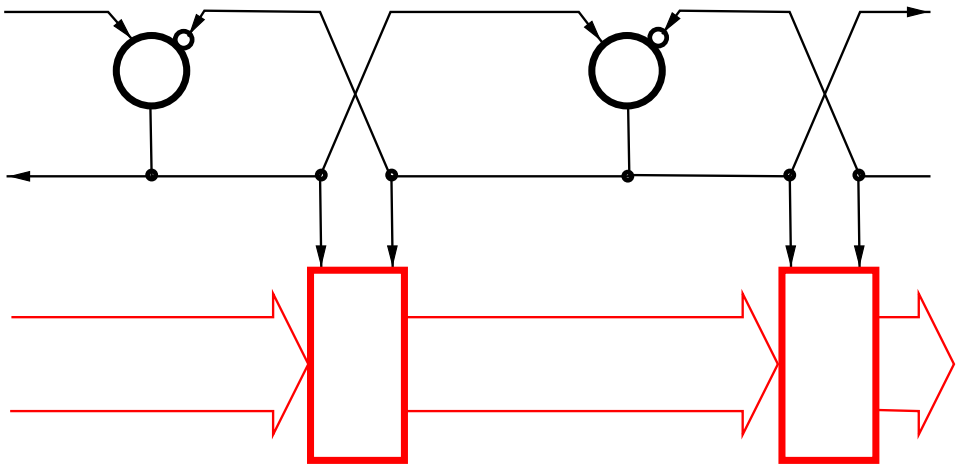
A MOVE In Datapath

- “make empty” = “make transparent”
  “make full” = “make opaque”



Control And Data Path

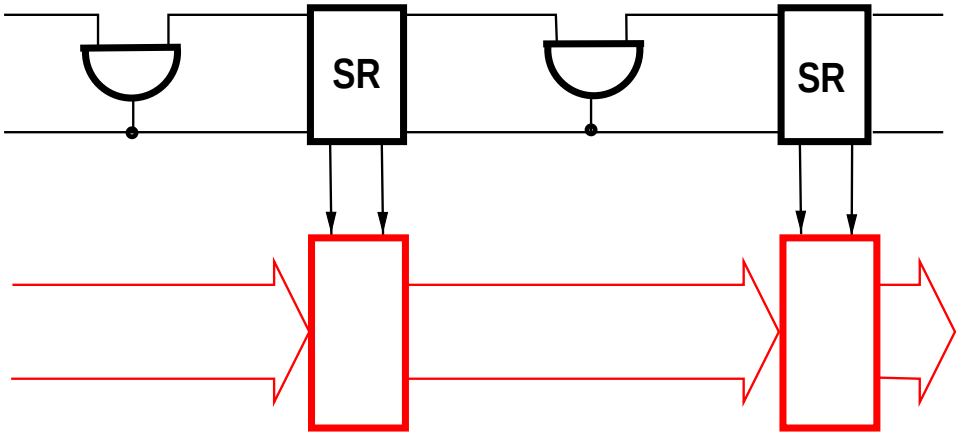
- Complete "Transition" FIFO



- Micropipeline: Add combinational logic

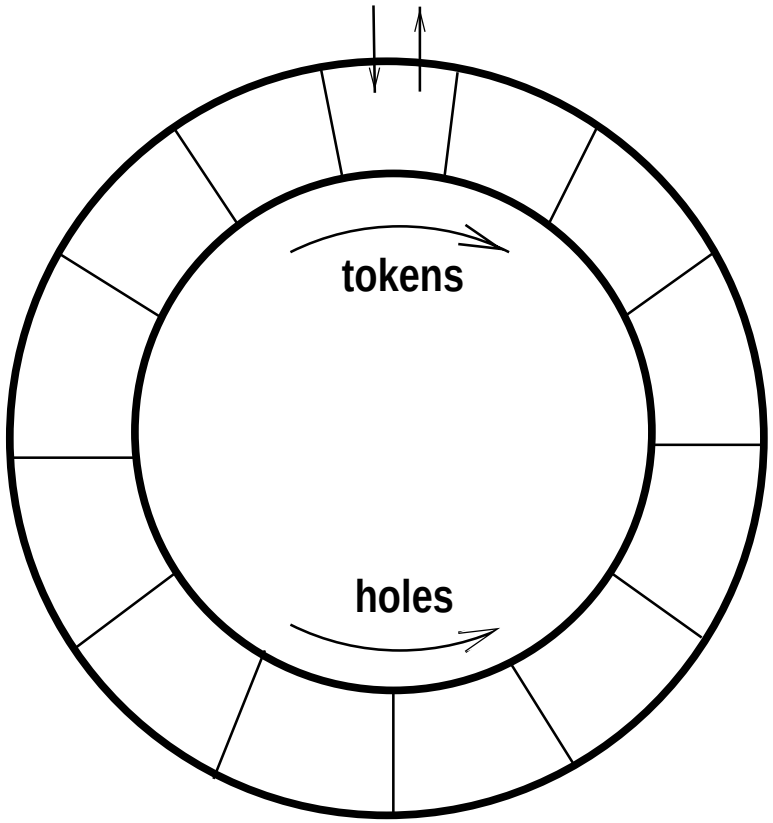
ASP* FIFO

- Uses standard elements in control and data path
- Level-signalling as opposed to transition signalling
- Delay constraints



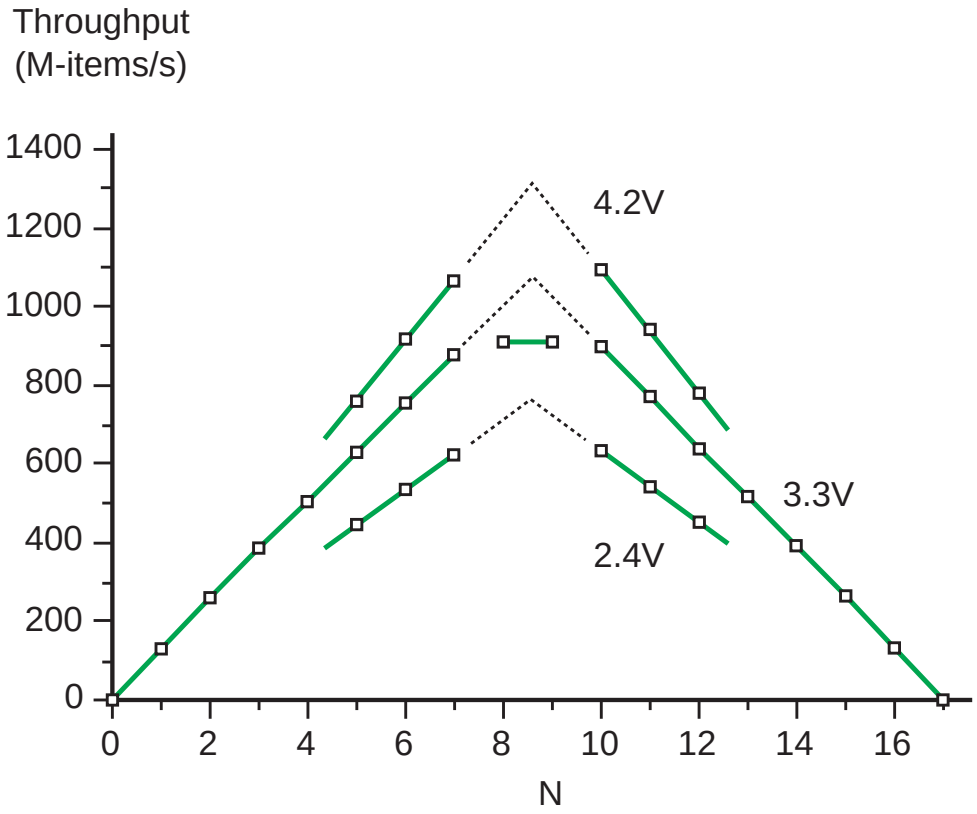
Async FIFOs at SunLabs

- Built and tested several ring FIFOs in .6μ.
- Main focus: speed
- Challenge: How to test speed of actual chip?



Speed?

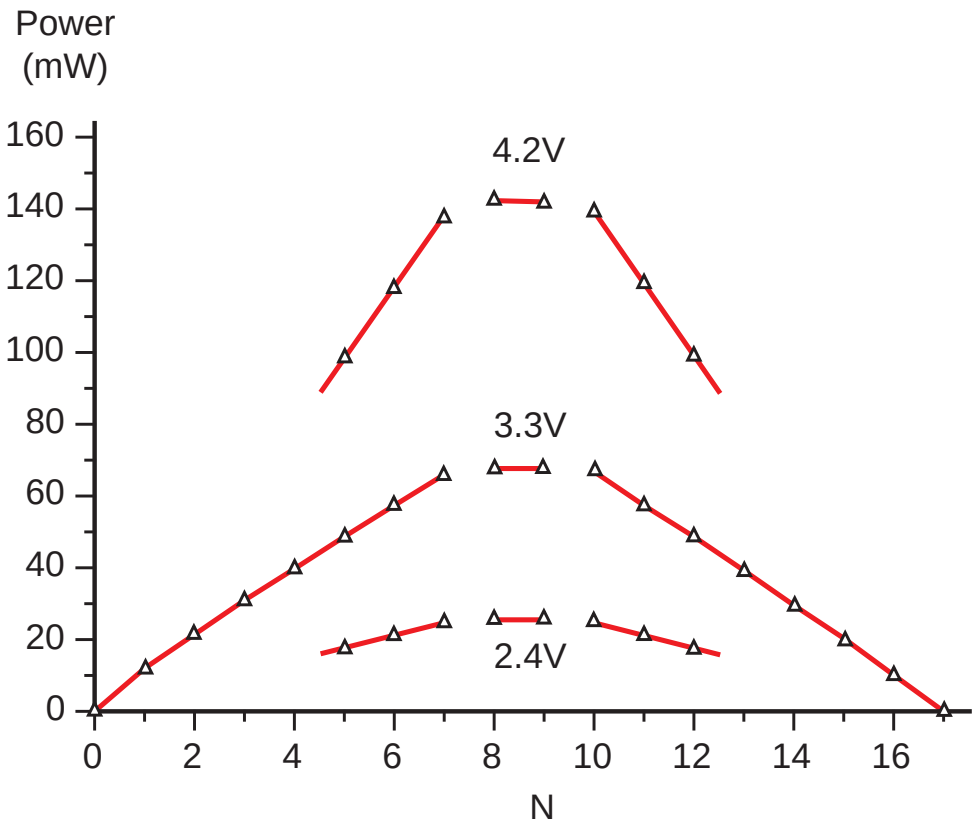
- Measurements from actual chip, ASP* FIFO



Throughput vs Number of Full Cells

Low Power?

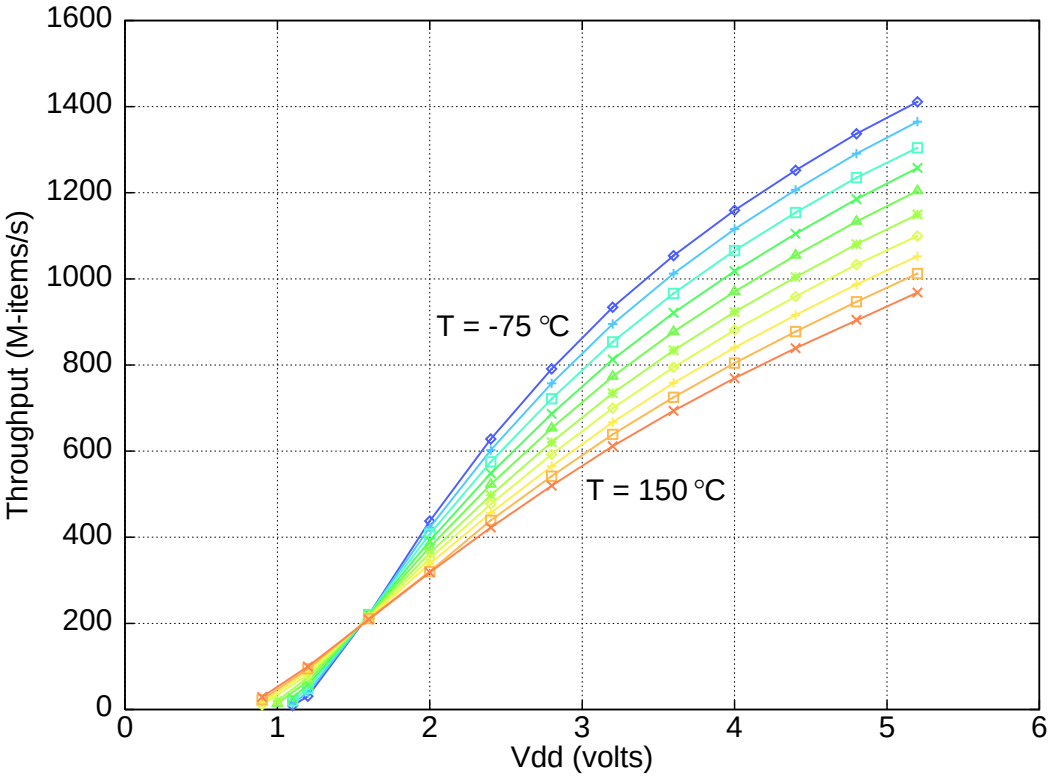
- Measurements from actual chip, ASP* FIFO



Power vs Number of Full Cells

Robustness?

- Measurements from actual chip, transition FIFO



- Max Throughput vs Power Supply and Temperature

More On Speed

- ASP* FIFO Ring
- 1 Giga Data Items/second (GDI/s)
  $\approx$ 5 gate delays
- Standard data latches
- As fast as fastest shift register AND more flexible

Still More On Speed

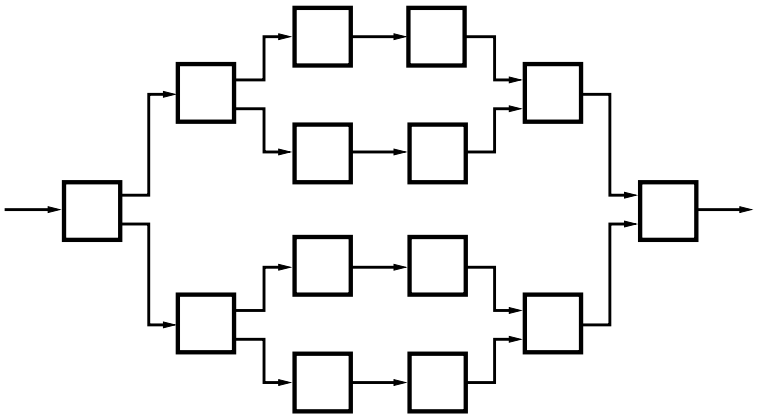
- Transition FIFO Ring
  - Non-standard data latches
  - 1.6 GDI/s $\approx$ 3 gate delays
  - Fastest FIFO on planet in .6μ.
- Transition Pipeline
  - Standard data latches
  - Conditional branching of data stream
  - .6 GDI/s $\approx$ 8.5 gate delays

Architectural Freedom?

- Can more freedom lead to better FIFOs?
- Lower power?
- Lower latency?

A Non-Linear FIFO

- The idea:



- What is latency?
- What is power consumption?
- What is cycle time of a "leaf" cell?
- Can you do this with a clocked design?

Meanwhile, Elsewhere ..

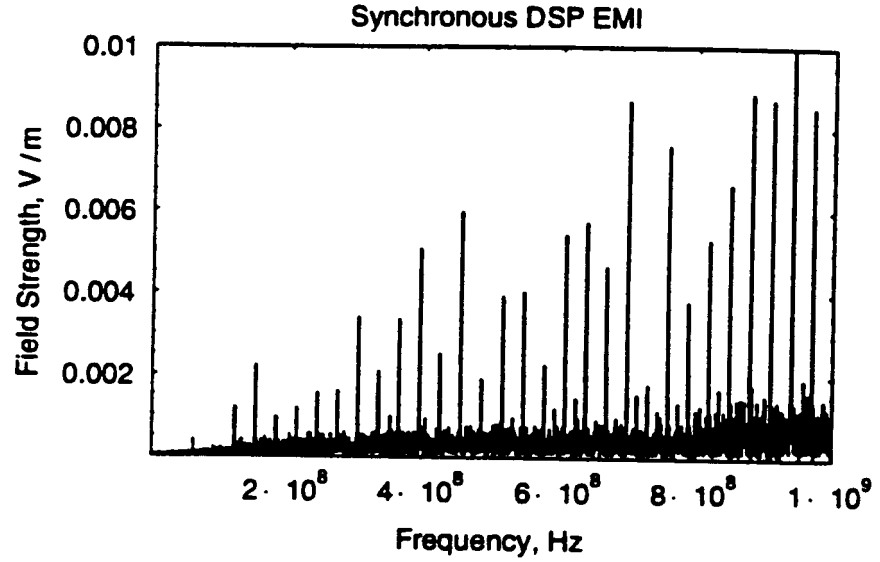
- At Philips. Their focus:
  - low power
  - low electromagnetic emission
  - VLSI Programming
- Designed over 10 chips
- Most complex: DCC Error Corrector
- Consumes 30-90% less energy than sync design
- No "clocks" in electromagnetic emission spectrum

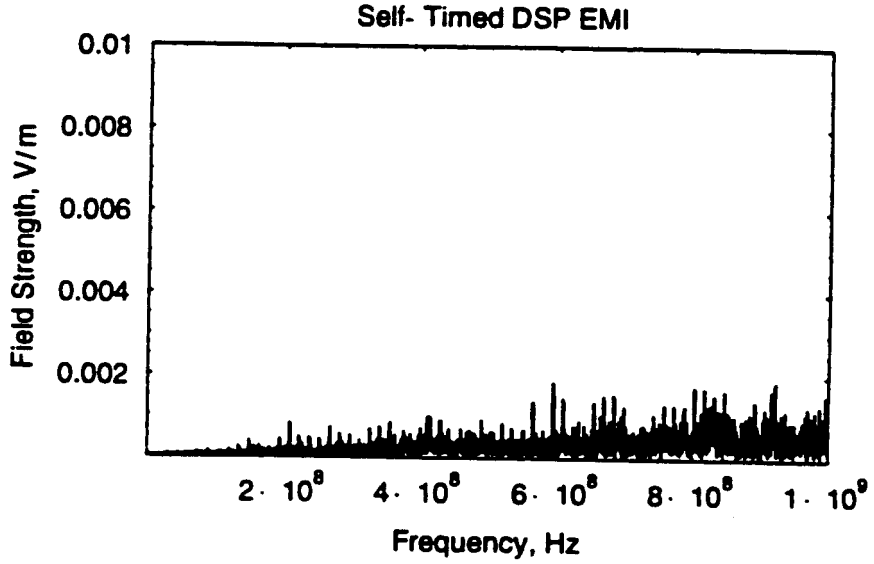
Meanwhile, Elsewhere ..

- At Manchester. Their focus:
  - low power
  - low electromagnetic radiation
- An asynchronous ARM for embedded systems
- Start-up Cogency. DSP chip for fax/modem
  - consumes 50% less energy than clocked design
  - MUCH lower noise generation than clocked design

EMI Comparison

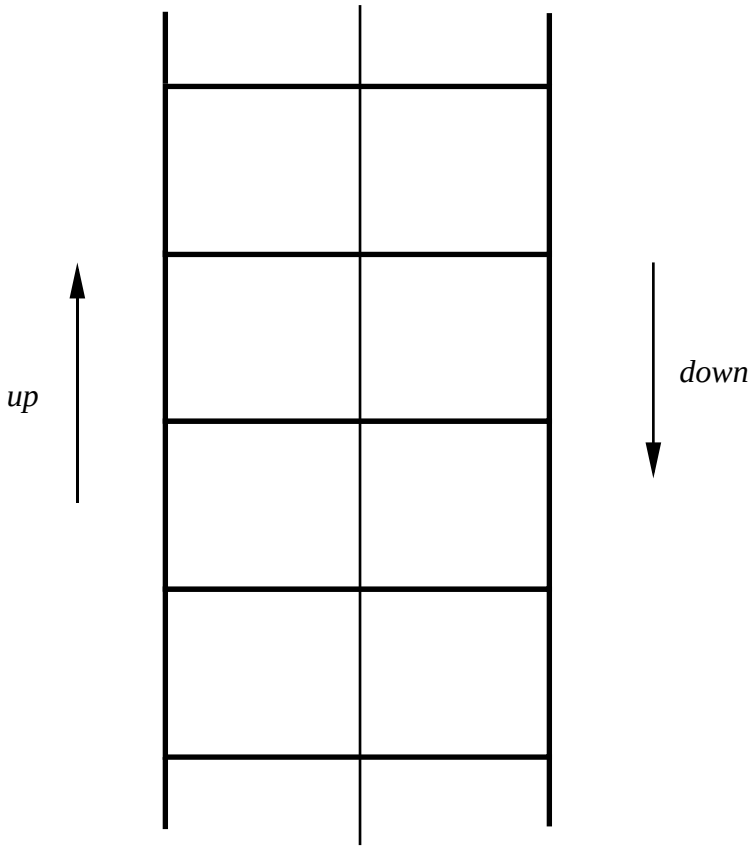
Source: Cogency's ASYNC98 paper.





The Counterflow Pipeline Test Chip

- The idea:



- Each up and down-datum that pass each other must exchange information.

Challenges

- Education
- Tools
- Enabling Theory
- Testing
- A few more success stories

To Clock Or Not To Clock?

- An expert's opinion:

  "But this is just clocked design.."

- What can we do for you?