Sun Microsystems Laboratories

Subject: **Logical Effort Slides**
Date: **September 18, 1997**
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SML#: **97:0508**

References:

Sproull, R.F., and Sutherland, I.E., "Logical Effort: Designing for Speed on the Back of an Envelope," IEEE Advanced Research in VLSI, C. Sequin, ed., MIT Press, 1991.

Sutherland, I.E., "Micropipelines," Communications of the ACM, June 1989.

Logical Effort

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SYMBOLS (normalized & unitless)		
WHAT	of stage	of path
Ideal inverter delay	τ	
parasitic delay	p	$P=\Sigma p$
delay	d	$D=\Sigma d$
number stages	1	N
electrical effort	$h=C_{out}/C_{in}$	$H=C_{out}/C_{in}$
branching effort	$b=C_{total}/C_{on}$	$B=\Pi b$
logical effort	g	$G=\Pi g$
effort or *total effort*	f=gbh	F=GBH
gate delay (unitless)	d=gbh+p	

LOGICAL EFFORT OF A GATE IS:

1) Number of times worse the gate is at delivering output current than an inverter with equal input capacitance.

2) Number of times more input capacitance the gate needs than an inverter would to deliver equal output current.

3) Number of times more slowly a ring of such gates oscillates than does a ring of an equal number of inverters. (ignoring parasitic delay)

4) Factor by which the "gain" of the logic gate is worse than the "gain" of an inverter.

WHAT'S WRONG WITH LOGICAL EFFORT?

1) deals poorly with parasitic capacitance.

2) ignores rise time of signals.

3) assumes series transistors act together.