GasP:
A Minimal FIFO control

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GasP Design Methodology

- Simple pipelines
- Branching and joining pipelines
- Join on demand through arbitration
- Conditional branch and join
- Scheduled branch and join
- Others
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GasP Control

- Reduced Complexity
- Six gate delay transactions
- Automated transistor sizing
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"A FIFO Data Switch Design Experiment"

- Two phase handshake protocol
- 583 to 629 million data transaction per second in a 0.6u process
- Asynchronous computing is fast!
- Trivial computing
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"Counterflow Pipeline Experiment"

- Two pipelines, data items flow in opposite directions
- Interactions depend on contents of data items
- asP* control
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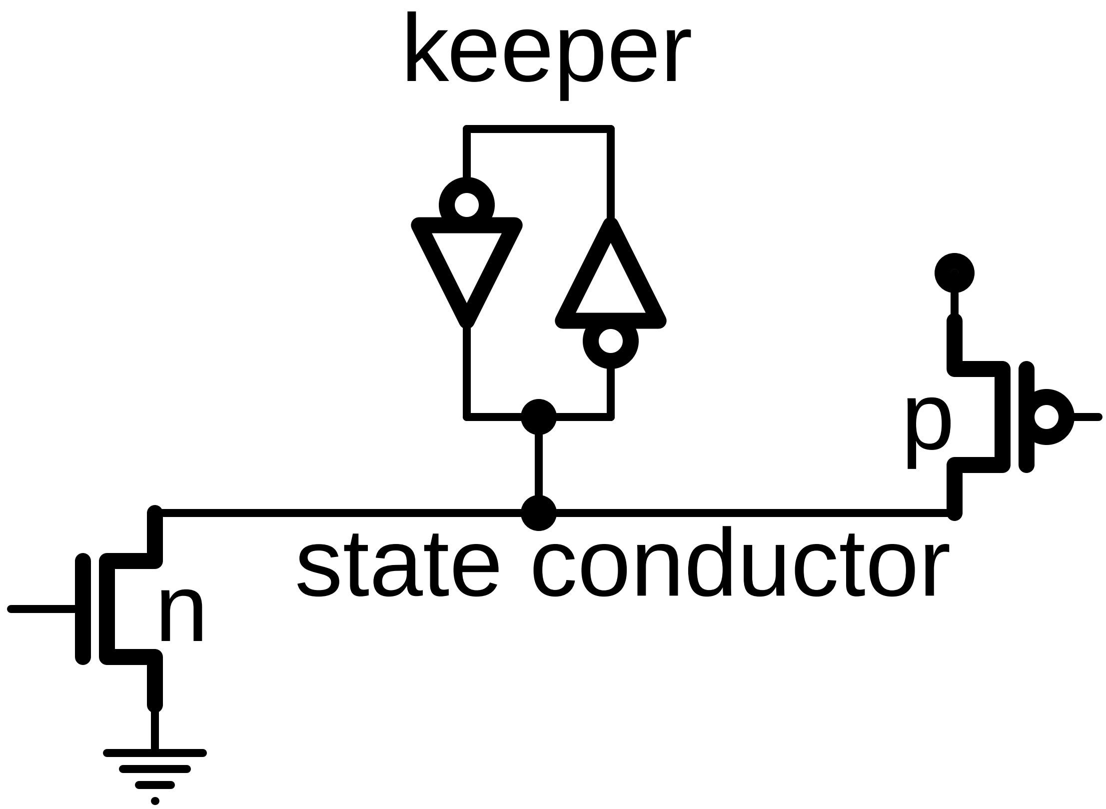
QUASI INVERTER



Dynamic asP drawbacks

- 1) Two types of basic control cells
- 2) Three gate delay pulses in six gate delay cycles
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SYMMETRY

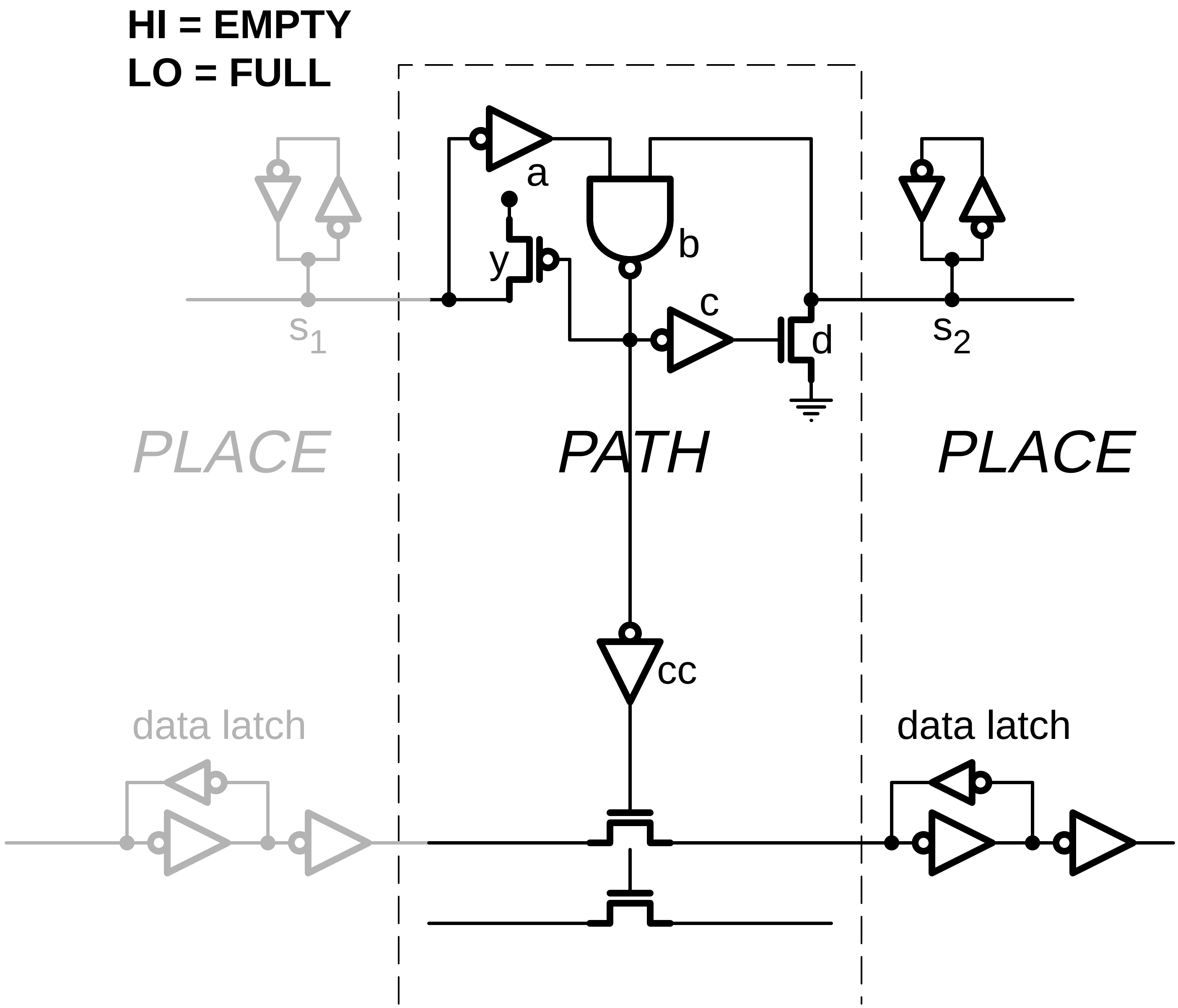
form	forward delay	reverse delay
dynamic asP*	3	3

odd and even control types
too fast forward

form	forward delay	reverse delay
GasP	3	3

one control type
uniform delay required

A GasP Stage


HI = EMPTY
LO = FULL
a
b
c
d
y
s_1
s_2
PLACE
PATH
PLACE
cc
data latch
data latch

FULL - EMPTY

$\downarrow$

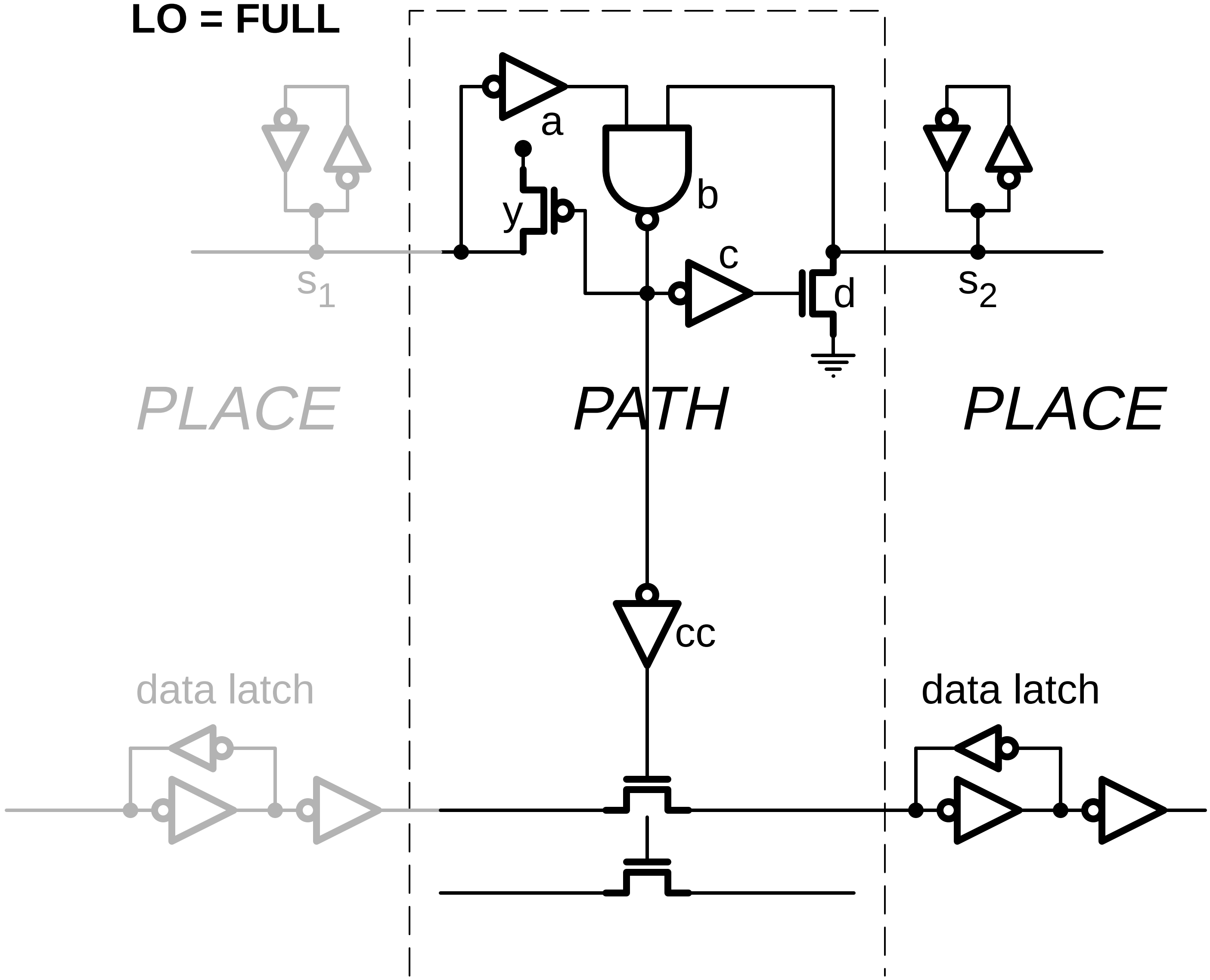
Copy Data

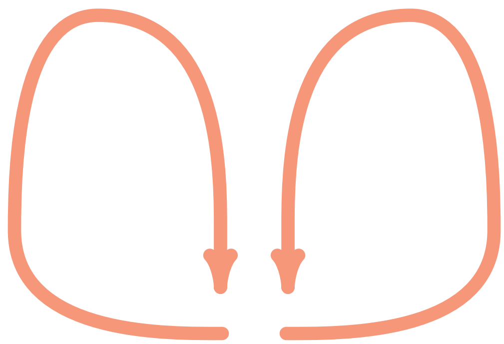
$\downarrow$

EMPTY - FULL

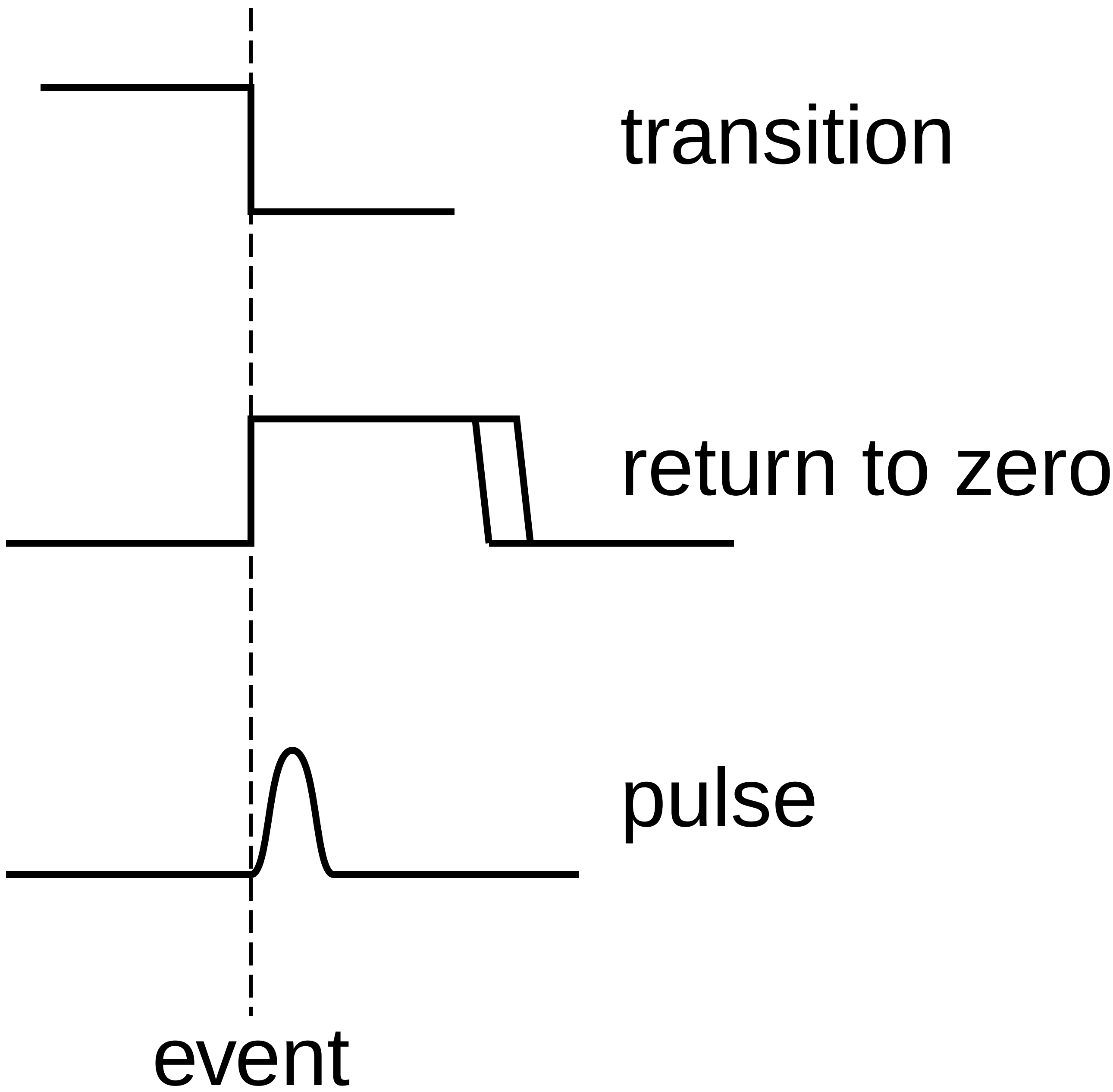
A GasP Stage

HI = EMPTY
LO = FULL

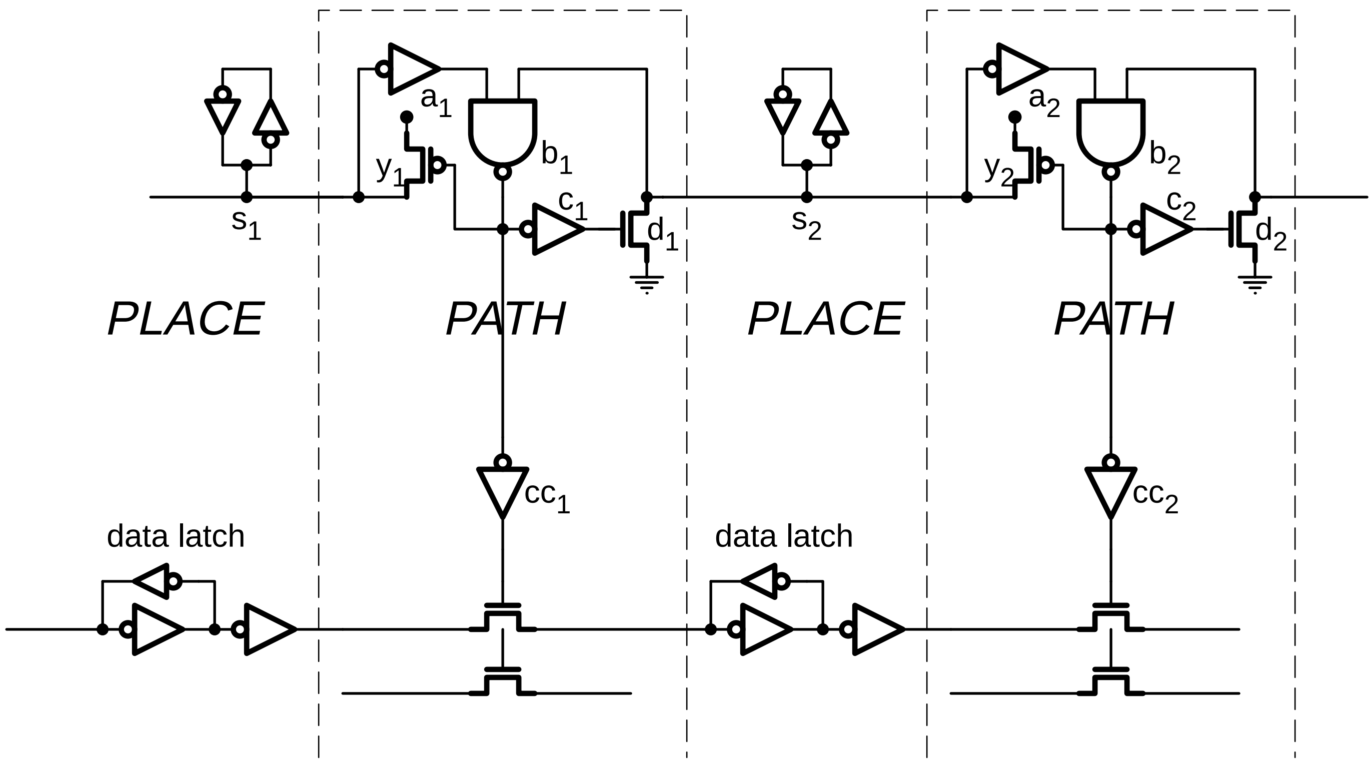




THREE EVENT ENCODINGS

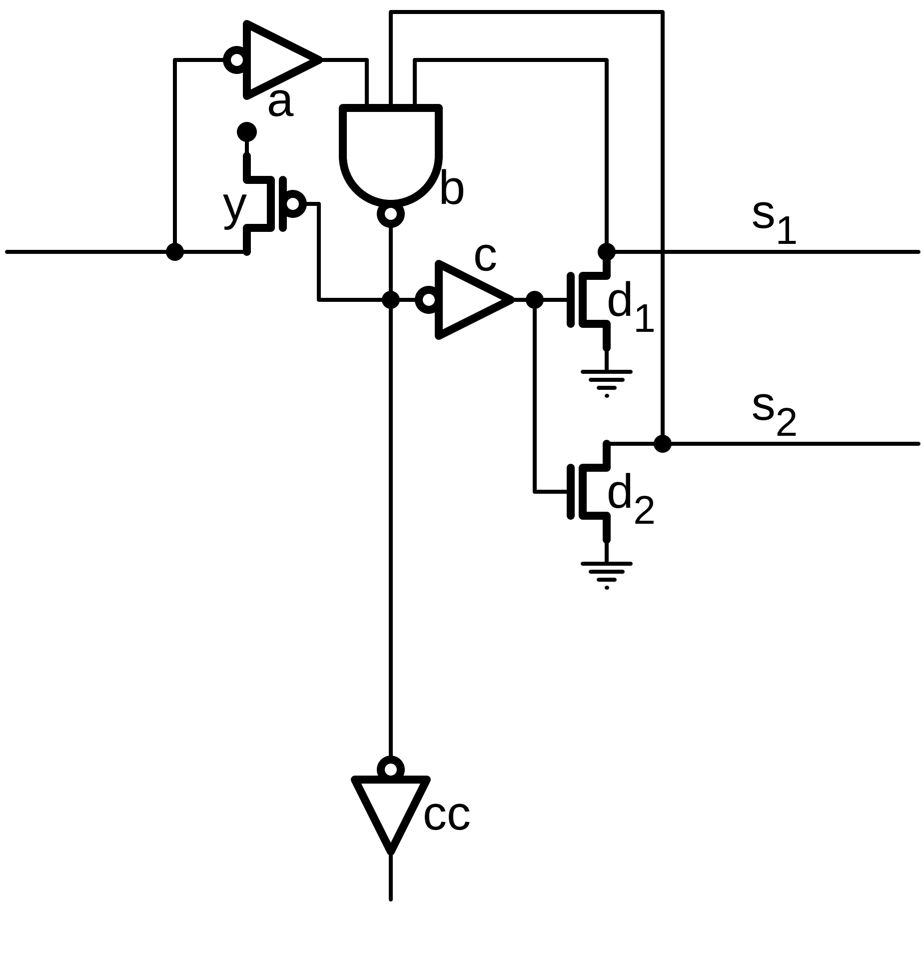


HI = EMPTY
LO = FULL

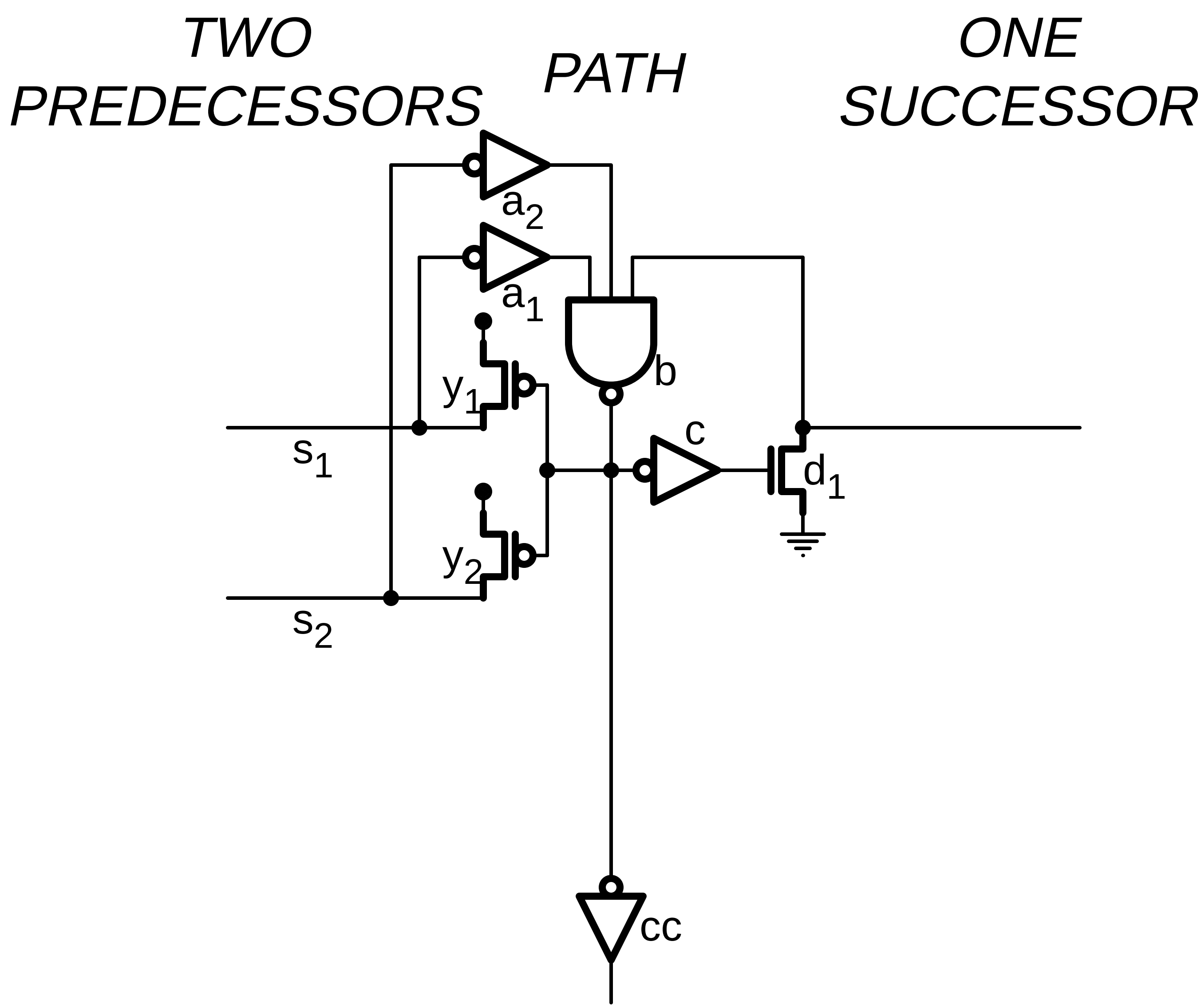


UNCONDITIONAL BRANCH

ONE PREDECESSOR | *PATH* | *TWO SUCCESSORS*

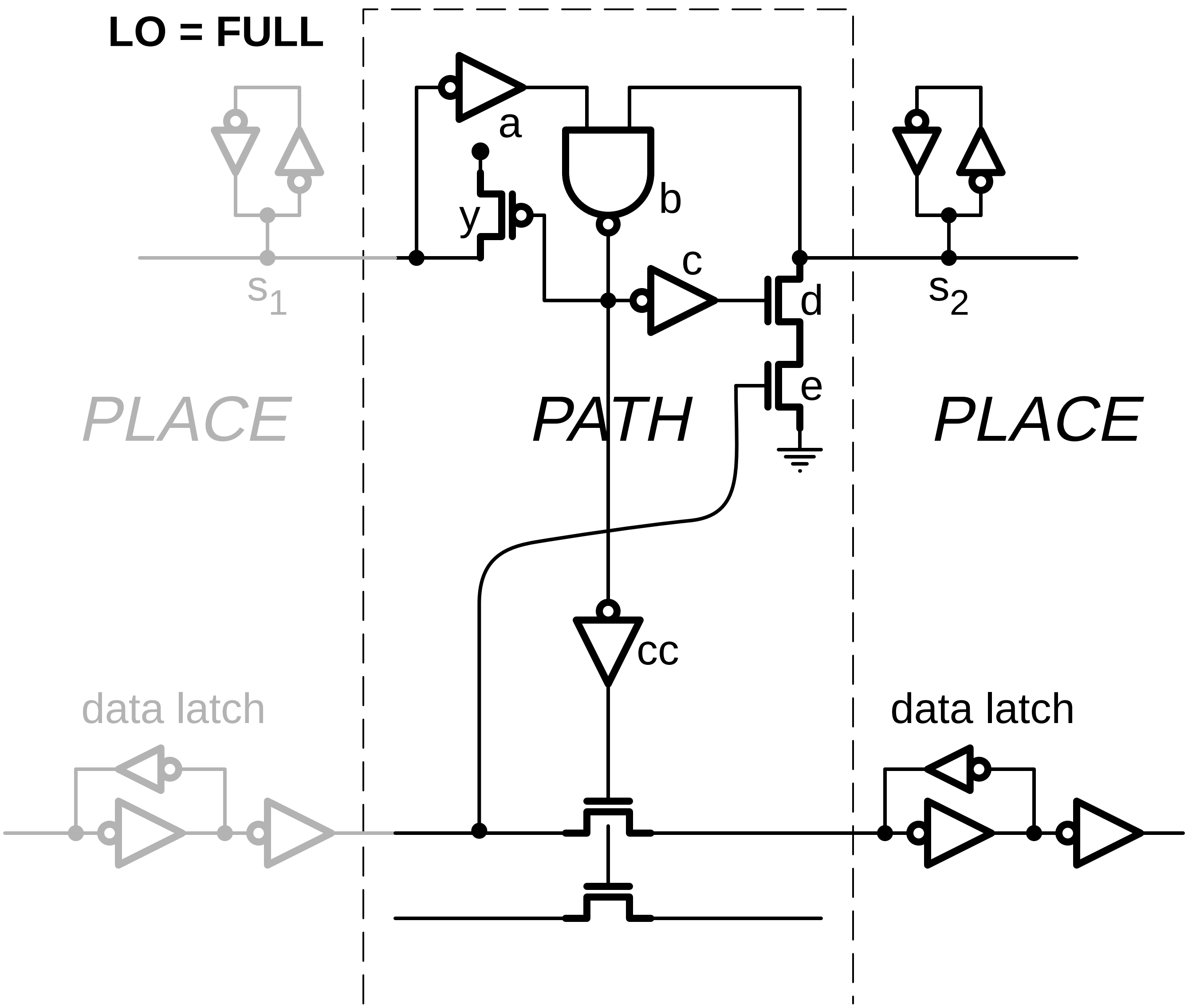


UNCONDITIONAL JOIN

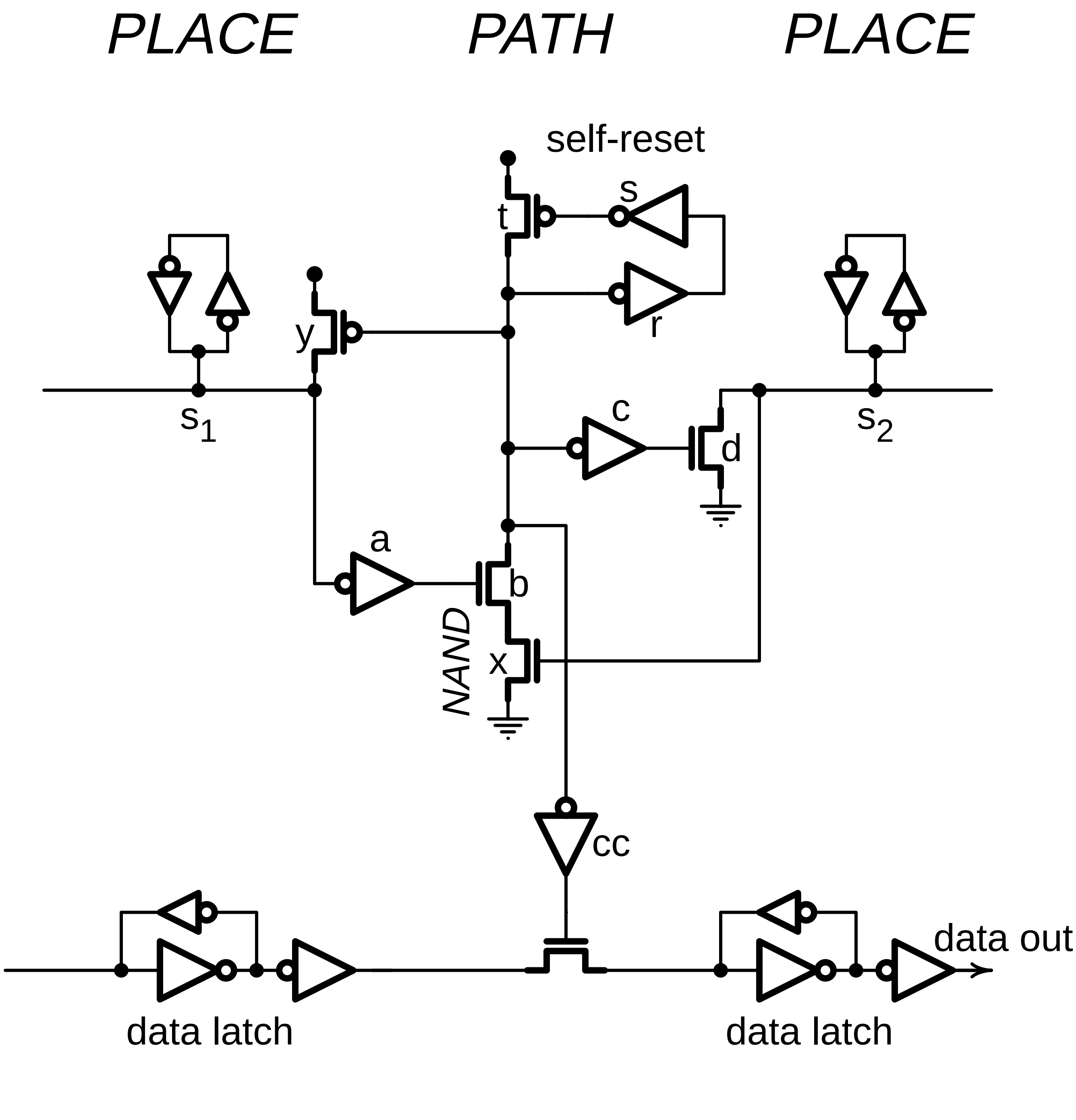


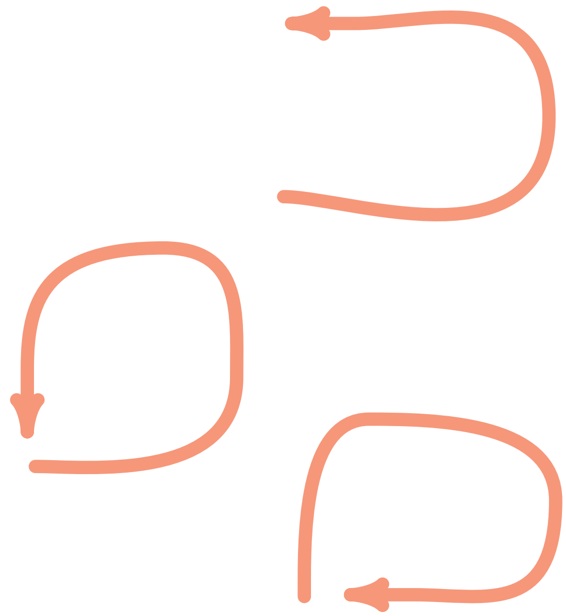
CONDITIONAL FILL

HI = EMPTY
LO = FULL



Self-resetting GasP





Power Supply Robustness

1.2V − 4.8V +

-
- nominal: 3.3V
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GasP Circuits: A Minimal FIFO Control

- Faith −> Speed
    - data transaction in six gate delay
    - throughputs in excess of 1.5GDI/sec in 0.35u
- Logical Effort −> Faith
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