Highly-efficient thermally-tuned resonant optical filters

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Abstract: We demonstrate spectral tunability for microphotonic add-drop filters manufactured as ring resonators in a commercial 130 nm SOI CMOS technology. The filters are provisioned with integrated heaters built in CMOS for thermal tuning. Their thermal impedance has been dramatically increased by the selective removal of the SOI handler substrate under the device footprint using a bulk silicon micromachining process. An overall ~20x increase in the tuning efficiency has been demonstrated with a 100 μm radius ring as compared to a pre-micromachined device. A total of 3.9 mW of applied tuning power shifts the filter resonant peak across one free spectral node of the device. The Q-factor of the resonator remains unchanged after the co-integration process and hence this device geometry proves to be fully CMOS compatible. Additionally, after the cointegration process our result of 2π shift with 3.9mW power is among the best tuning performances for this class of devices. Finally, we examine scaling the tuning efficiency versus device footprint to develop a different performance criterion for an easier comparison to evaluate thermal tuning. Our criterion is defined as the unit of power to shift the device resonance by a full 2π phase shift.

OCIS codes: (130.5990) Semiconductors; (130.3120) Integrated Optics Devices; (130.7408) Wavelength Filtering Devices.

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1. Introduction

Silicon-on-Insulator (SOI) based photonics continue to gain interest in computing system applications owing to the prospects of bringing optics close to the processor chip [1]. Compared to traditional electrical signaling, silicon photonics offers lower latency, higher bandwidth and potentially ultra low power consumption. Silicon photonic devices can be wafer scale produced on a SOI platform using established CMOS manufacturing practices at high yield and low cost [3–5]. Furthermore, a WDM point-to-point communication network can be constructed with silicon photonic components linking a number of CPU cores and scaling up computing system performance with minimal consumed energy [1,2 and 6,]. In one option, a WDM optical link is comprised of a modulator and MUX/DEMUX filters that are based on the resonant effects when built around a waveguide ring in SOI technology. Some key benefits for this class of devices are high operating speed, low modulation power, low optical loss and compact size. Additionally, these components must have predictable and stable wavelength characteristics throughout the range of operation. Due to their resonant nature, a ring device has a spectral window of operation that is extremely narrow of the order of a picometer. Furthermore, in our target system design, we use a channel spacing of 200 GHz (1.6 nm) to accomplish WDM routing [1,6]. The optical components (modulators, filters etc.) would ideally have their wavelength resonances centered on the ITU grid enabling high fidelity color separation in a multichannel WDM photonic fabric. Unfortunately, the accuracy of positioning these peaks is mainly influenced by the fabrication tolerances and the combination of these errors can radically shift a ring's resonant peak off design targets. Such manufacturing errors can require excessive tuning to operate this class of devices in a WDM network [1]. Thermal tuning is a convenient approach to shift each resonance to its design targets however this correction can consume significant power depending upon the device structure.

A number of prior efforts [7–12] have addressed tuning of the microphotonic devices and micro-resonators under thermal control. One of the key metrics quantifying tuning quality has been the so called "tuning efficiency". Typical values are about 4 mW/nm [7] that were measured for III-V rings while silicon photonic rings built on the SOI substrate report a similar thermal tuning efficiency [8]. In other efforts the tuning efficiency has been improved by 5x when combining shrinking the device footprint and direct filter heating [11]. Still, it has been particularly challenging to quantify the metric of thermal efficiency reported in the literature and extract relative performance in a meaningful way when comparing resonant devices of different structure and layout.

In CMOS based resonators the heat generated in the ring is dissipated through heat spreading in the substrate and in the top metal, dielectric stack up. Because the thermal

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conductivity of the crystalline substrate underneath the ring is so large then significant power must be applied to shift the resonance across its free spectral range to align to a laser channel and correct potential mismatches of a 2π phase shift or more. The main purpose of our communication is to report a 20x improvement in tuning efficiency of a ring MUX filter upon co-integration of a back-side etch pit with silicon micromachining technology. The selective removal of the entire SOI handler substrate under the device footprint has substantially increased the device thermal impedance and dramatically improved tuning performance. A second objective of this communication is to clarify some of the other issues affecting the so called "tuning efficiency" metric by examining how tuning performance scales as the device footprint shrinks. Based on this perspective of scaling we introduce a new figure of merit that is defined as the power to shift a full 2π range in the device resonance. The benefit of this new metric is to develop a more effective figure of merit to quantify the actual efficiency for thermal tuning of this class of devices for WDM applications.

2. Device description

Thermal tuning of our resonators was accomplished with structures designed and implemented in a commercial, high yield, 130nm SOI CMOS process. More specifically the devices were built on Freescales' 130 nm process node that consists of six metal layers of Cu intertwined with interlayer dielectrics composed principally of silicon nitride (SiN_x) and silicon dioxide (SiO_2). We can expect the structural integrity of the Cu, silicon nitrides and dioxides to have characteristics inherent to PVD, CVD and PECVD grown layers respectively, since they are a generic property common to nearly all CMOS technologies. Furthermore, the thermal and electrical transport characteristics of these films may differ substantially from bulk properties. Rings of different diameters (24 μm, 40 μm, 60 μm and 200 μm) were fabricated and characterized. Their cross-section is schematically illustrated in Fig. 1a. A typical reported tunable circuit configuration positions the metal heater above the optical silicon waveguide with a dielectric layer in between [7,8]. In this approach the temperature of the optical waveguide is raised in its vicinity with an appreciable fraction of tuning power potentially radiated away from it.

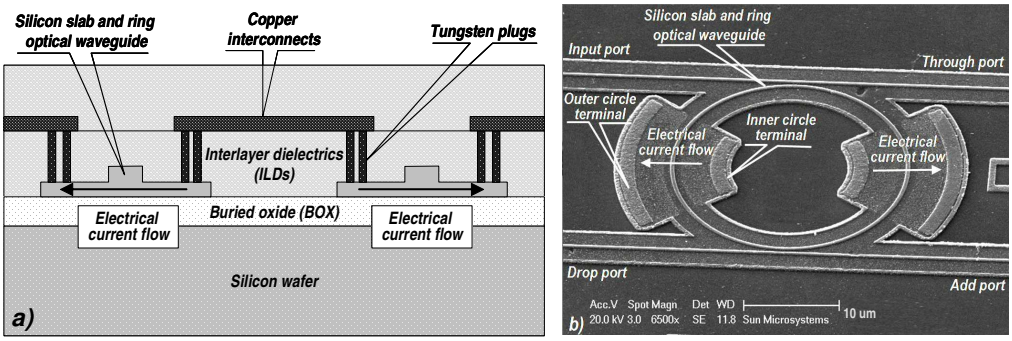

Fig. 1. Thermally tunable resonant waveguide structures: (a) schematic cross-section, (b) SEM image of the silicon waveguide ring with 24 μm diameter and its bus waveguides without the metal interconnects and interlayer dielectrics.

In our rings the electrical current is forced directly through the optical ring waveguide by lateral conduction. Multiple tungsten plugs connect to the doped silicon slab that carries the waveguide. Therefore the temperature is raised in the optical signal path potentially improving the tuning power efficiency. Figure 1b contains SEM image of the waveguide ring with two straight waveguide buses and the thermally active silicon slab sections. The slab is formed around the waveguides by a complete silicon removal down to the underlying buried silicon oxide therefore further isolating the areas elevated in temperature and increasing the structure's thermal impedance. The 24 μm diameter ring filter is shown without the dielectric CMOS layers and its metal interconnects to better visualize its details. Figure 2 is a top view

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optical micrograph of the manufactured tunable filter circuit with a respective scale. The indicated optical ports are based on the grating couplers and are immediately accessed by the external optical fibers.

Our ring MUXes are based on ridge waveguides that were optimized for low loss and tight bending to enable compact device footprints. They were built with waveguide thickness of 300 nm, width of 360 nm and slab height of 150 nm. This waveguide structure only supports TE mode. The slab and ridge sections of the rings were intentionally doped for electrical transport with resistances of several hundred ohms. The bus waveguides were provisioned with grating couplers that facilitated optical access to the devices with low coupling losses of about 2 to 3 dB per unit.

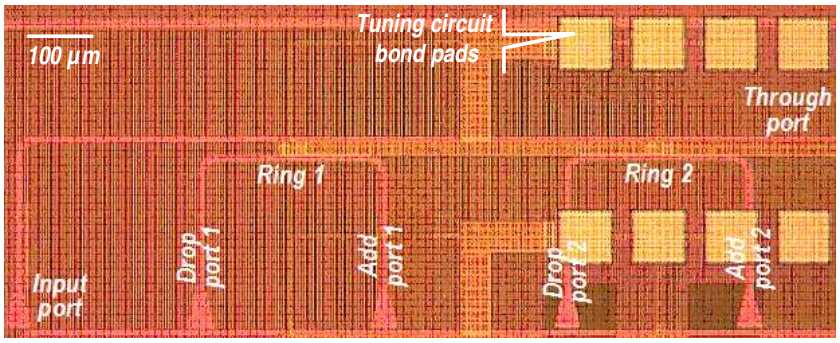

Fig. 2. A fragment of the MUX/DEMUX circuit with two thermally tunable rings and their respective waveguide ports.

As seen from Fig. 1a the silicon waveguiding structures to be tuned are surrounded by a CMOS stack up that is composed of multiple layers of vias, copper interconnects and different dielectrics. The vias are cylindrical metallic structures connecting vertically the copper interconnects to the active silicon and to each other in their respective layers. They are approximately 0.2 µm in diameter, arrayed with nearly one micron pitch and are 0.5 µm tall. This waveguide environment forms a thermal conduit that may essentially extract the delivered tuning power away from the silicon waveguide ring and affect the efficiency of the tuning itself. The rings are featured with a twin silicon heater system (Fig. 1b), each heater is actuated with electrical current that flows between the inner circle terminal and outer circle terminal.

3. Thermal tuning performance

Light from a tunable laser source was launched into the input filters' ports via the grating couplers and their spectral response was monitored as the current was applied to the heaters. Current, voltage and the corresponding power level are accurately monitored and maintained. The 200 µm diameter ring optical performance is shown in the Fig. 3 for a variable applied electrical power and its spectral response measured. Due to the thermo-optic coefficient of silicon as the temperature increases, the silicon ring refractive index increases resulting in the shift in its resonant peak to longer wavelength. The free spectral range for the filter, shown in Fig. 3, is about 1 nm. Its resonance peak can be shifted by 2π with 82 mW of applied electrical power. The amount of wavelength (and phase) shift is observed to have a linear dependence on the electrical tuning power indicative of a linear thermo-optic effect. In our case the thermal efficiency for thermal tuning of this ring filter equates to about 80mW/nm which is consistent with the geometry of the ring.

#130214 - $15.00 USD Received 16 Jun 2010; revised 16 Aug 2010; accepted 16 Aug 2010; published 23 Aug 2010

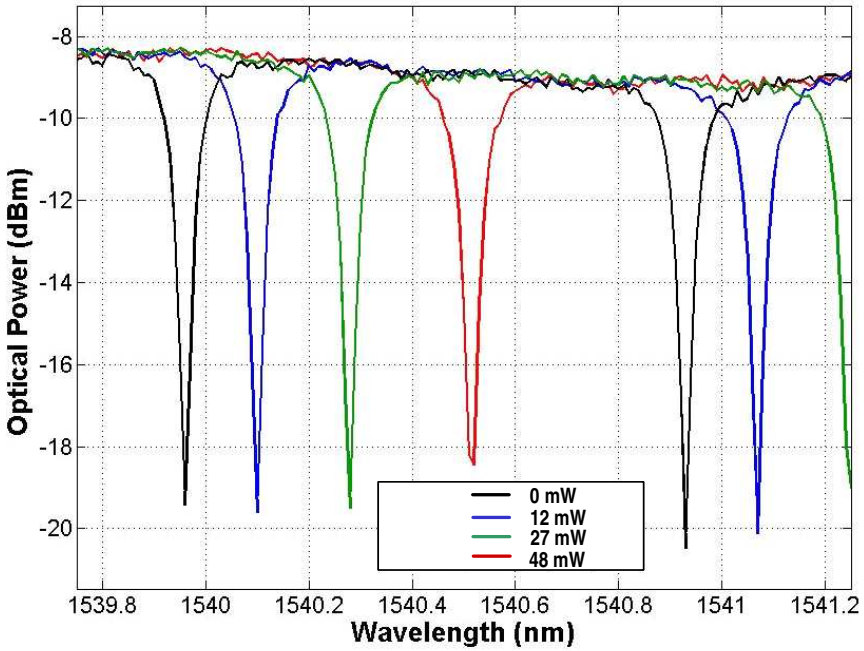

Fig. 3. Filter transmission versus wavelength as a function of applied power to a ring MUX of 200 µm diameter.

Previously we have reported on the tuning performance of CMOS rings of different radii when thermally tuned with applied electrical power [12]. These devices are also built in the same 130 nm CMOS node and have an identical heater geometry in which current passes from the rib section through the interior of the ring. The devices have ring diameters ranging between 24 µm and 60 µm. Figure 4 plots tuning performance versus power for several different ring radii. The tuning efficiency of our smallest ring is 15 mW/nm. The slopes of the resonant shift versus power are different depending on the ring radius indicating a larger wavelength shift for a smaller ring. Clearly the tuning efficiency of the small 24 µm ring is far better than the 200 µm ring in Fig. 4. Upon inspection the resonator shift versus applied power is fit well by an inverse relationship on the device radius. Some factors contributing to such a dependence are as follows:

1) From simple resonator equations the change in wavelength for a given index change is independent of the ring radius.

2) As the ring size increases more power or heat has to be applied per unit active length to achieve the same amount of wavelength shift.

3) Finally, the thermal impedance of a hot disk is approximately inversely related to the radius. This effect may not be mutually independent from issue 2).

Hence, we anticipate that the shift in wavelength of a resonator results from the three effects in which an inverse dependence on the ring radius develops.

#130214 - $15.00 USD Received 16 Jun 2010; revised 16 Aug 2010; accepted 16 Aug 2010; published 23 Aug 2010

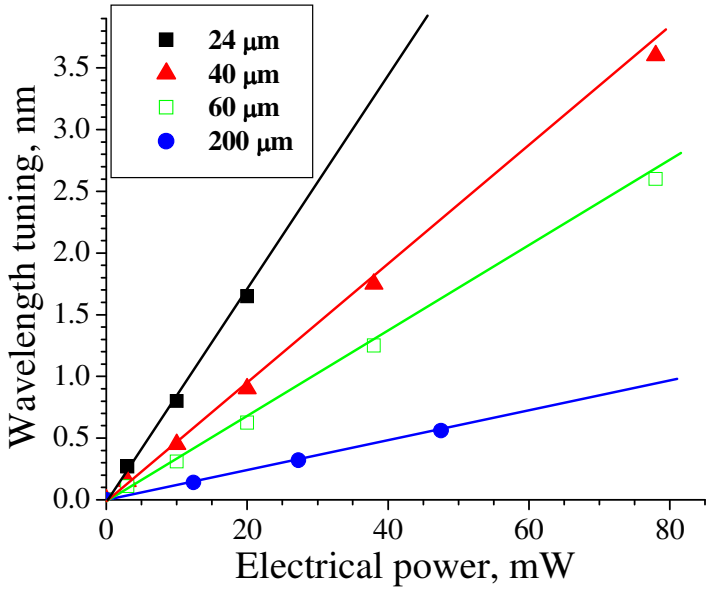

Fig. 4. A linear dependence of wavelength shift with applied electrical tuning power shown for different diameter rings.

Given the inverse dependence of thermal efficiency on ring radius identified above it may seem sensible to design WDM filters using smaller diameter rings in order to minimize the applied power for tuning a given wavelength range. Based on this sole criterion alone WDM designers would be tempted to design systems with the smallest ring radius possible to minimize overall tuning power. Nevertheless, there is another relevant tuning performance metric to consider in WDM applications which is the power required to shift a resonator within its free spectral range. To evaluate this metric we recall that the wavelength change required for a full 2π phase shift actually decreases with ring radius as follows from simple resonator theory. Combining this with the above relationship, we can further conclude that the applied power needed to tune a ring across a full 2π phase shift is actually independent of the radius of the ring. Further, this latter metric is particularly useful when combined with the cyclical or repetitive property of a filters' frequency characteristic. For example, instead of tuning the device over multiple orders to correct shifts away from design targets it is possible to assign the laser to a higher order mode of the ring filter and then tune only over a 2π phase shift to achieve the WDM alignment. This can reduce excessive tuning power required to overcome micro fabrication errors that otherwise may need significant correction across multiple orders of the filter. Furthermore this latter metric enables comparative analysis of the ring tuning efficiencies that are actually independent of ring size. Thus we suggest a new figure-of-merit defined by the power needed for a 2π phase shift in addition to the mW/nm tuning efficiency widely used for this class of devices.

4. Co-integration of back-side etch pit

Our device design of an isolated ring/disk waveguide device with a locally removed substrate from underneath it is accomplished herein using a chemical etch process. Our approach differs from previous methods that report an undercut of silicon waveguides on an SOI platform [13,14] or polysilicon waveguides in bulk silicon substrate [15,16] particularly as viewed at the local environment surrounding the device. The MEMS community has successfully demonstrated localized substrate undercut to improve sensitivity of their thermal

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components [17]. In previous undercut approaches the application to thermally tuned ring devices has not been reported. In our approach the silicon substrate is removed and this effectively eliminates a heat sink from the device's immediate proximity. Regardless of the given substrate thickness the location of the back-side silicon material from beneath the footprint of the resonant structure could be accurately identified and extracted. In our demonstration the process for the back-side substrate removal is based on wet selective chemistry. Silicon on insulator platform provides a natural etch stop in the case of silicon oxide. The approach could of course be extended to dry etch processes as well. Both the dry and wet etch chemistries could be readily optimized for high selectivity processes that react with the silicon substrate only while keeping the silicon oxide intact.

The standard 130 nm SOI-CMOS processed photonics chips [8,12] have been thinned down to 200 µm. The back side is polished to an optical finish and PECVD coated with low stress silicon nitride layer of 300 nm thickness. This back-side nitride is selectively dry etched to pattern its surface into an array of square or rectangular openings down to silicon matching the locations of photonic resonant structures on the front-side of the chip. The nitride openings are effectively sized to accommodate for the anisotropic nature of hydroxide wet etching of silicon and to result in the undercut of designed area beneath the photonic device (Fig. 5). The openings are aligned to [110] silicon direction.

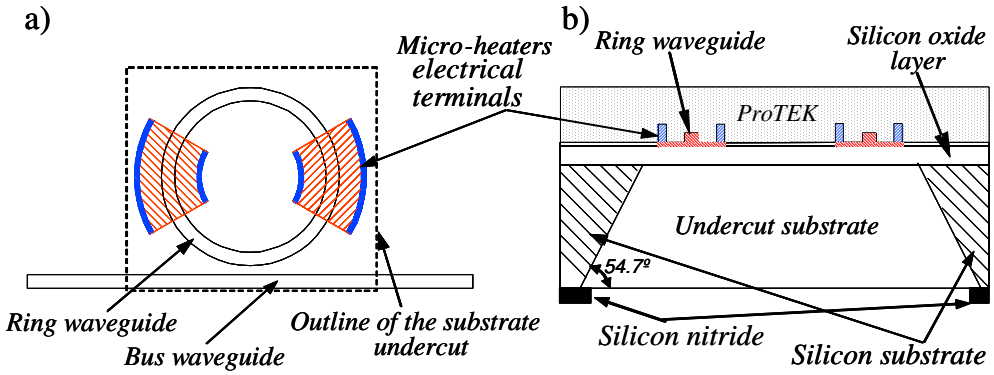

Fig. 5. Silicon photonic resonant structures with a substrate undercut. Top view (a) showing the heating elements and undercut area, and a respective cross-section (b) displaying the front and back side masking layers.

A ring of 40 µm diameter, for example, would need a window size on the order of 400x 400 μm^2 large in the back-side silicon nitride in order to achieve an undercut below the ring with ten times its respective area. A further reduced chip thickness and a substrate undercut performed with a highly directional dry etch would substantially reduce the amount of the required etched silicon substrate and make the footprint of the back-side hard mask window equal to that of the actual device on the front side.

The wet etch is carried out in the hydroxide bath and therefore requires adequate front-side device circuitry protection to make sure the resonant structures remain unaffected and their performance unaltered except for the enhanced thermal impedance and improved thermal tuning efficiency. To ensure this, a ProTEK B3 resist from Brewer Science, Inc [18]. is spin applied to the SOI-CMOS chip front side and properly cured (Fig. 5b). It forms approximately a 3 µm thin uniform layer specially formulated to withstand a hydroxide bath at temperatures and durations necessary to micromachine silicon into the designed structures. The masked chip is immersed into a 30% (by weight) KOH solution which is maintained at 80°C with a provision for continuous agitation by magnet stirring. The (100) plane silicon etch rate at these conditions is 1.37 µm/min. To clarify, the back side etch pit is formed with (111) plane silicon sidewalls as the etch rate in this crystalline direction is at least 40 times slower than that of the (100) plane such that little attention has to be paid to the amount of hard mask silicon nitride undercut. Therefore accurate back-side etch pits are attainable as

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defined by the photolithographic process. As the etching progresses, it reaches the silicon oxide layer which carries the silicon photonic device structures. The silicon oxide etch rate is also several orders of magnitude lower than the (100) silicon etch rate. In our demonstration the oxide thickness is 0.8 μm. A highly-selective hydroxide wet etch eliminates the need for precise timing. The cured front-side coating is stripped in O_2/CF_4 plasma without residue to regain original access to the SOI-CMOS front-side circuitry and optical input ports. The (111) facet sidewalls and the SiO_2 box then act as an effective stop-etch so that the handler substrate removal process can be accurately defined with photolithographic precision.

The silicon dioxide in the SOI platform is grown stress free. Limited residual intrinsic stress is expected at that interface. Once the substrate is removed from under the resonant optical device it is situated on and supported by this stress free layer. The device carrying the silicon oxide membrane is held by the remaining silicon substrate under the rest of the circuitry where the thermal isolation is not required. The devices isolated and suspended by the undercut remain mechanically supported and stable. The described process could be readily demonstrated on the wafer level in a batch process. It is tool-compatible and chemistry-compatible with conventional back-end MEMS manufacturing.

Figure 6 shows the tuning performance of a 200 μm diameter ring after selective removal of the handler substrate as described above. Upon comparing Fig. 3 and 6 it is clear the wavelength shift of the back-side pitted filter has dramatically increased per unit of applied power compared to the unetched filter. In Fig. 6 tuning with 3.9 mW of applied power is observed to produce a 2π phase shift which amounts to tuning of 4 mW/nm. We have recently demonstrated that identically designed and structured rings of different diameter would experience the same amount of resonant peak phase shift for a given applied thermal power [12]. Provided that this observed trend holds for substrate undercut rings scaled down to 10 μm in diameter for example, the amount of thermal power to shift their resonance by 2π would the same 3.9 mW as was measured for a 200 μm ring It would translate to a proportionally scaled up value in the range of 0.1-0.2mw/nm. The work on smaller rings is currently in progress. They show similar trends in improved tuning with substrate undercut but complete scaling of their tuning performance continues to be evaluated and will be described in a publication to follow.

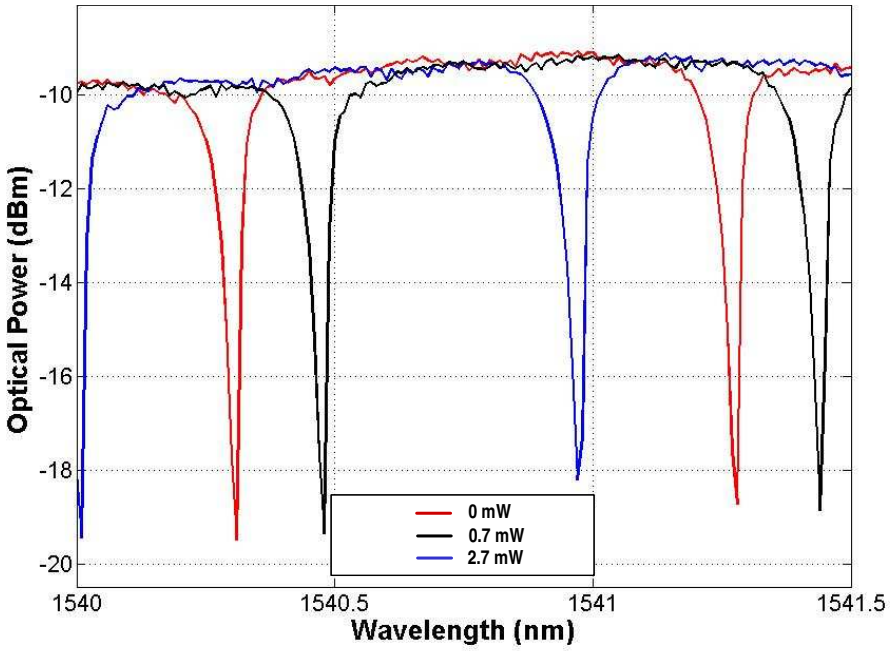

Fig. 6. Thermal tuning of the ring with a 100 μm radius.

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The response time for tuning a ring with removed undercut substrate was observed to slow down relative to the unetched devices. The time required to tune the device with locally etched substrate was observed to increase approximately three times compared to the unetched rings but still measured only several microseconds for a full 2π shift.

Furthermore, the ring's quality factor of Q = 9.6e4 remains unchanged after etching, at least to within the experimental resolution error. This implies that very little residual stress develops during the silicon handler removal process. Advantageously, due to the highly effective etch stop the internal stresses associated with non uniform and incomplete material removal can be alleviated in our fabrication approach. Otherwise these stress effects may cause strain induced inhomogeneity and local shape distortions in such a highly sensitive device with extremely high inherent Q.

The back-side etch pit can be expected to radically reduce tuning power because it disrupts heat flow spreading in the substrate of the device. This is supported by a simple analytic one-dimensional heat-flow analysis which also shows the thermal resistance of the device to decrease inversely with device diameter. A 20x reduction in the tuning has been experimentally verified and confirms expectations that thermal impedance has been drastically increased. When viewed with our simple model that scales the tuning with ring radius our result represents record performance compared with other results found in the literature [11].

5. Conclusion

We demonstrated spectral tunability of add-drop filters manufactured as ring resonators using commercial 130 nm SOI CMOS technology. Their thermal impedance has been dramatically increased by the selective removal of the SOI handler substrate under the device footprint by co-integration with bulk silicon micromachined structures. An overall ~20x increase in the tuning efficiency has been demonstrated with a post-processed 100 μm radius ring relative to its original performance with an intact substrate.

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