Sun Microsystems Laboratories

Title: **A FIFO Data Switch Design Experiment (Slides)**
Date: **23 March 1998**
Author: **Bill Coates**
SML #: **98-0141**

References

[1] SML #98-0014: *"A FIFO Data Switch Design Experiment"*, B. Coates et. al., 24 September 1997.

Summary

This document is a copy of a set of overhead transparency slides to be presented at the Async 98 conference in San Diego, CA on Monday, March 30, 1998. The referenced conference paper [1] has been previously cleared for external publication and the slides contain no new technical content.

Abstract of Talk

A core problem in many pipelined circuit designs is data-dependent data flow. We describe a methodology and a set of circuit modules to address this problem in the asynchronous domain. We call our methodology P**3, or "P cubed." Items flowing through a set of FIFO datapaths can be conditionally steered under the control of data carried by other FIFOs. We have used the P**3 methodology to design and implement a FIFO test chip that uses a data-dependent switch to delete marked data items conditionally. The circuit uses two on-chip FIFO rings as high-speed data sources. It was fabricated through MOSIS using their 0.6m CMOS design rules. The peak data switch throughput was measured to be a minimum of 580 million data items per second at nominal Vdd of 3.3V.

A FIFO Data Switch Design Experiment

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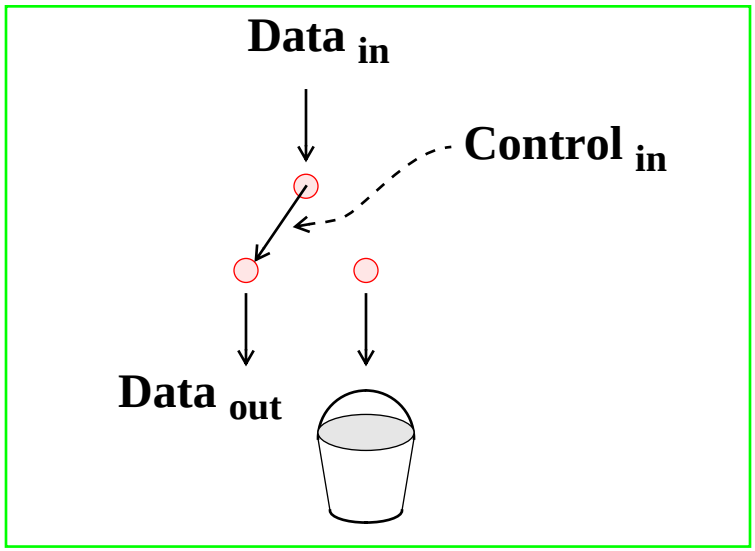
Presentation Outline

- **Background and Motivation**
- **Overview of the P**3 Methodology**
- **Design and Implementation of Experiment**
- **Measured results**
- **Conclusions and Ongoing Research**

Background and Motivation

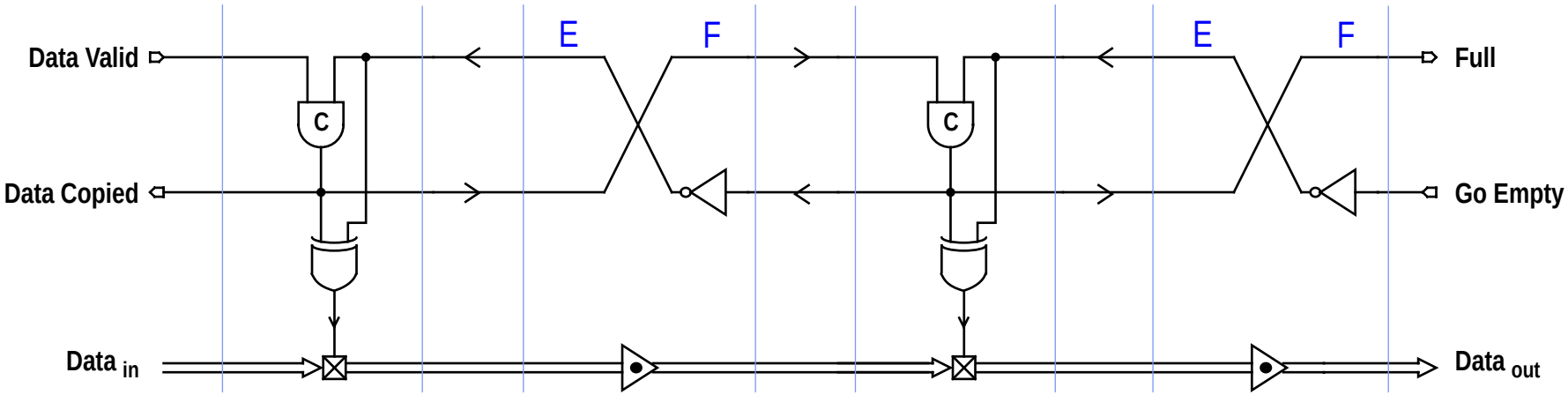
- **Impressive raw FIFO speeds**
  - **asP* control: ~ 1.0 GW/s (5 gate delays)**
  - **μPipeline control: ~ 1.5 GW/s (3 gate delays)**

  } **0.6μ MOSIS CMOS**
- **Next step:**
  - **Pipelines with data-dependent flow**
  - **Evaluation of P**3 design methodology**
- **Focus on core problem**
  - **FIFO with conditional drop**



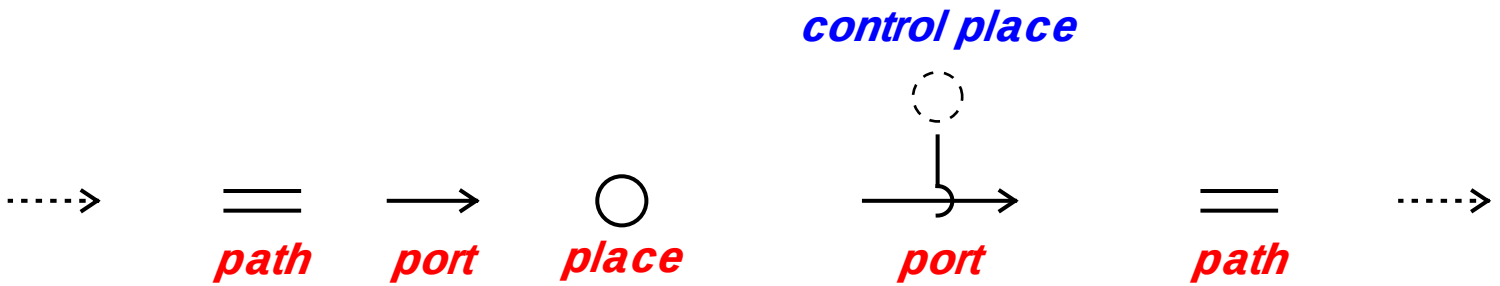
*The P**3 Methodology: An Overview*

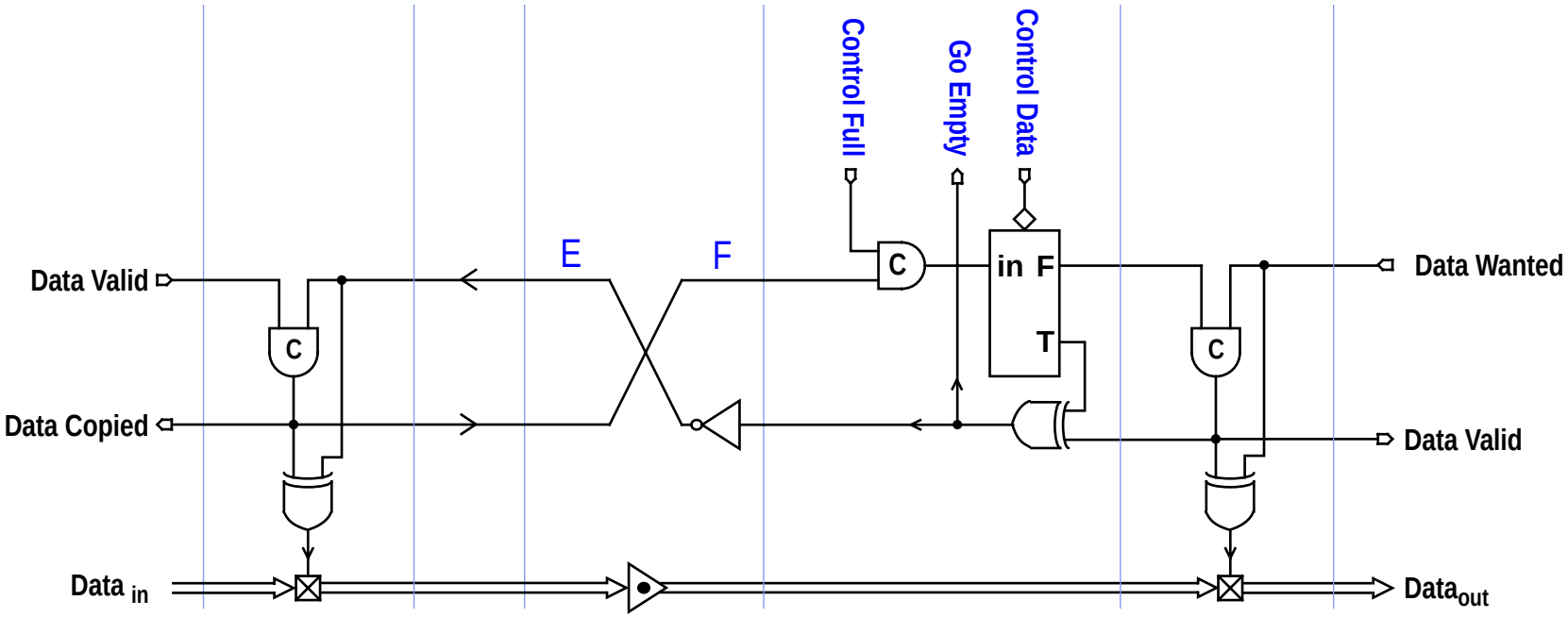
- **Three basic components:**
  - **Path**: *Data Transfer*
  - **Place**: *Data Storage*
  - **Port**: *Data Steering*
- **Example: Simple FIFO**



Controlled Ports: Conditional Movement

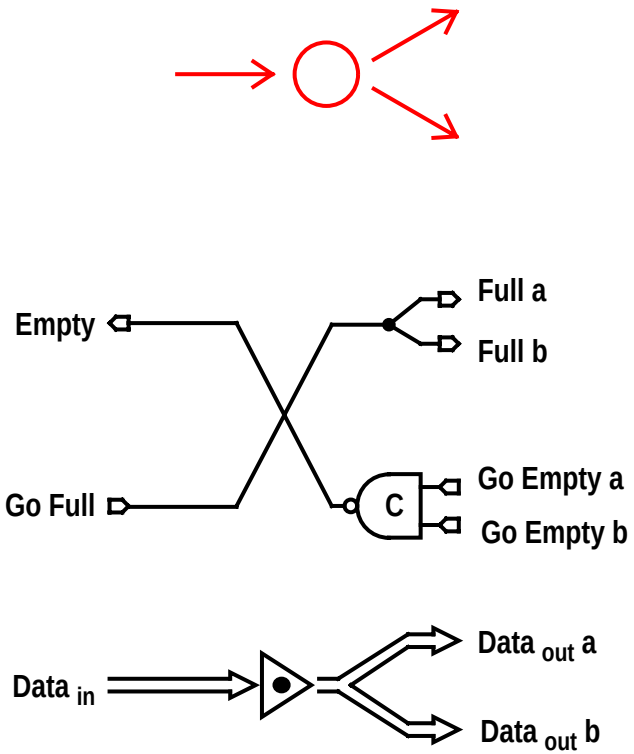
- **Control stream synchronized with data stream**



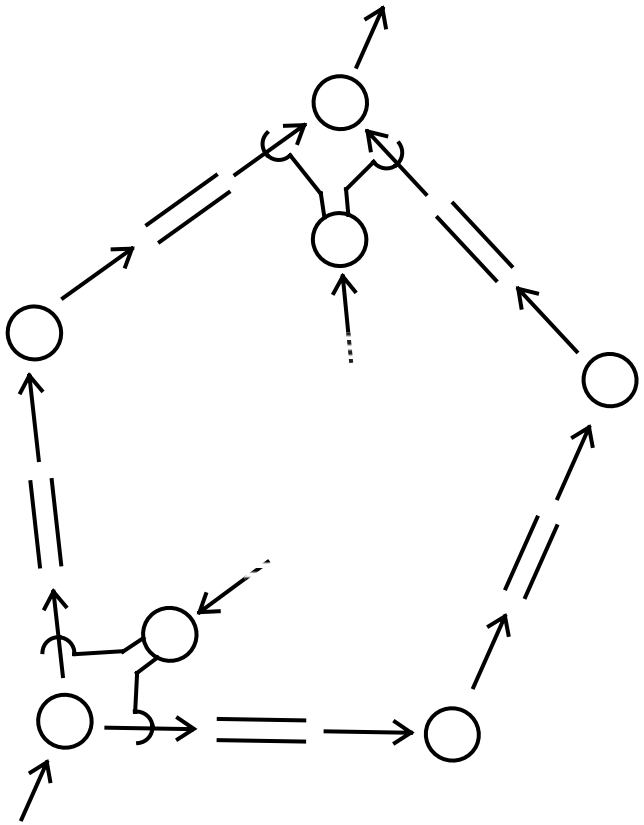


Pipeline Branching and Merging

Forking Place and symbol

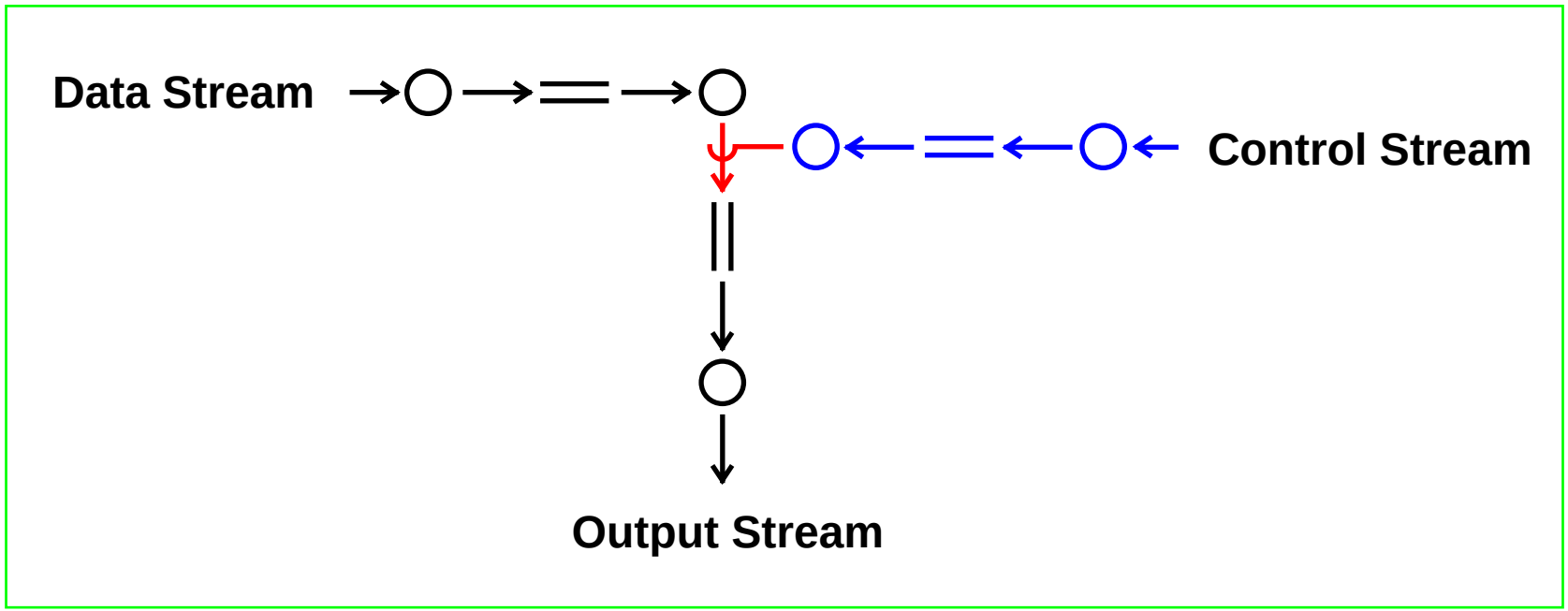


Controlled Data Flow



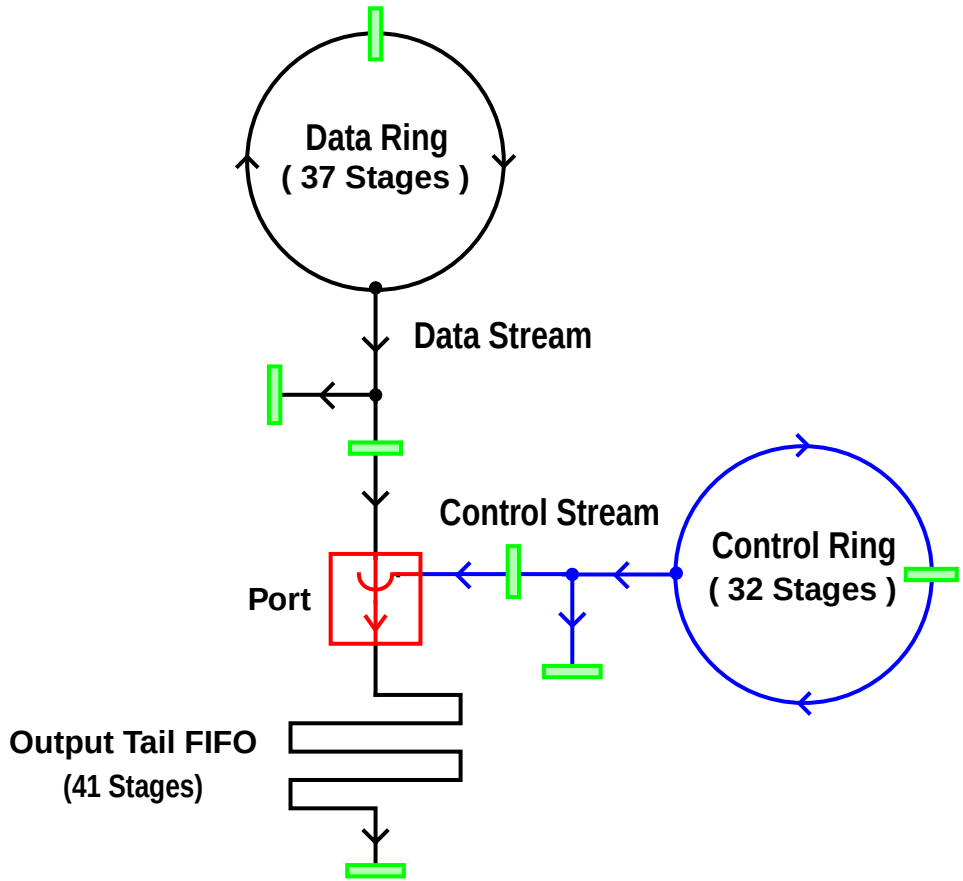
*P**3 Conditional Drop Configuration*

- **Exhibits desired core functionality**
- **Problem now is design of chip experiment**
  - **Control and observability issues**
  - **Circuit implementation details**

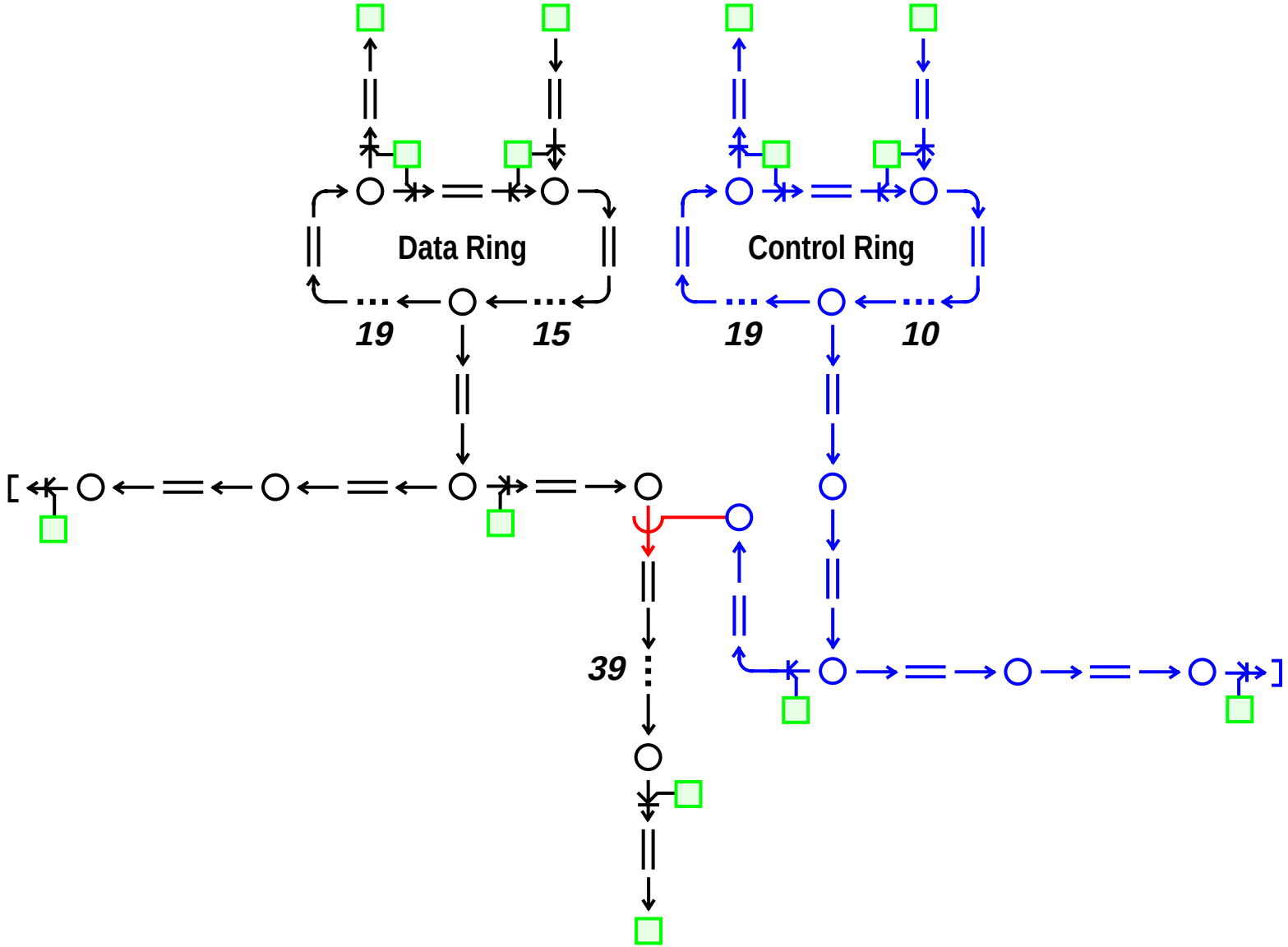


Two-Ring Chip: Experimental Design

- **On-chip FIFO rings used as high-speed data sources**
- **Long FIFO tail used to buffer result stream**



P**3 Experiment Specification



Simulation

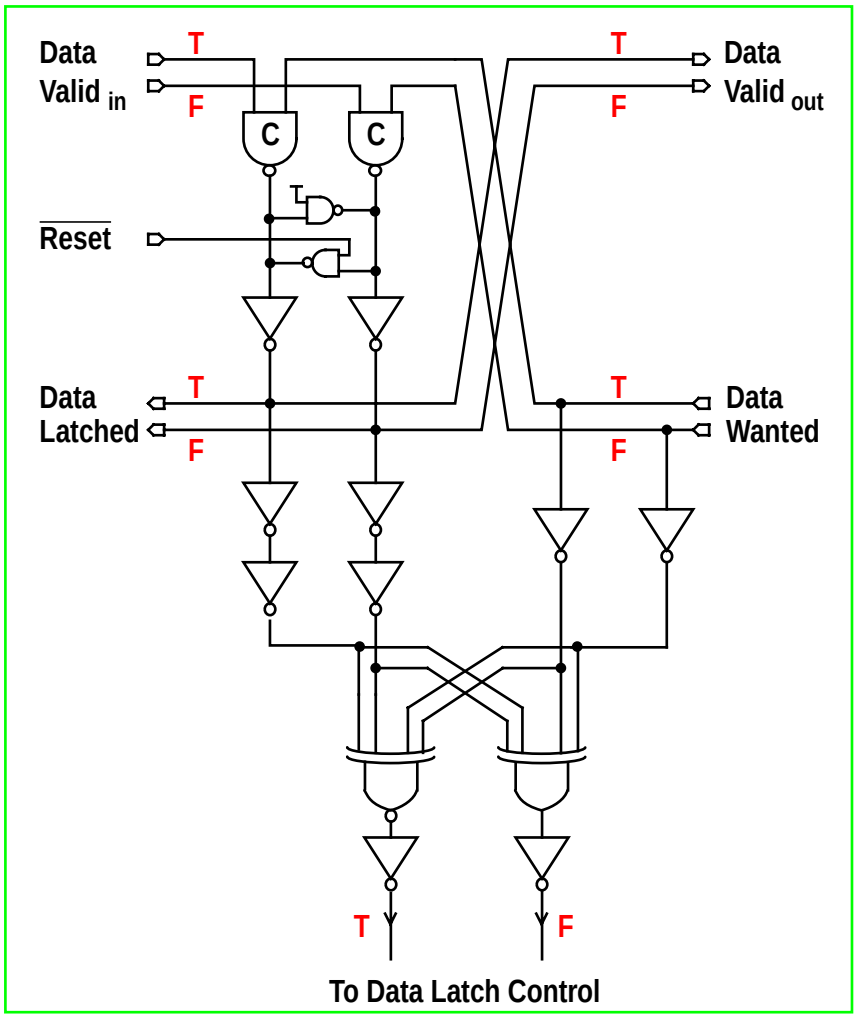
- C++ engine simulates P**3 structures
- Text description input, graphical back-end
- Spice circuit simulation for timing verification

Implementation

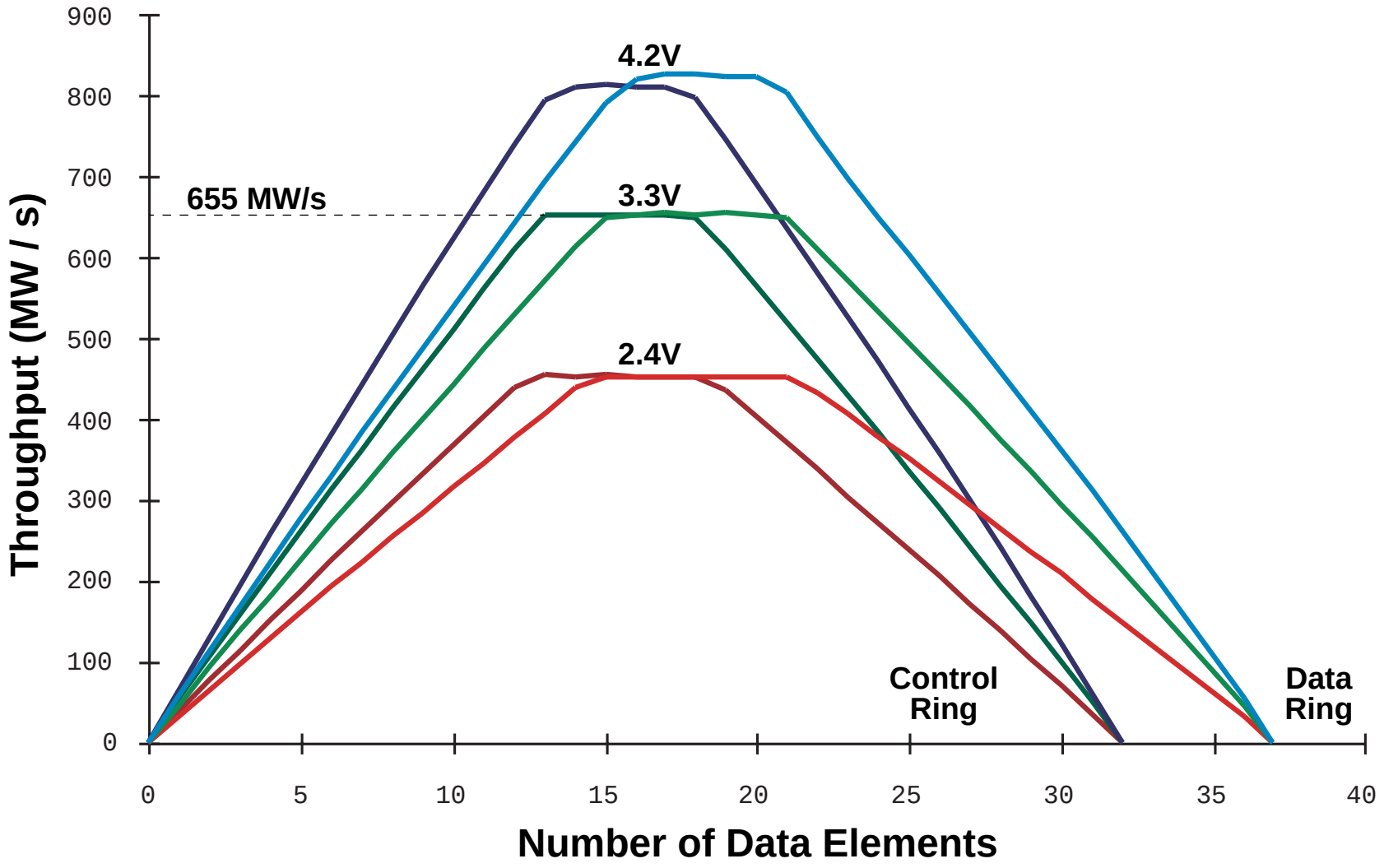
- Two-phase transition signalling
- Two complementary wires per control signal
- Standard cell based layout
- Test chips fabricated on two separate MOSIS runs

Circuit Implementation Detail

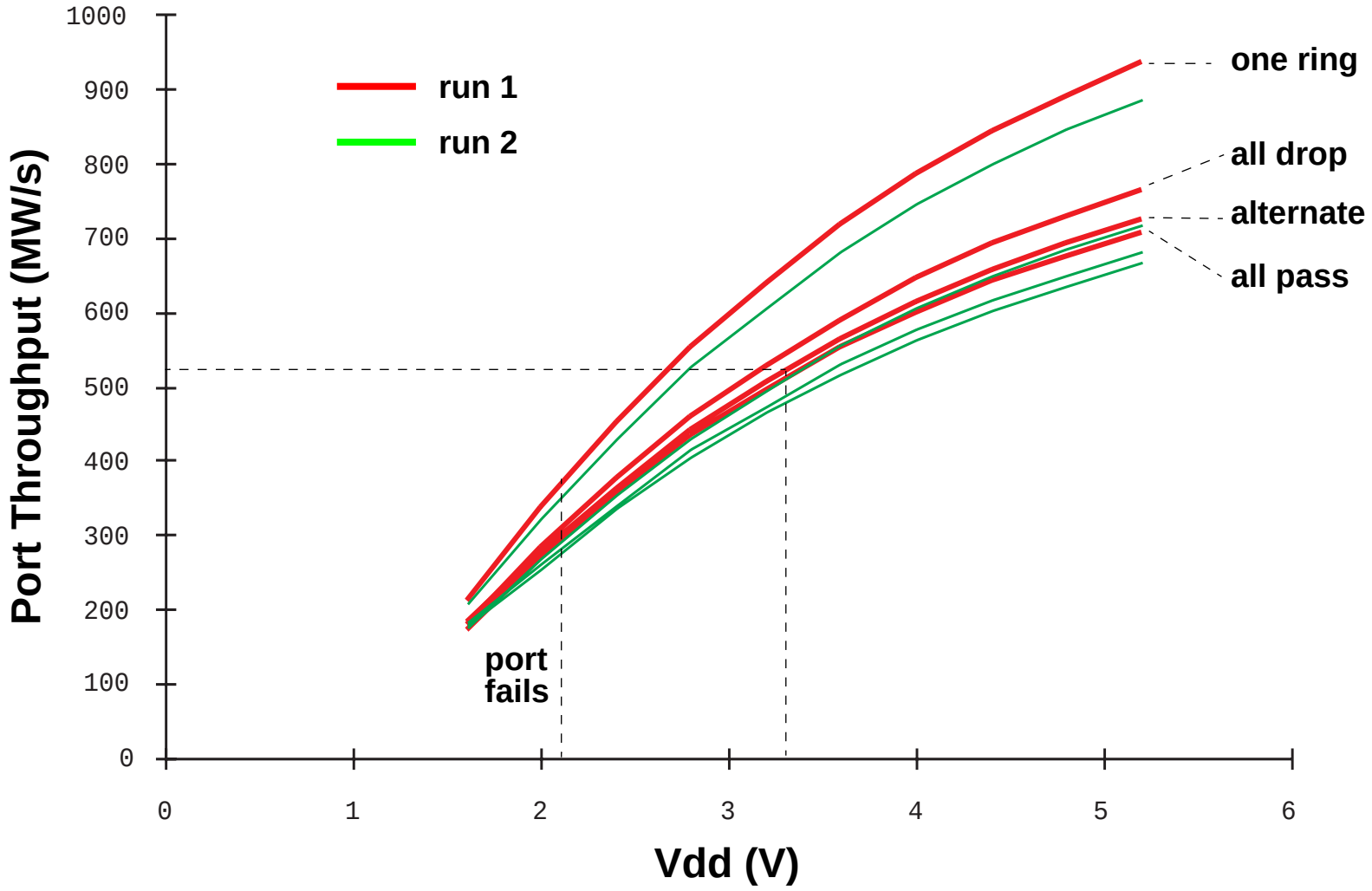
- **Example: standard Path component**



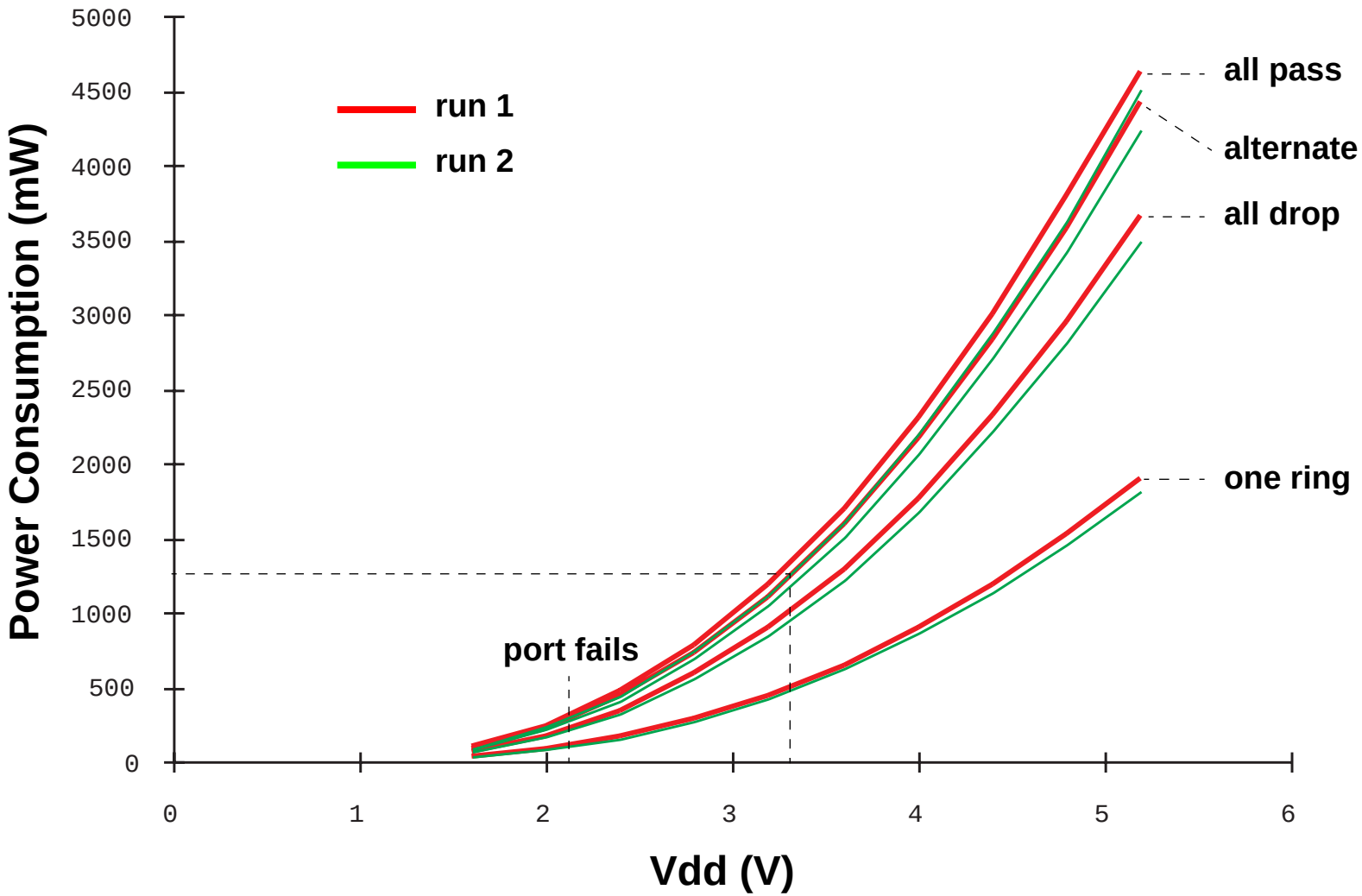
Ring Throughput vs Occupancy



Peak Port Throughput vs Supply Voltage



Peak Power Consumption vs Supply Voltage



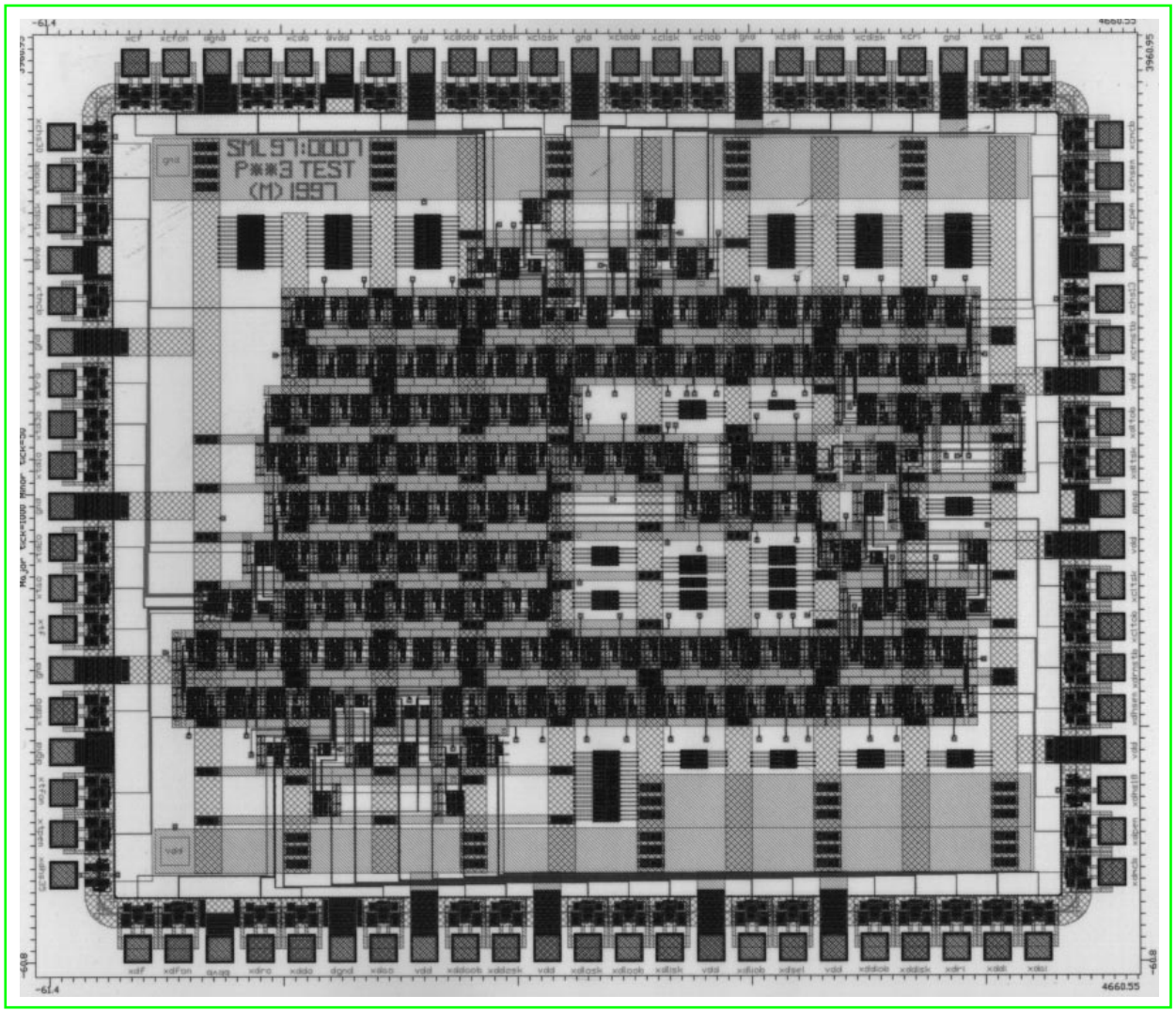
Conclusions

- **Methodology**
  - **Systematic design of a high-speed system**
  - **Useful shorthand notation for pipelined structures**
  - **Complexity still a problem**
- **Circuit Issues**
  - **Complementary transition signalling: fast but large area**
  - **Delay from long wires in standard cells**
- **Timing analysis**
  - **Critical to achieving high performance**
  - **Gate-and-Delay models inadequate**

Ongoing Research

- **Formal semantics for P**3**
- **Timing analysis**
- **Improved module implementations**
  - **Many layout and circuit optimizations are possible**
  - **Now believe that 1.0 GW/s is possible**
- **Design of more complex systems**
  - **Counterflow Pipeline test chip now in fab**

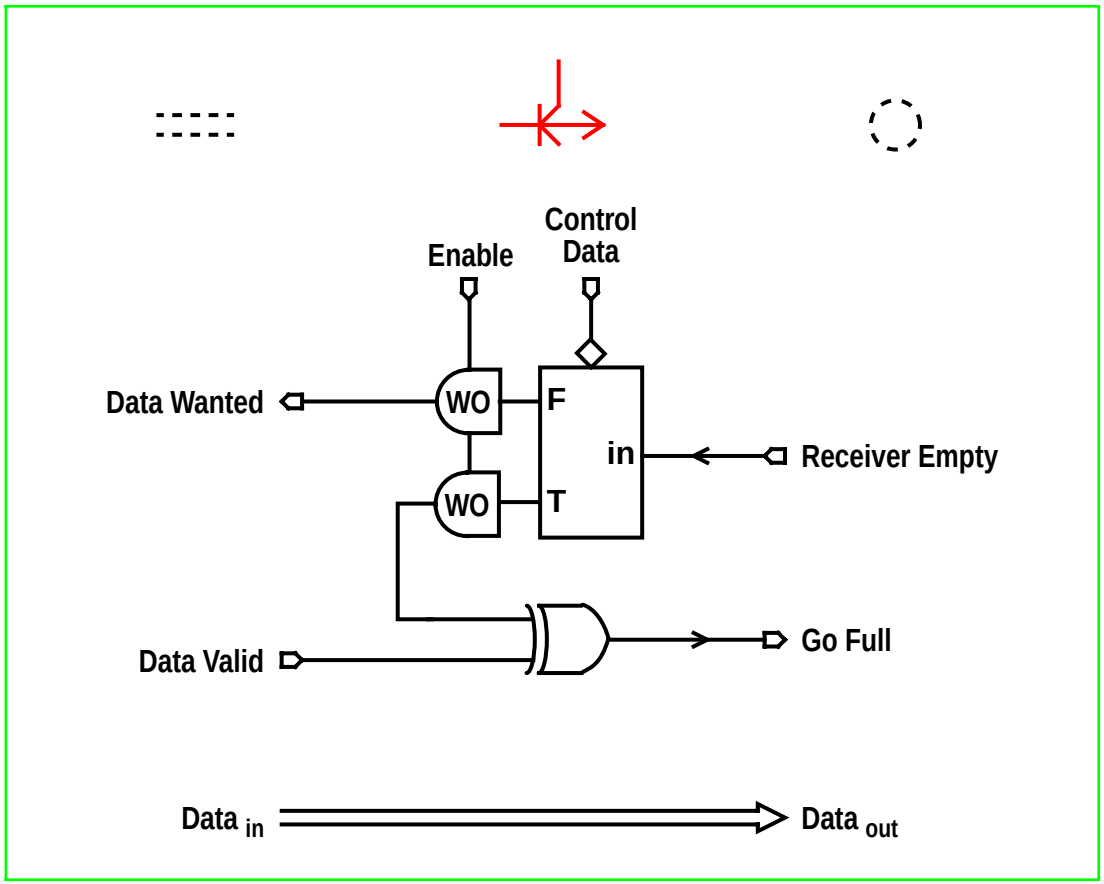
Chip Layout Plot



External Chip Interface

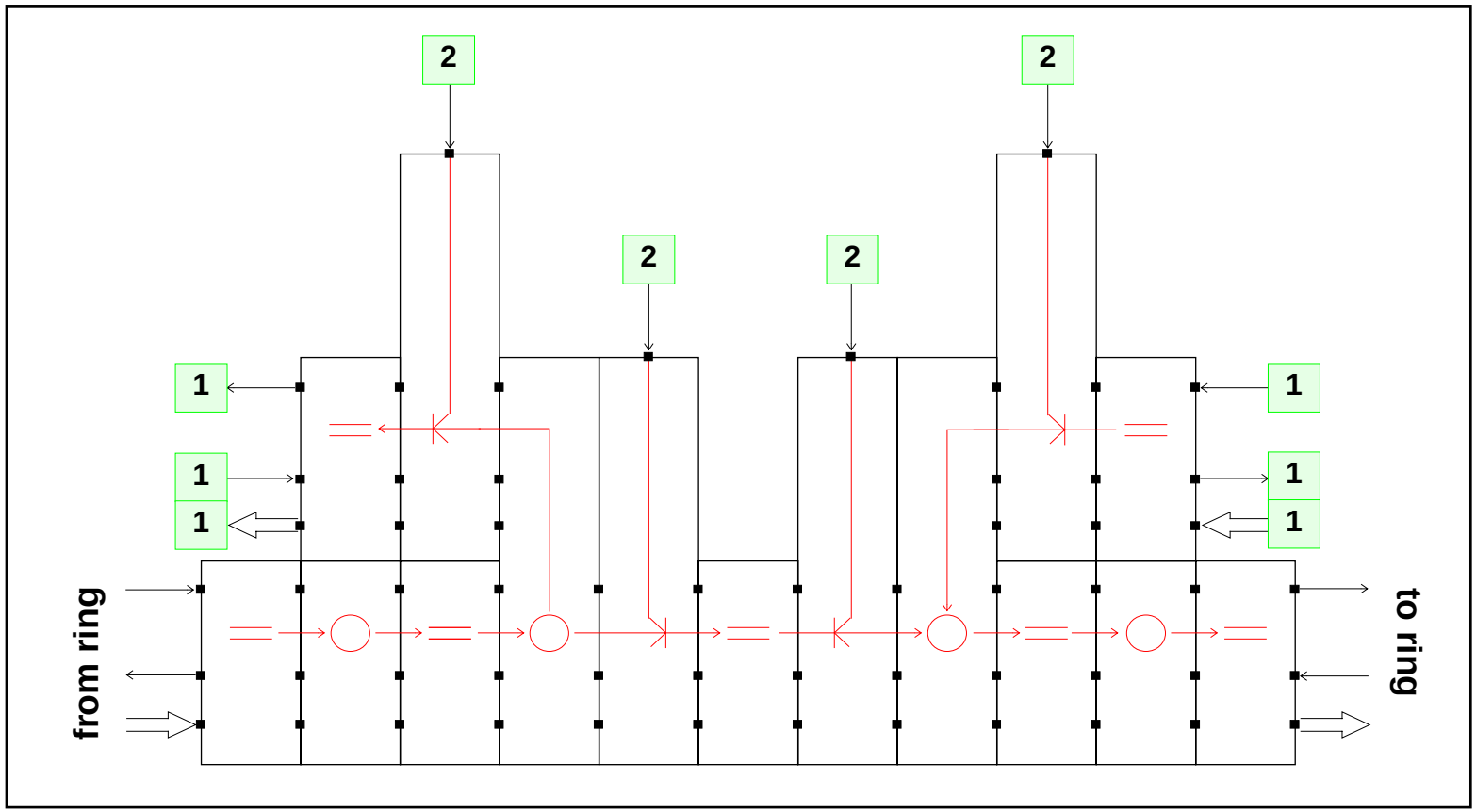
- **No high-speed handshake signals across chip boundary**

Observing Input Port and Symbol



Standard Cell Implementation

- **Example: Ring Interface**



Circuit Implementation Detail

- **Example: Output Port**