A sub-picojoule-per-bit CMOS photonic receiver for densely integrated systems

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Abstract: We report ultra-low-power (690fJ/bit) operation of an optical receiver consisting of a germanium-silicon waveguide detector intimately integrated with a receiver circuit and embedded in a clocked digital receiver. We show a wall-plug power efficiency of 690μW/Gbps for the photonic receiver made of a 130nm SOI CMOS Ge waveguide detector integrated to a 90nm Si CMOS receiver circuit. The hybrid CMOS photonic receiver achieved a sensitivity of −18.9dBm at 5Gbps for BER of 10^{-12}. Enabled by a unique low-overhead bias refresh scheme, the receiver operates without the need for DC balanced transmission. Small signal measurements of the CMOS Ge waveguide detector showed a 3dB bandwidth of 10GHz at 1V of reverse bias, indicating that further increases in transmission rate and reductions of energy-per-bit will be possible.

OCIS codes: (040.6040) Silicon detectors; (250.0250) Optoelectronics; (130.6622) Subsystems integration and techniques; (200.4650) Optical interconnects; (060.4510) Optical communications

References and links

1. A. V. Krishnamoorthy, R. Ho, X. Zheng, H. Schwetman, J. Lexau, P. Koka, G. Li, I. Shubin, and J. E. Cunningham, "Computing microsystems based on silicon photonic interconnects," Proc. IEEE **97**(7), 1337–1361 (2009).
2. D. A. B. Miller, "Device requirements for optical interconnects to Silicon chips," Proc. IEEE **97**(7), 1166–1185 (2009).
3. X. Zheng, J. Lexau, Y. Luo, H. Thacker, T. Pinguet, A. Mekis, G. Li, J. Shi, P. Amberg, N. Pinckney, K. Raj, R. Ho, J. E. Cunningham, and A. V. Krishnamoorthy, "An ultra-low power all CMOS Si photonic transmitter," in Frontiers in Optics, OSA Technical Digest (CD) (Optical Society of America, 2009), paper PDPB5, 2009.
4. G. Williams, "Wide dynamic range fiber optics receivers," *IEEE Solid State Circuits Conf.* pp. 80–81, February 1982.
5. D. Fraser Jr., G. Williams, R. Jindal, R. Kushner, B. Owen, "A single-chip NMOS preamplifier for optical fiber receivers," *IEEE Solid State Circuits Conf.* pp. 80–81, February 1983.
6. A. A. Abidi, "Gigahertz transresistance amplifiers in fine line NMOS," IEEE J. Solid-state Circuits **19**(6), 986–994 (1984).
7. A. V. Krishnamoorthy, A. L. Lentine, K. W. Goossen, J. A. Walker, and T. K. Woodward, J. E. Ford, G. F. Aplin, L. A. D'. Asaro, S. P. Hui, B. Tseng, R. Leibenguth, D. Kossivcs, D. Dahringer, L. M. F. Chirovsky, and D. A. B. Miller, "3-D intcgration of MQW modulators over active submicron CMOS circuits: 375 Mb/s transimpedance receiver transmitter circuit," IEEE Photon. Technol. Lett. **7**, 1288–1290 (1995).
8. O. Vendier, S. W. Bond, Myunghee Lee, Sungyung Jung, M. Brooke, N. M. Jokerst, and R. P. Leavitt, "Stacked silicon CMOS circuits with a 40Mb/s through-silicon optical interconnect," IEEE Photon. Technol. Lett. **10**(4), 606–608 (1998).
9. A. L. Lentine, K. W. Goossen, J. A. Walker, J. E. Cunningham, W. Y. Jan, T. K. Woodward, A. V. Krishnamoorthy, B. J. Tseng, S. P. Hui, R. E. Leibenguth, L. M. F. Chirovsky, R. A. Novotny, D. B. Buchholz, and R. L. Morrison, "Optoelectronic VLSI switching chip with greater than 1 Tbit/s potential optical I/O bandwidth," Electron. Lett. **33**(10), 894–895 (1997).
10. T. K. Woodward, and A. V. Krishnamoorthy, "Optical receivers for optoelectronic VLSI," IEEE J. Sel. Top. Quantum Electron. **5**(2), 146–156 (1996).

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11. D. H. Hartman, M. K. Grace, and C. R. Ryan, "A monolithic silicon photodetector/amplifier IC for fiber and integrated optics application," J. Lightwave Technol. **3**(4), 729–738 (1985).
12. P. J.-W. Lim, A. Y. C. Tzeng, H. L. Chuang, and S. A. St. Onge, "A 3.3 V monolithic photodetector/CMOS preamplifier for 531 Mb/s optical data link applications," in *Tech. Dig. 1993 Int. Solid State Circuits Conf. (ISSCC)*, pp. 96–97, 1993.
13. T. K. Woodward, and A. V. Krishnamoorthy, "1 Gb/s CMOS photoreceiver with integrated detector operating at 850 nm," Electron. Lett. **34**(12), 1252–1253 (1998).
14. C. L. Schow, J. D. Schaub, R. Li, J. Qi, and J. C. Campbell, "A 1-Gb/s monolithically integrated silicon NMOS optical receiver," IEEE J. Sel. Top. Quantum Electron. **4**(6), 1035–1039 (1998).
15. M. Ingels, and S. J. Steyaert, "A 1-Gb/s, 0.7- m CMOS Optical Receiver with Full Rail-to-Rail Output Swing," IEEE J. Solid-state Circuits **34**(7), 971–977 (1999).
16. A. Emami-Neyestanak, D. Liu, G. Keeler, N. Helman, and M. Horowitz, "A l.6Gb/s, 3 mW CMOS Receiver for Optical Communication," 2002 Symposium On VLSl Circuits Digest of Technical Papers, pp. 84–87, 2002.
17. D. Guckenberger, J. D. Schaub, D. Kucharski, and K. T. Kornegay, "A 1V, 10mW, 10Gb/s CMOS optical receiver front-end" Proc. IEEE Radio Frequency Int. Circuits Conf., pp. 309–312, June 2005.
18. G. Masini, G. Capellini, J. Witzens, and C. Gunn, "High-speed, monolithic CMOS receivers at 1550nm with Ge on Si waveguide photodetectors," Proc. LEOS (Institute of Electrical and Electronics Engineers, New York 2007), pp. 848–849, 2007.
19. C. Gunn, "CMOS Photonics for High-Speed Interconnects," IEEE Micro **26**(2), 58–66 (2006).
20. L. Chen, and M. Lipson, "Ultra-low capacitance and high speed germanium photodetectors on silicon," Opt. Express **17**(10), 7901–7906 (2009).
21. L. Vivien, J. Osmond, J.-M. Fedeli, D. Marris-Morini, P. Crozat, J.-F. Damlencourt, E. Cassan, Y. Lecunff, and S. Laval, "42 GHz p.i.n Germanium photodetector integrated in a silicon-on-inculator waveguide," Opt. Express **16**, 6252 (2008).
22. T. Pinguet, B. Analui, E. Balmater, D. Guckenberger, M. Harrison, R. Koumans, D. Kucharski, Y. Liang, G. Masini, A. Mekis, S. Mirsaidi, A. Narasimha, M. Peterson, D. Rines, V. Sadagopan, S. Sahni, T. J. Sleboda, D. Song, Y. Wang, B. Welch, J. Witzens, J. Yao, S. Abdalla, S. Gloeckner, and P. De Dobbelaere, "Monolithically Integrated High-Speed CMOS Photonic Transceivers," *Proceedings of IEEE conference on Group IV Photonics* (Institute of Electrical and Electronics Engineers, New York, 2008), pp.362–364, 2008.
23. R. Ho, J. Lexau, F. Liu, D. Patil, R. Hopkins, E. Alon, N. Pinckney, P. Amberg, X. Zheng, J. E. Cunningham, and A. V. Krishnamoorthy, "Circuits for silicon photonics on a 'macrochip', " IEEE Asian Solid-State Circuits Conference 2009, (to be published).

1. Introduction

The unique advantages of silicon photonics in terms of power, latency and bandwidth density can benefit integrated computing systems and permit the scaling of the bisection bandwidth of computing systems to unprecedented levels [1]. Limits on cost-effective heat removal at both the package and the system level make necessary very efficient photonic communication links (sub-pJ/bit) [2]. Among the key building blocks of a low power photonic link is an energy efficient optical transmitter integrated with a driver, and a receiver circuit integrated with a photodetector. Using low-parasitic micro-solder bumps, we have previously demonstrated an all-CMOS silicon photonic digital transmitter with a 400 fJ/bit energy efficiency [3]. Here we report on a 690 fJ/bit silicon photonic receiver that combines the benefits of an integrated CMOS waveguide detector and a fully integrated clocked CMOS receiver circuit with on-chip bias control.

MOSFET-based Trans-Impedance Amplifiers (TIAs) with active feedback have been investigated since the early 1980s for low-cost and low-area receivers [4–6]. Most early work was based on discrete detectors, but efforts to intimately flip-chip integrated III-V compound semiconductor detectors to CMOS TIAs with low parasitics was launched in the early 1990s [7–9], leading to receiver efficiencies of approximately 3 pJ per bit [10].

The use of Si MOS-compatible detectors has also been widely investigated and is appealing to system designers from the perspectives of cost, parasitic loading, high-speed operation, and integration with electronics for switching and computing. Early work in this area traded sensitivity for speed to compensate for the long absorption length in Silicon [11, 12], but even so, was eventually able to provide Gigabit speeds from standard silicon CMOS or Silicon-on-Insulator (SOI) foundry detectors monolithically integrated with TIA-based receivers [13, 14]. In [13] a monolithic CMOS receiver and Si detector demonstrated an energy efficiency as high as 1.5 pJ per bit at 1Gbps, but required external biasing of the TIA.

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Meanwhile, commercial-grade receivers with on-chip biasing and offset-correction were also built at Gigabit speeds but resulted in an order-of-magnitude larger energy-per-bit [15]. The use of DC-balanced input data, however, allowed novel, lower-power circuits to be explored. For instance, TIA-less CMOS receivers with energies less than 2 pJ/bit were recently demonstrated at 1.6 Gbps [16]. This result used a III-V flip-chip detector and an on-chip bias correction circuit and eliminated the need for external TIA biasing. In [17], the authors capacitively coupled a discrete PIN detector to a TIA to significantly reduce parasitic loading and simplify TIA biasing, albeit at a somewhat reduced sensitivity, to achieve a record energy efficiency of less than 1 pJ/bit at 10 Gbps.

More recently, evanescently-coupled waveguide-based Ge detectors have been incorporated into SOI CMOS [18, 19] to achieve the combined benefits of high-speed operation, good responsivity, and full CMOS integration. This approach has gained momentum and several groups have demonstrated Ge waveguide photo detectors with capacitances as low as a few fF [20], bandwidths above 40GHz [21], and excellent responsivity. Initial receiver work with such Ge waveguide detectors has focused on achieving high speed operation (10 Gbps and higher) [22], rather than energy-efficiency.

In this work, we present the first sub-pJ/bit operation of an all-CMOS photonic receiver by intimate integration of Ge photo detectors manufactured in a CMOS SOI photonic platform to a 90 nm bulk CMOS circuit. This work takes advantage of the integration of Ge detectors into Si waveguides, the intimate integration of detectors to receiver circuits, and novel circuit techniques that embed on-chip TIA bias and offset-correction at extremely low power [23]. The receiver circuit targets an integrated computing system with a distributed system clock, and is optimized with a unique architecture that employs fewer amplification stages and a special bias setting mechanism that does not require DC balanced data transmission, providing further energy savings from reduced coding overhead. The integrated receiver achieved sensitivity of −18.9 dBm (10^{-12} BER) at a data rate of 5 Gbps with a power consumption of 3.45 mW to achieve a record energy efficiency of 690 fJ/bit.

2. All CMOS photonic receiver

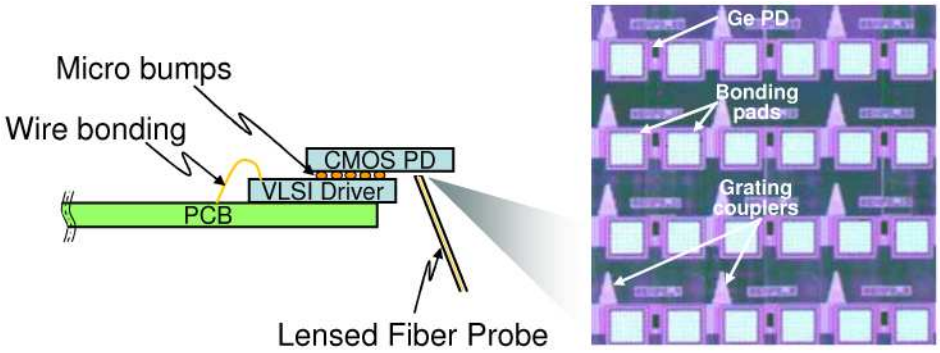

Fig. 1. Flip-chip integrated chip-on-board silicon photonic all CMOS receiver. The blow-up picture shows array of CMOS Ge waveguide detectors with grating couplers for optical coupling.

The integrated receiver used a chip-on-board package as depicted in Fig. 1. With a goal to achieve optimized overall energy efficiency, we used different CMOS platforms to make waveguide photo detector devices and the associated CMOS receiver circuit due to their different requirements on substrate and other parameters. A custom low parasitic micro-solder technology described in [1] was used to integrate the photonic device and the CMOS circuit chip to create a hybrid "CMOS photonic-bridge" configuration with an electrical interface for local communications and optical access for global interconnections via either fiber or waveguides on another routing layer. The hybrid receiver chip assembly was die-attached and

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wire-bonded to a printed circuit board (PCB). Such hybrid silicon CMOS receiver achieved a sensitivity of −18.9 dBm for data rate of 5 Gbps at a bit-error-rate of 10^{-12}. The integrated all-CMOS receiver has a record-low power consumption of below 700 fJ/bit. The details of the key building blocks of the receiver are discussed in the following sections.

2.1 CMOS Ge waveguide photo detector

Ge-PIN waveguide diodes with grating couplers for optical input were used in this work for high-speed signal detection [18]. They were fabricated with Luxtera's Ge-enabled optoelectronic process integrated in Freescale's HIP7_SOI 130 nm CMOS [22]. A picture of the detector array is in Fig. 1. The detector chip we used for this demonstration has size of 7×10mm, containing more than 49 Ge-PIN waveguide detectors and other test photonic devices. Characterization showed that the Ge waveguide photo detectors, similar to those used in the integrated receiver, had a high responsivity of 0.7 A/W at 1550 nm, a low dark current of 3 μA at 25C and 0.5 V reverse bias. At 1 V reverse bias, it had an extremely low capacitance of less than 20 fF, and a −3 dB bandwidth exceeding 10 GHz, as shown in Fig. 2. The exceptional quality of the Ge-PIN waveguide detector enabled high speed receiver designs with high sensitivity.

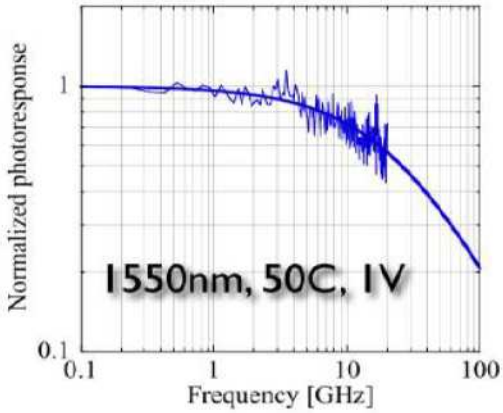

Fig. 2. Small signal frequency response of the CMOS Ge waveguide photo detector.

2.2 CMOS VLSI receiver chip

Optical receivers convert a modulated optical signal to an electrical digital signal, using photodetectors as a front end to receive optical signals as photo current. Typically a trans-impedance amplifier (TIA) converts the photocurrent signal into a voltage, and the voltage signal is then further amplified by multiple limiting amplifiers (LA) to a level that can be faithfully identified as either a logical "1" or "0" by the downstream digital circuits. Due to the optical loss of the link components and limited laser source power, the received optical signal power level is typically low, on the order of 10 μW, which translates to 10 μA of photo current with typical detector responsivity around 0.5~1 A/W. Converting this 10 μA current signal to a full-swing CMOS voltage requires an amplifier with large gain. For better energy efficiency, we used a low power receiver design with a 3-stage TIA, followed by a sense amplifier, as shown in Fig. 3 [23].

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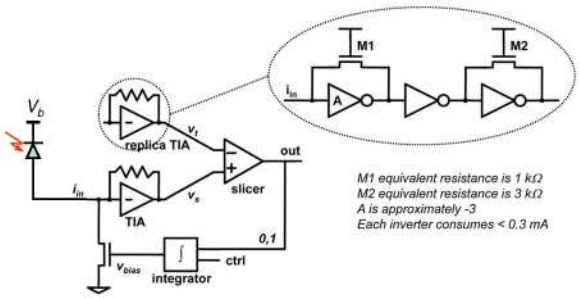

Fig. 3. Schematics of the receiver design. The TIA uses n-transistors in triode as feedback resistors. The integrator consists of an adder, two 8b registers storing calibration voltages, and an output DAC [23].

The 3-stage TIA gives a total gain of about 10k, giving a 100 mV output voltage for a 10 μA input signal. A simple and power-efficient clocked sense amplifier then subsequently amplifies the TIA output to a full-swing CMOS signal. To maximize the input amplifier's small signal gain, it was biased to give an average output of ½ Vdd, by shunting an appropriate amount of input current from the initial stage amplifier. Consequently, the sense amplifier was also biased at ½ Vdd by using a replica TIA. The transistor mismatch (about 10 mV(1σ) for 90 nm CMOS), residual thermal noise in the sense amplifier beyond transistor mismatch, and residual noise in the detector bias path limit the sensitivity of the receiver. The input referred noise current was calculated to be 1.1 μA.

Due to different link loss and imperfect extinction ratio of the modulators, the average signal level received by the photo detector varies from link to link. Even for the same link, due to ambient environment change and other impairments like component aging, the received signal power varies over time. The TIA bias, therefore, needs to be set differently for different channels and adjusted for each particular channel over time according the average signal power received. This is normally accomplished by using analog filters for feedback control, but unfortunately, analog feedback consumes significant power. In addition, it requires DC balanced data, which adds significant energy overhead to the total link power consumption: 25% in the case of 8B/10B DC-balanced coding. To minimize the overhead, we used a digital feedback scheme, as shown in Fig. 3, employing a globally-synchronized refresh operation to set the TIA bias correctly. Upon the initiation of global refresh, the bias control voltage is pre-discharged to 0 V, zeroing the bias shunt diversion current, and the transmitter sends a constant string of 0s. At the worst sensitivity and extinction ratio, this transmitted 0 will still be seen as a high input, and because the TIA has an inversion, sliced as a 0. Next, the integrator will gradually step up the bias voltage until the slicer generates a 1, at which point the TIA output will have just risen past ½ V_{dd}. This bias voltage is stored in an 8 b register. A similar process, based on pre-charging the bias voltage to V_{dd}, sending 1s, and gradually lowering the bias voltage, finds and stores the bias voltage that causes the TIA output to fall just past ½ V_{dd}. Finally, the integrator takes the mean of these two bias values to find a setting that forces the average of a 0 and a 1 to sit at the ½ V_{dd} threshold. (Note that if sending 1s, with the bias voltage pre-charged to V_{dd}, the slicer already evaluates to a 0, then the signal swing is very large and has large voltage margins, validating this threshold scheme.)

The advantage of this approach is that as long as the bias refresh is done periodically to overcome the signal power variation caused by ambient change and component aging, DC balanced data transmission is not required. Since ambient environment change and component aging are low frequency events, the refresh frequency can also be low, which makes it a very low overhead solution. For example, assuming we use 500 1s and 500 0s for calibration, it would take 100 nanoseconds at 10Gbps data rate. To follow kHz environment changes, we employ 10 refreshes every millisecond. The refresh overhead can then be calculated as

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100ns/0.1ms, or 0.1% equivalently. This approach, however, does require a global synchronization to avoid refresh request and acknowledgment between the transmitter and receiver, which would significantly reduce the useful link bandwidth. In a closely integrated micro-system (*e.g.* a macrochip [1]) where a globally shared clock source is available and phase errors between any two chips' clocks is bounded, we believe it is feasible.

Because the clock rate of computing systems is currently at 5 GHz or lower, we designed the photonic driver circuit for 5 Gbps operation to reuse the system clock and to avoid any serialization and de-serialization latency from clock gear-matching, although the detector itself has a much higher −3 dB bandwidth of 10 GHz (Fig. 2). In addition, the receiver chip was designed to interface with an external clock input and clocked digital output data buffer, and thus a clocked digital receiver with an on-chip clock distribution network was created to emulate a real system application. The VLSI receiver chip was fabricated in a commercial 90nm CMOS process with size of 5.5mm × 6mm, containing 87 receivers and other test circuits.

2.3 Flip-chip integration of hybrid CMOS receiver

The receiver and detector were integrated together using the same hybrid approach as described in [3]. The fabricated Ge photodetector chip and the VLSI chip were first processed to add under-bump-metallization (UBM) to the bonding pads using electroless plating. Low profile and small foot-print micro-solder bumps were added to the pads on the detector chip after UBM with a few microns of vertical compliance. Two post-processed chips were then integrated together using flip-chip bonding.

The hybrid chip assembly was die-attached and wire bonded to a test PCB for power, control and high speed digital I/O connections. A picture of the flip-chip bonded chip assembly is shown in Fig. 4a. The digital photonic receiver prototype is shown in Fig. 4b, with the CMOS VLSI receiver chip facing up and the CMOS SOI photonic detector chip facing down. Figure 4c shows a side view of the hybrid "CMOS photonic-bridge".

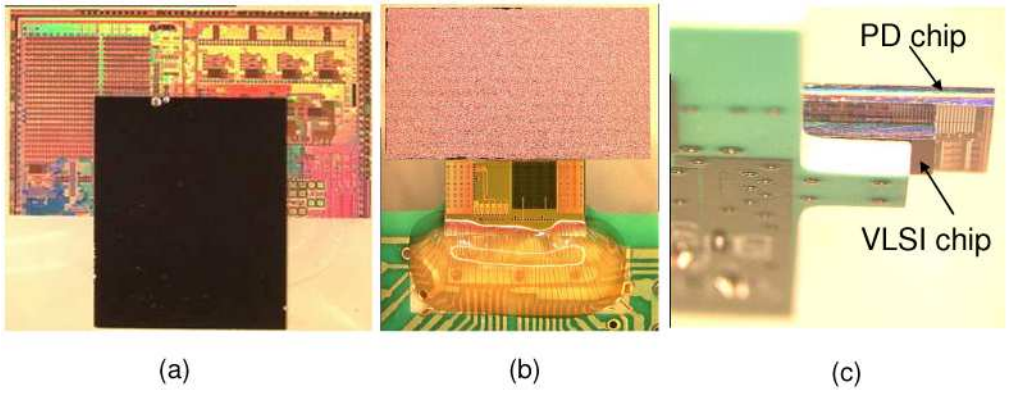

Fig. 4. Photo of the hybrid chip assembly, with VLSI receiver chip facing up . (b) is a photo of the integrated receiver, showing hybrid bonded VLSI receiver chip (facing up) and photodetector chip (facing down) wire bonded on a test PCB. (c) shows a side view of the hybrid "CMOS photonic-bridge".

3. Performance testing and results

The receiver was embedded in a test environment representative of a clocked digital link. We tested the integrated receiver performance with a commercial lightwave transmitter driven by 2^{31}-1 PRBS data from a pattern generator at 5 Gbps. The modulated optical signal has an extinction ratio (ER) better than 10 dB. A lensed fiber was used to couple the light signal to the waveguide Ge detectors through grating couplers. A high speed external clock was fed to the chip, aligned with the input data at the sense amplifier, and used to clock the digital data

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out through the high speed buffers after the receiver. I/O pads then translated the full-logic-swing 5 Gbps signals to CML signals to drive the data off chip. These high speed signals passed through short wire-bonds from the CMOS receiver chip to a test PCB (shown in Fig. 4 c) first, and then traveled over several inches of trace leading up to a flex connector. Through a flex cable, and additional traces after the connector on a second test board (not shown), the data signals were received finally by an error detector on a BER tester through high quality RF cables for performance characterization.

With a modulated optical signal at 18 μA average photo current (equivalent to an optical power of −16 dBm for detector responsivity of 0.7 A/W), we obtained error free operation for more than 6 hours, indicating a BER better than 10^{-14}. The mechanical drift of the actuators we used to manipulate the fiber probe made it very difficult for longer term BER measurement. Instead, we measured the receiver BER for different average input power levels. The plot in Fig. 5 shows the measurement results, indicating a receiver sensitivity of about −18.9 dBm for a BER of 10^{-12}. With 0.7 A/W detector responsivity, an −18.9 dBm optical signal would generate 9 μA average photo current. Assuming similar Gaussian noise for both "1s" and "0s", the corresponding input referred noise level is estimated at about 1.3μA (1σ). This agrees almost exactly with our analysis employing foundry-provided transistor channel noise models, in which the transimpedance amplifier's output noise was simulated in Spice, divided by the gain of the amplifier, and combined with the input's kT/C noise.

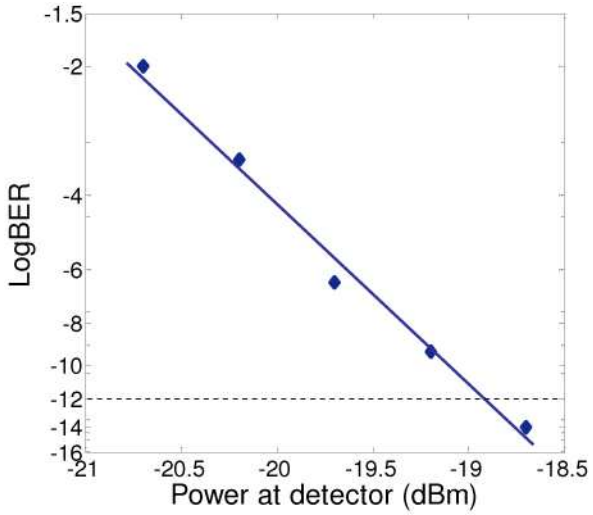

Fig. 5. Receiver sensitivity measurement results.

We then measured the receiver amplitude and timing margin using an input optical signal with an average power of −18.9 dBm by shifting the phase of the clock relative the input data signal at the sense amplifier. The result is plotted as inverse error function Q versus the sampling offset, as shown in Fig. 6. Using Dural Dirac jitter model, we obtained the estimated deterministic jitter (DJ) of about 63 ps, and random jitter (RJ) of about 14 ps (rms).

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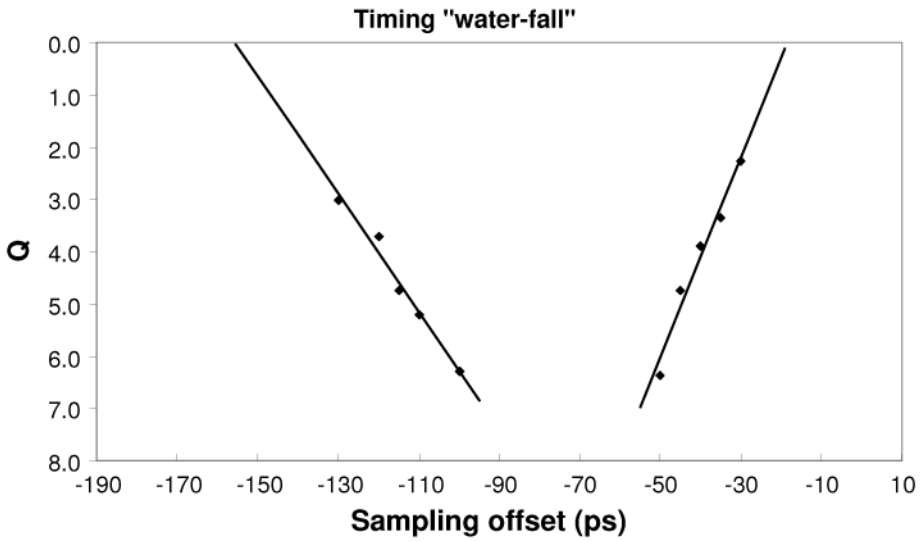

Fig. 6. Receiver timing margin measurement results.

We directly measured a total receiver power consumption of 3.45 mW (excluding the power consumed by the digital data buffers, and the on-chip clock distribution) during extended operation by measuring the supply voltages and currents. This corresponds to a receiver energy of 690 fJ/bit and represents the entire power of the photo detector and its CMOS receiver, as well as any excess power required to drive circuit parasitics including internal wiring and flip-chip pads.

4. Conclusions

We have demonstrated for the first time a sub-picojoule per bit, hybrid integrated, all-CMOS photonic receiver using a Ge waveguide detector and 90 nm CMOS receiver circuits. The integrated receiver employed a 3-stage TIA followed by a low power clocked sense amplifier, and was embedded in a digital system with digital data/clock interface and on-chip clock distribution. It achieved a sensitivity of −18.9 dBm at 5 Gbps for a BER of 10^{-12} with an ultra-low power consumption directly measured below 700 fJ/bit. To our knowledge, this is the lowest energy/bit (power/bit-rate) receiver in any technology. Unlike conventional optical receivers, DC balanced data transmission is not required for the receiver to work properly. This is enabled by a low-overhead temporal bias refresh scheme. This successful demonstration of a low energy silicon photonic receiver marks another significant step towards a complete sub-pJ/bit link that is expected to be critical for future inter-chip and intra-chip interconnect applications.

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