Electric™, a VLSI CAD framework using the Java Technology

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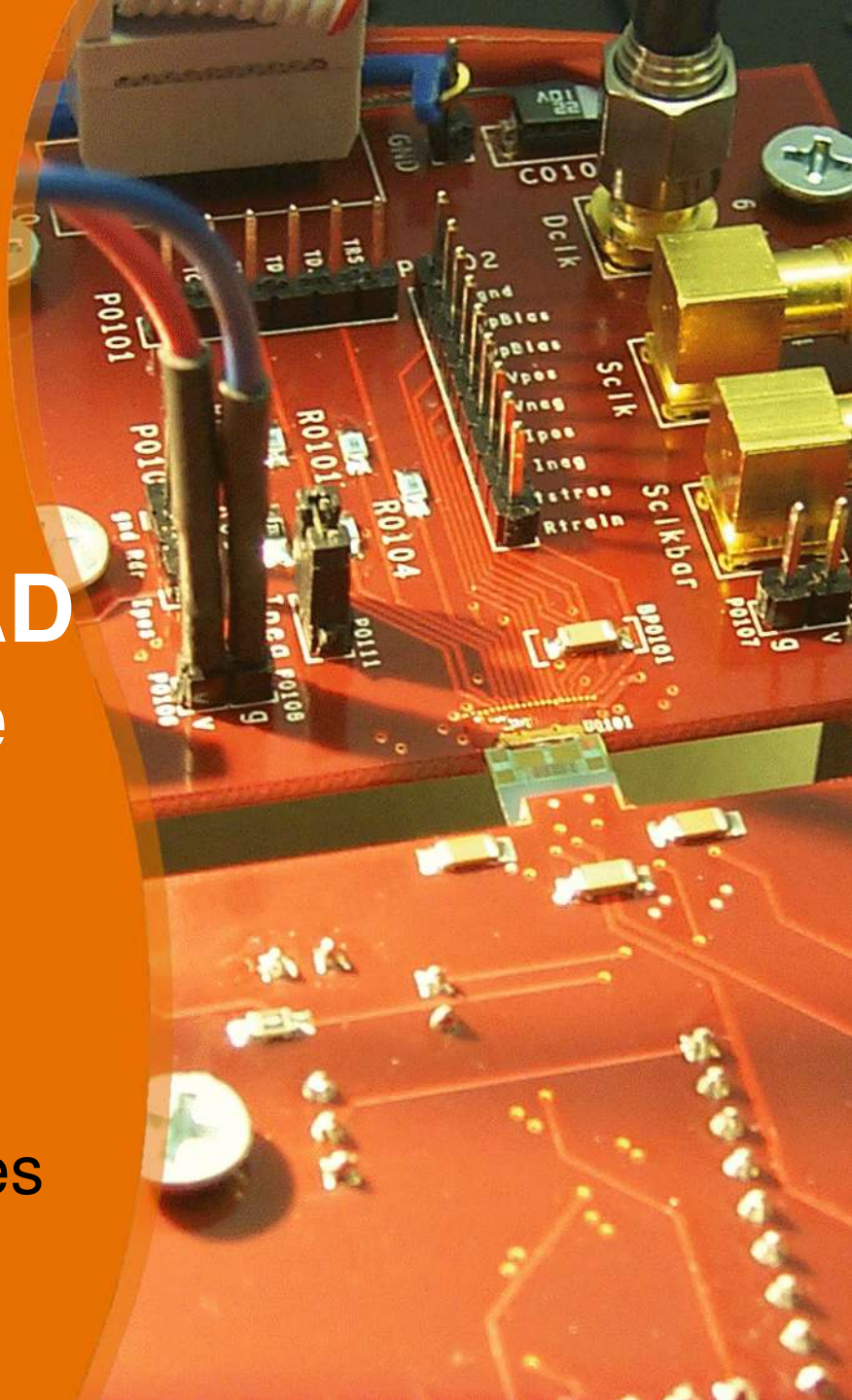


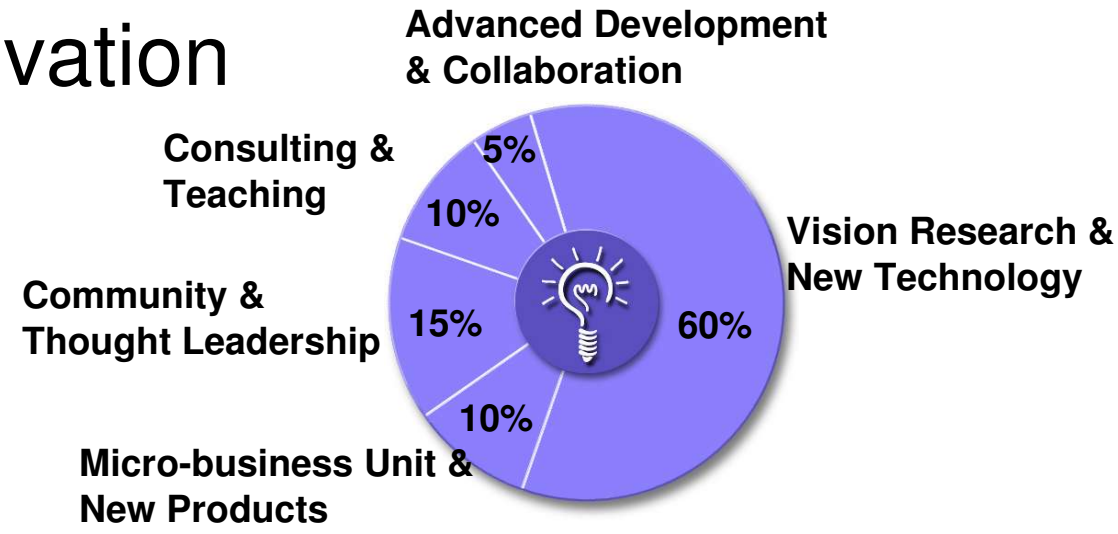
Outline

- Sun Labs and Asynchronous Group 
- VLSI design workflow
- Electric framework 
- Java framework 

- What is next
- Summary
- Q&A

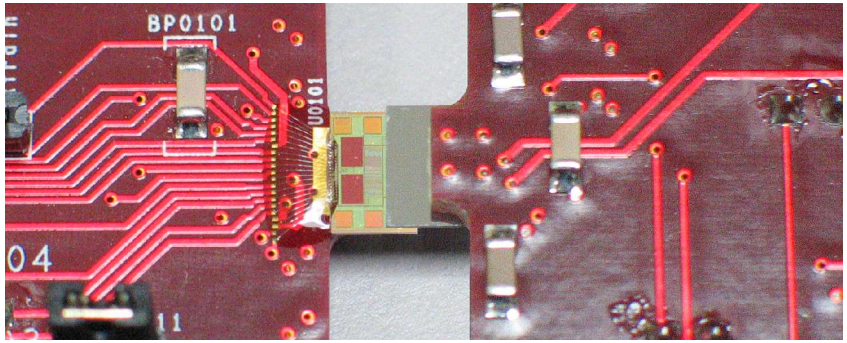
Sun Microsystems Laboratories

- Center for innovation
  - > Project focus
  - > What we do



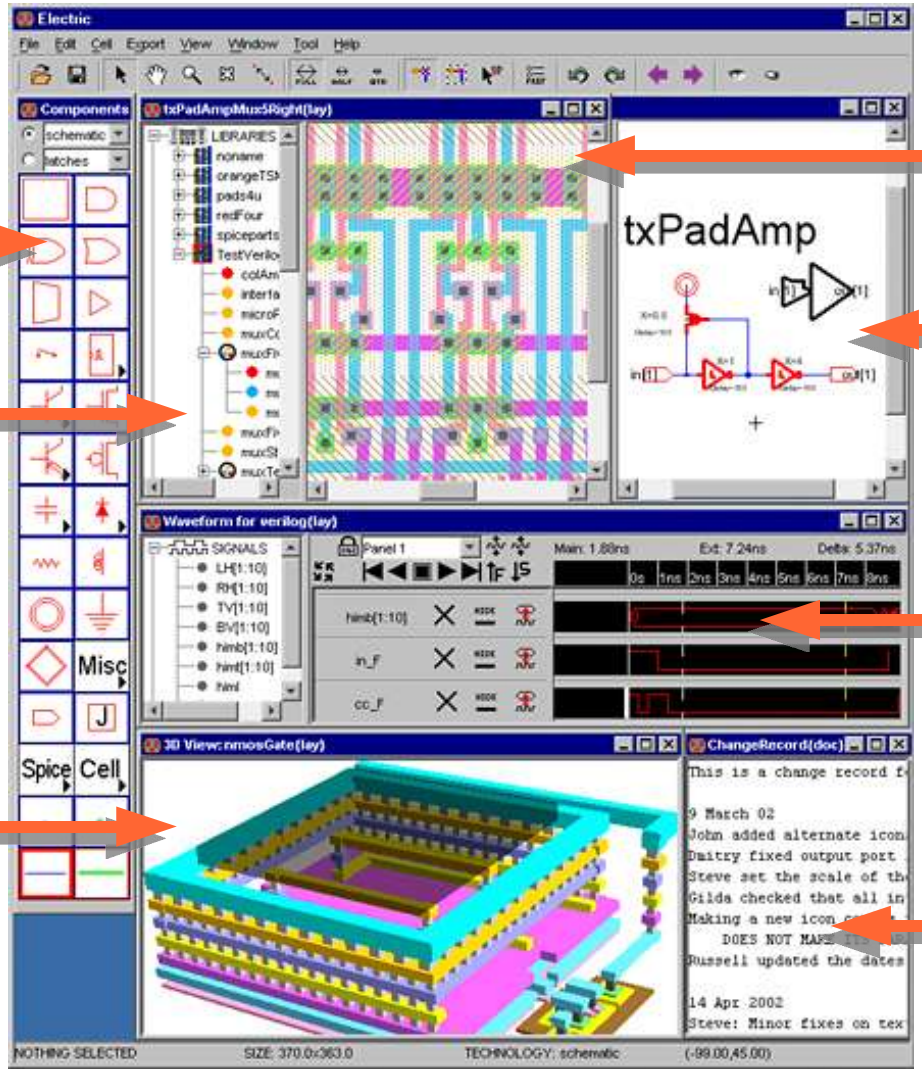
- Technology transfer leadership
  - > Java, Sun Ray, JFluid, Electric, Proximity I/O

Asynchronous Group



- Asynchronous design
  - Clockless systems
- Major benefits
  - Faster speeds, lower power consumption, more architectural freedom
- Major contributions
  - UltraSPARCIIIi, GasP, FLEET, Proximity Communication

Electric: VLSI Framework



Palette

Explorer Tree

3D View

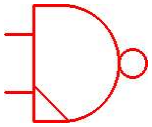
IC Layout

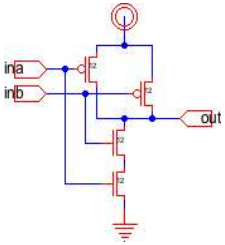
Schematic

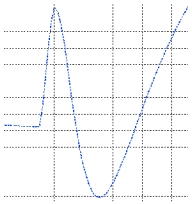
Waveforms
Simulation

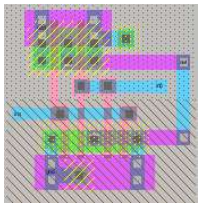
Documentation

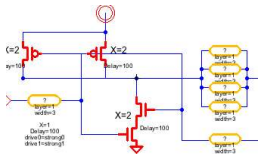
VLSI Design Workflow

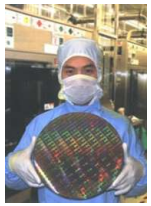


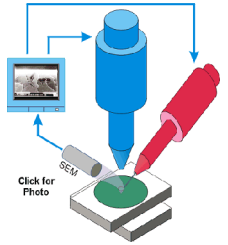








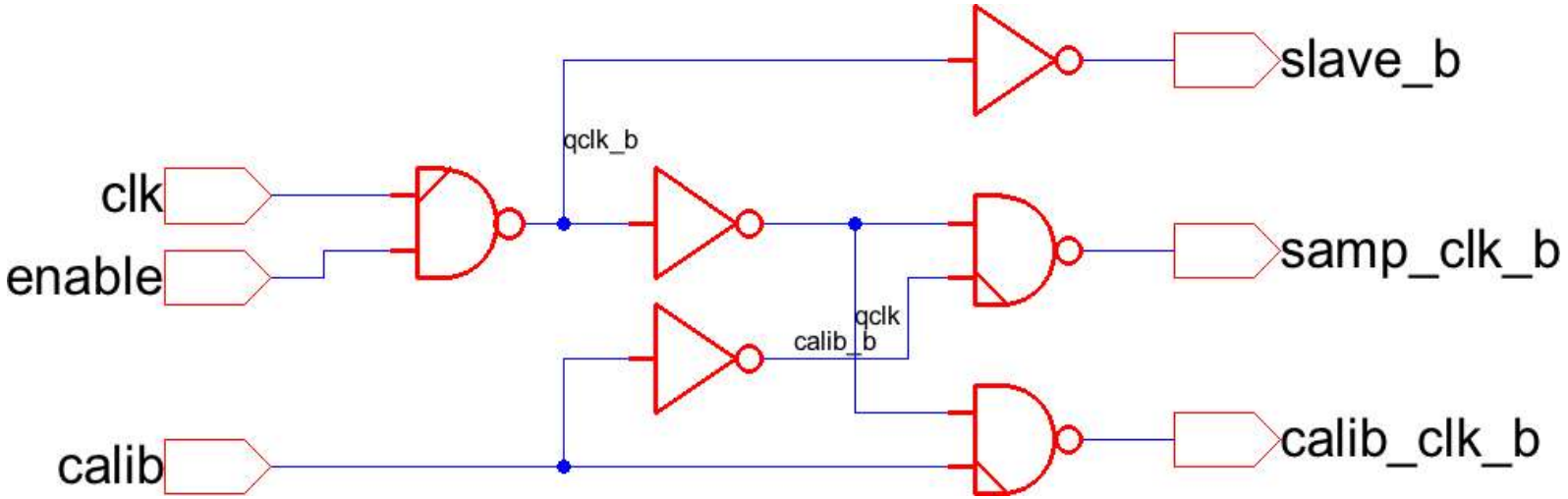


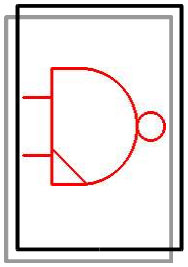
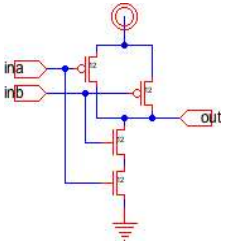


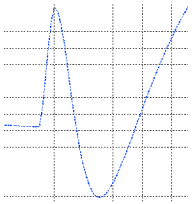
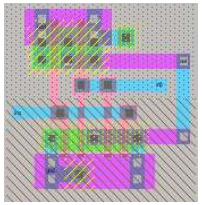
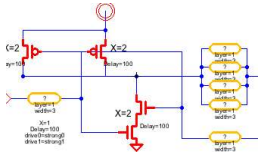
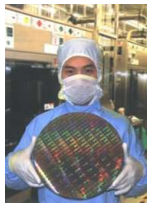
Courtesy of Tom O'Neill, Async Group

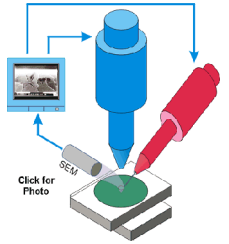
VLSI Design Workflow

- Circuit design in Electric



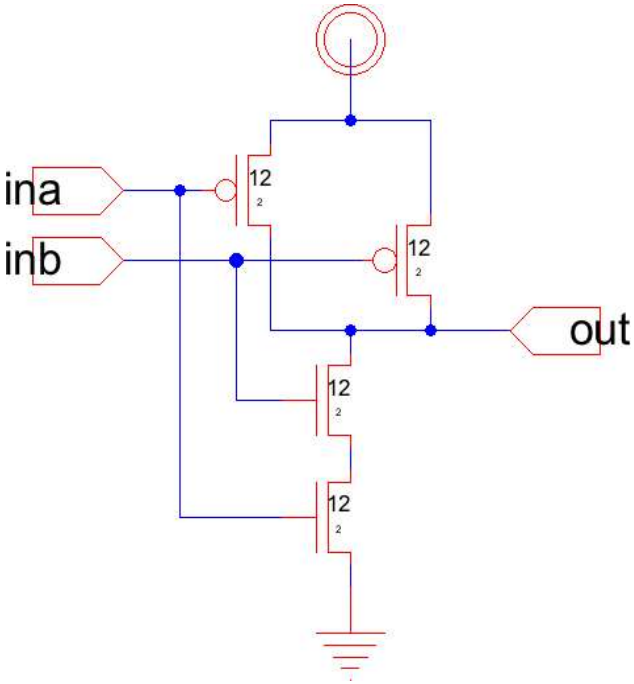



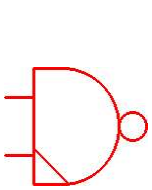





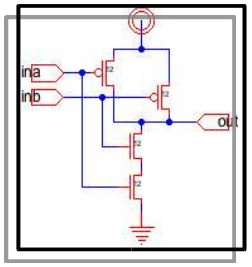


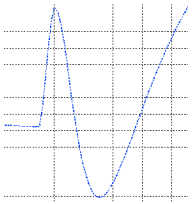
VLSI Design Workflow

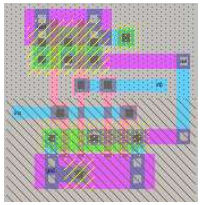
- Transistor sizing in Electric
  - > Transistor sizes determine speed, power
  - > Logical effort theory => sizes

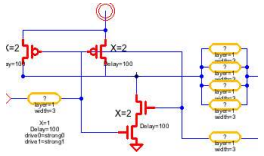


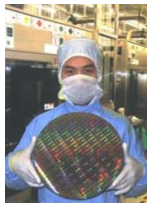


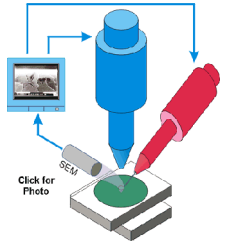






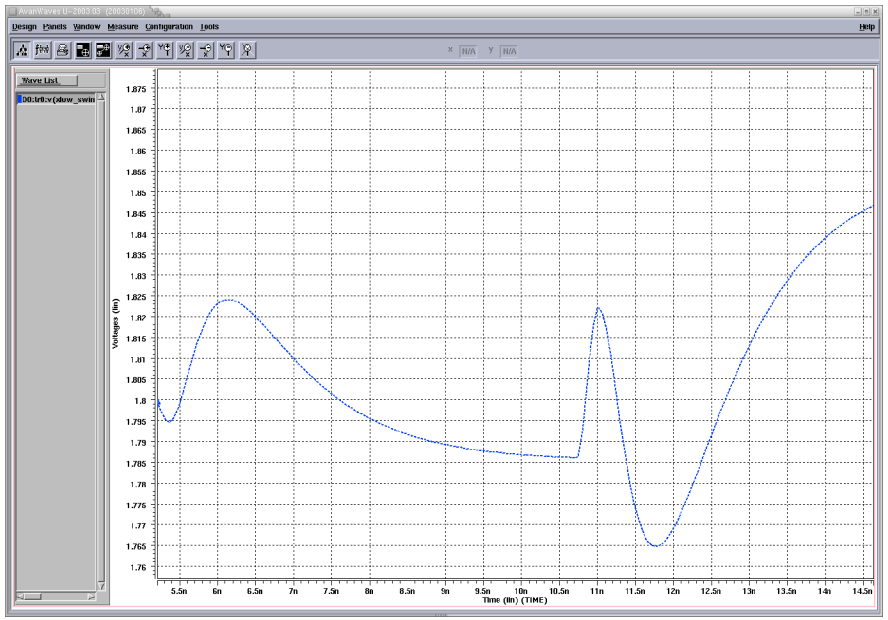


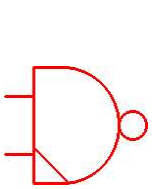


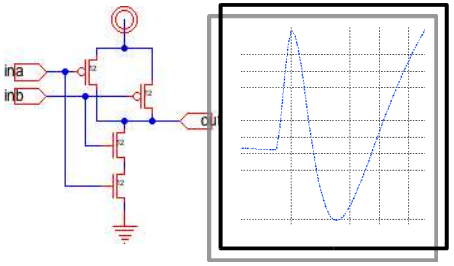


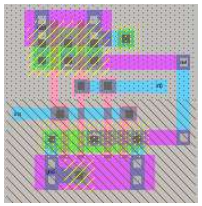
VLSI Design Workflow

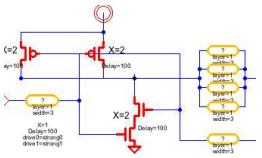
- Simulation
  - > IRSIM in Electric
- Netlist generation
  - > SPICE, others
- Textual Languages
  - > VHDL, Verilog

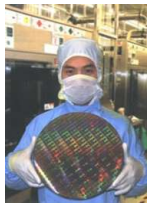


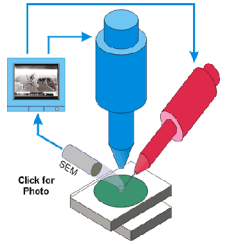












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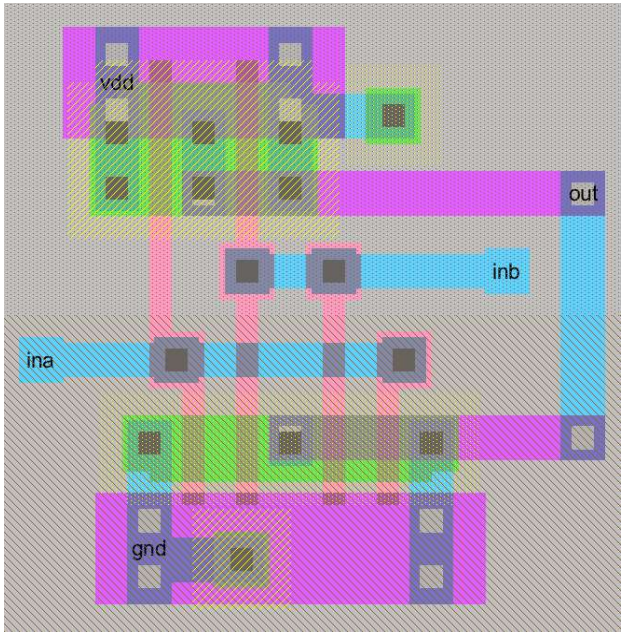
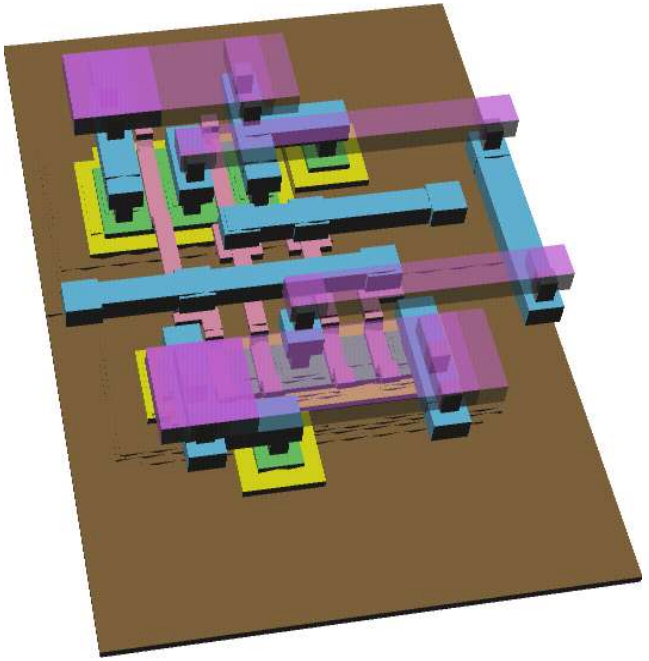
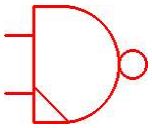
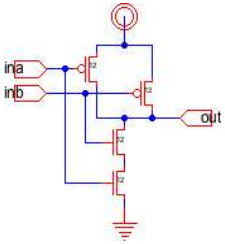
VLSI Design Workflow

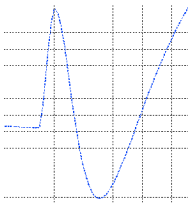
- Layout in Electric

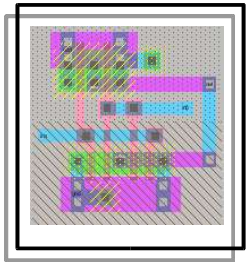


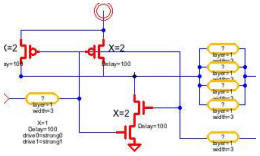


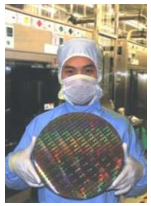


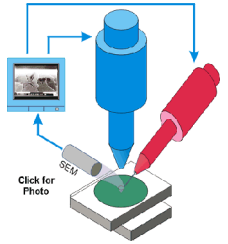






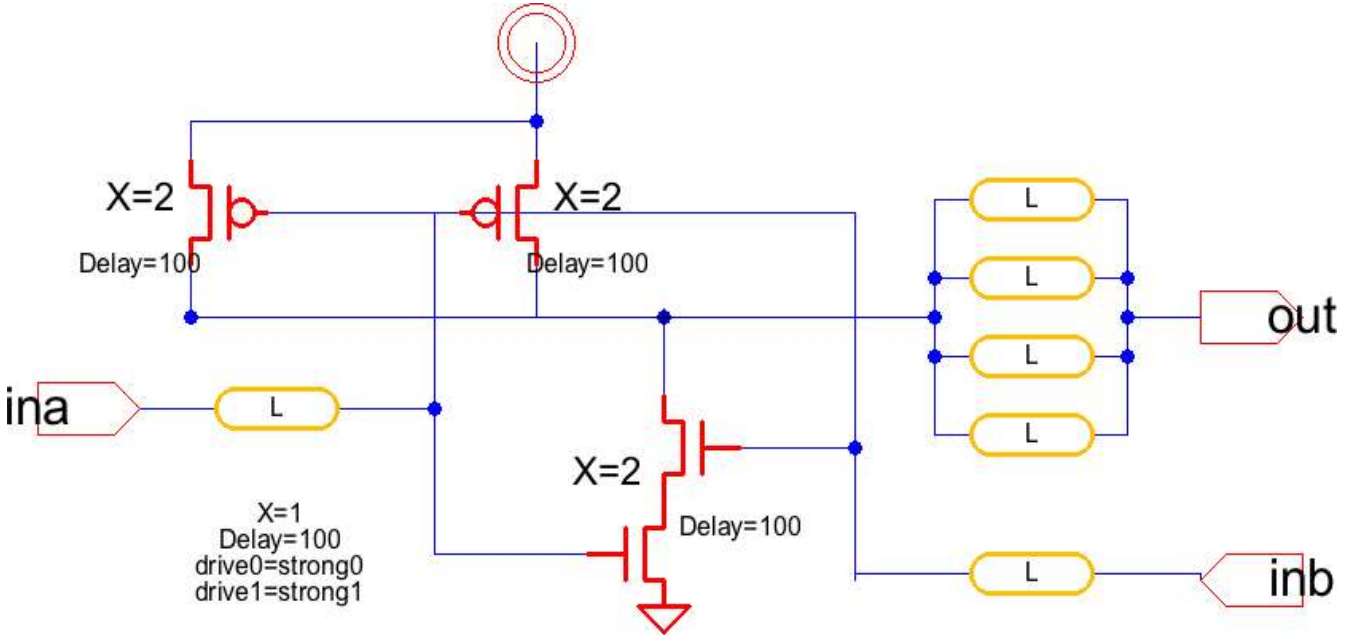


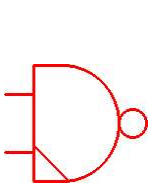


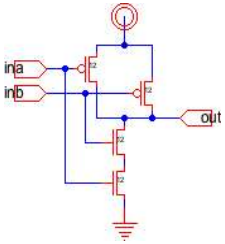


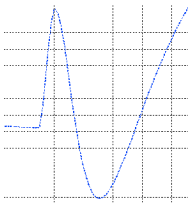
VLSI Design Workflow

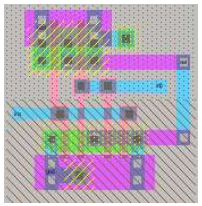
- DRC, NCC, Annotation in Electric

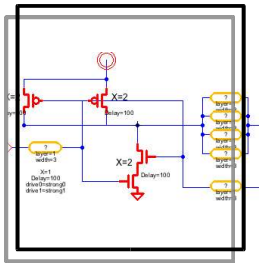


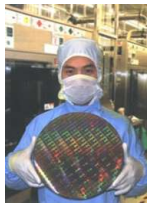


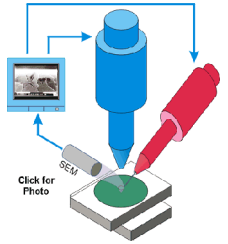






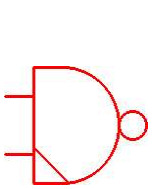


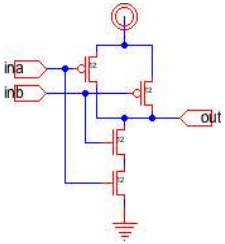


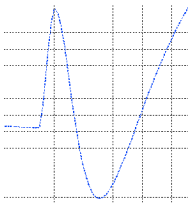


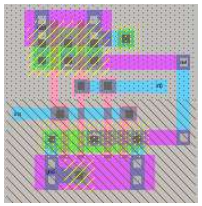
VLSI Design Workflow

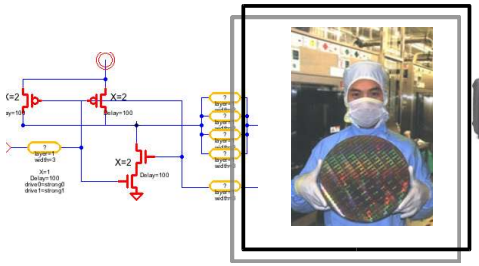
- Chip fabrication

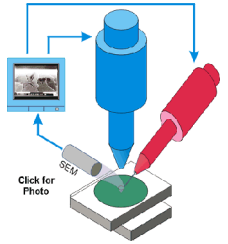












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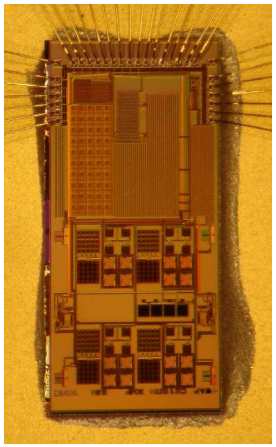
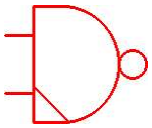
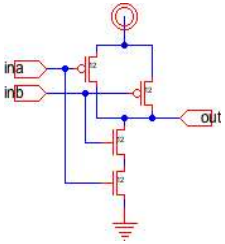
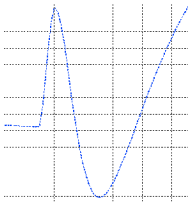
VLSI Design Workflow

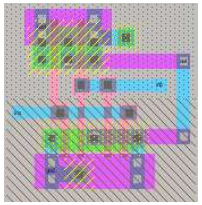
- In-house chip testing
  - > Test software library written in Java

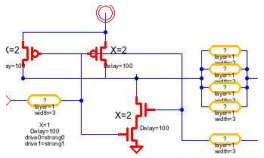


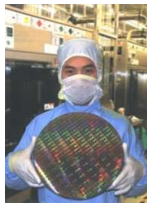


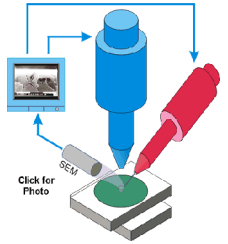






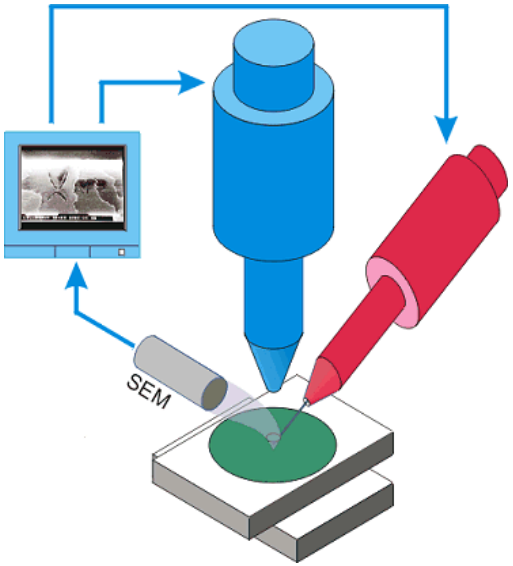


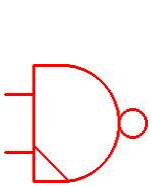


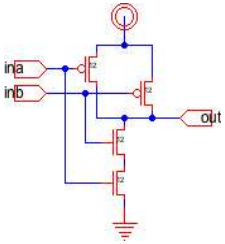


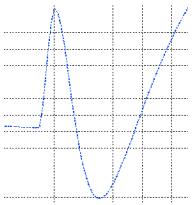
VLSI Design Workflow

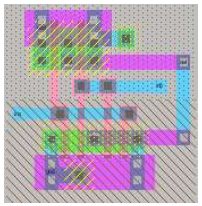
- Chip repair using FIB

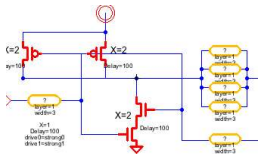


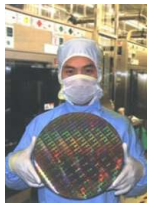


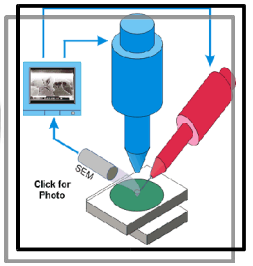












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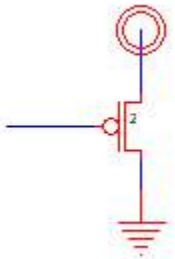
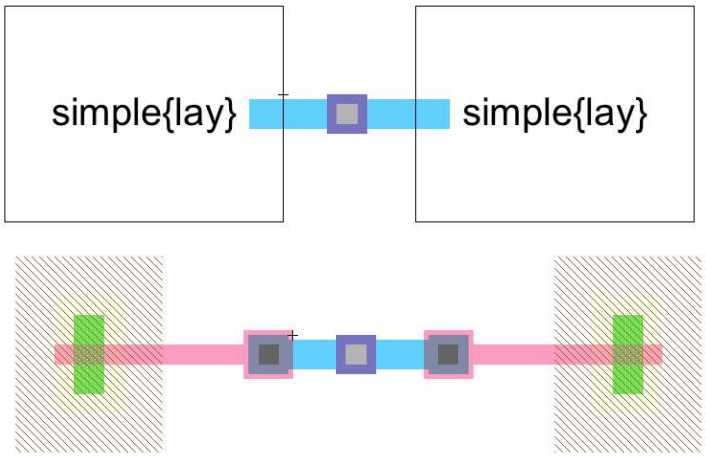
Electric Roadmap

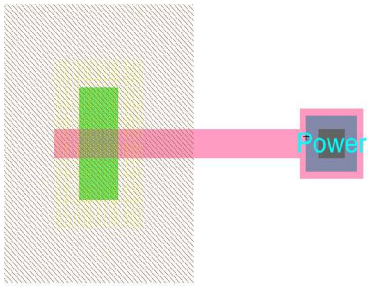
- Steven M. Rubin, author and owner
  - Development started in 1982
  - Open source vision: GNU license
    - ~50 contributors; >100 users, mainly in universities
- Original C code
  - 460k lines, 25% GUI
  - Ported to all platforms (v7.0 Sept 2004)
- Used since 2000 by Asynchronous Group
  - “Customer-owned tool” for custom solutions
  - Conjunction with Cadence tools

Electric Framework

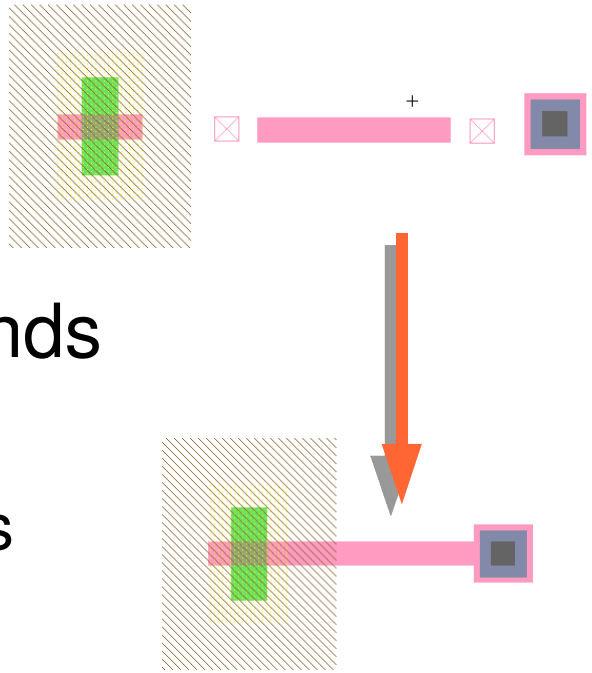
- Scalable database
  - > Nodes and arcs made of layers
  - > Instances and prototypes
  - > Hierarchical representation







Electric Framework ...



- Integrated circuit connectivity
  - Ports on nodes; pins for arc bends
  - Advantages
    - One UI for layouts and schematics
    - Topology-based tools are smarter
      - Can tolerate inaccurate geometry
    - No node extraction
      - can do LVS before DRC
    - Network information always available
  - Disadvantages
    - Extra work during layout (power tools help)
    - Display not WYSIWYG

Electric Framework ...

- Layout constraints
  - Built on topological representation
  - Rigid wires, fixed-angle wires, outward propagation
  - Enables “top-down” design
  - Demo! 

Electric Framework ...

- Extensible technologies
  - Moore's Law, fast trend
  - Encapsulates geometry, topology, and behavior
- Extensible tools
  - Tightly-coupled in a single process
  - Can run in parallel as appropriate
  - Listeners for interactive tools
- Powerful database
  - Constraint propagation, undo/redo
  - Plug-ins for proprietary and open source code

Java Framework

- Standard libraries
  - No need to re-invent the wheel
    - Collections, geometry operators
  - Code reduced by 2/3 over C
- UI and JFC/Swing
  - Platform independent components
    - C required many interface modules
- Interpreted environment enables faster development
- JavaDoc simplifies internal documentation

Java Framework ...

- Multi threading
  - Each task in a separate thread
  - Isolation of code failures
  - Enables multiprocessing
- Plug-ins via Reflection
  - Dynamically determines if code is available
- Java 3D – scene graph paradigm for rendering
  - Serialization
  - Demo! 

What is Next

- What to read
  - *Computer Aids for VLSI Design*, Steven M. Rubin
  - *Effective Java*, J. Bloch
  - *Logical Effort*, I. Sutherland, B. Sproull & D. Harris
- Challenges in Electric
  - Transactional database
  - Collaborative environment
  - More tools

Summary

- VLSI CAD tool for free
  - http://www.staticfreesoft.com
- Open source as valid option for technology development
- Java suitable for CAD applications
  - More stable, better UI, faster than C version
  - Ported useful subset in less than a year
  - Ported entire system in less than two years
  - Developers unfamiliar with Java at start

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Q&A