VLSI CAD Research @ Sun Microsystems

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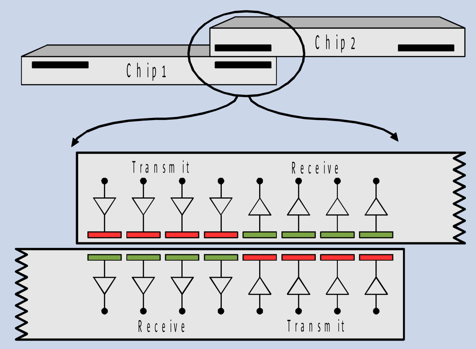
Sun Microsystems Laboratories, research.sun.com/vlsi

VLSI Research Group

- Focus on VLSI circuits and VLSI CAD issues
- Diverse research agenda, including
  - Proximity Communication, efficient wires, on-chip optics
  - Concurrent architectures, asynchronous circuits
  - **Cutting edge CAD and design optimization tools**



Proximity Communication

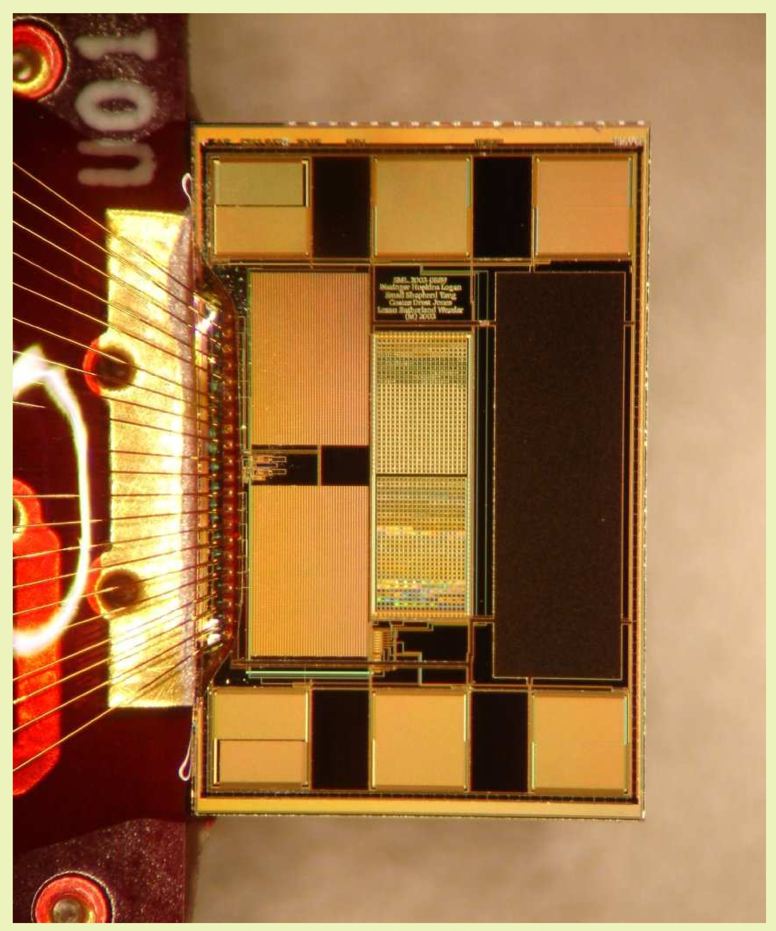
VLSI CAD Research

Challenges

- Increasingly complicated fabrication rules
- Exploding design complexity and team size
- Growing need for large data set visualization
- CAD tools must still be fast and responsive

Research topics

- Handling of large data sets
- Robust geometrical algorithms
- Data visualization
- Cross-site collaboration
- Parallelization of algorithms



Enable testchips like these (Collaboration with Harvey Mudd College, CA)

Electric VLSI Design System™

A complete chip design system

- Developed by Sun's VLSI Research Group
- Schematic capture, IC layout, design rule checks, simulation waveform display

Fully open source, written in Java

- A cross-platform framework for academic and open source collaboration

Next-generation CAD database

- Thread-safe database built with immutable objects
- Lazy construction of data structures
- Server/client decomposition enables cross-site collaborative design

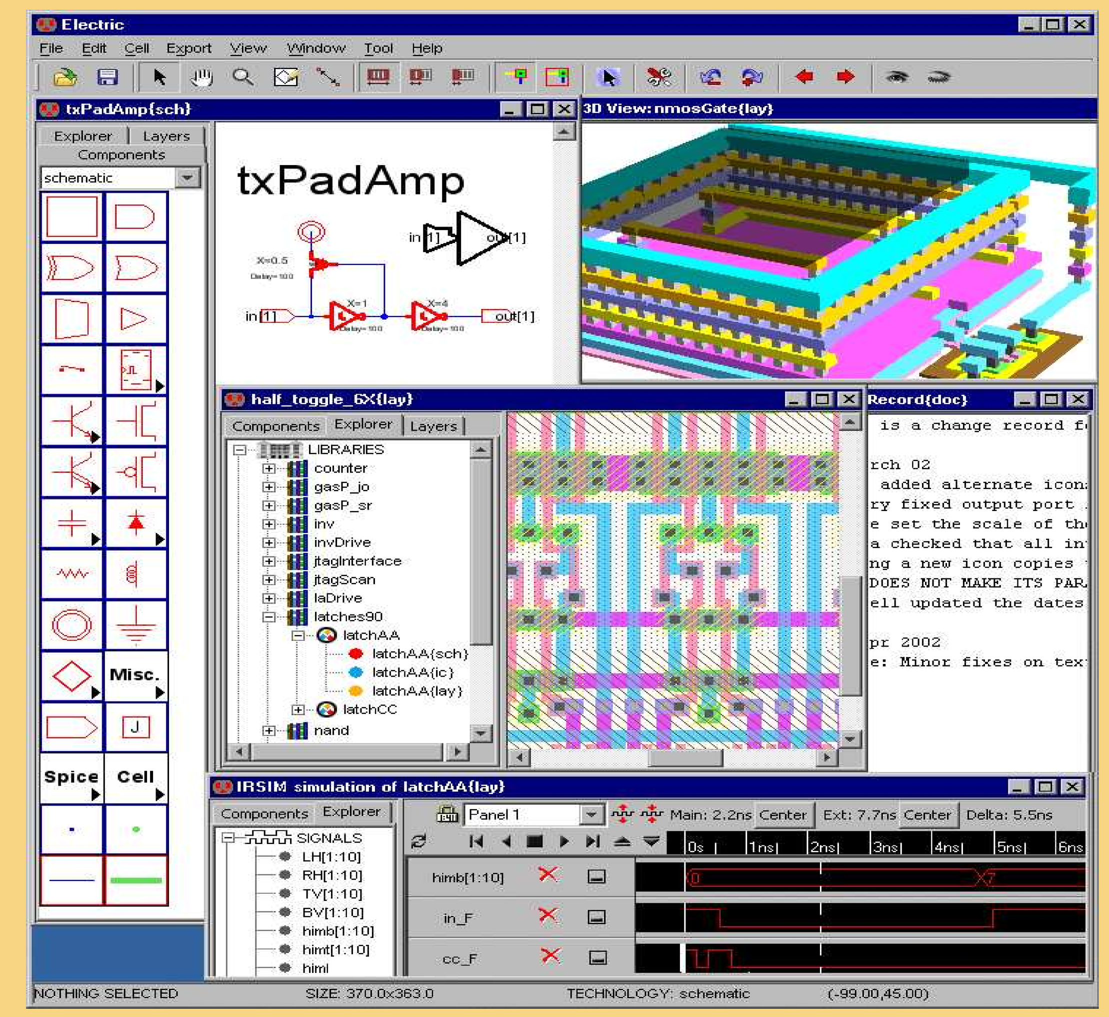
Multi-threaded CAD algorithms

- Leverage Java's multi-threading environment to gain CAD tool performance
- Independent threadable tasks controlled by Electric's job manager

Electric's capabilities

Design environment

- Schematic, netlist, icon, and layout views
- Simulation waves and cross-probing
- 3D layout views and text editing
- "Explorer tree" for selection

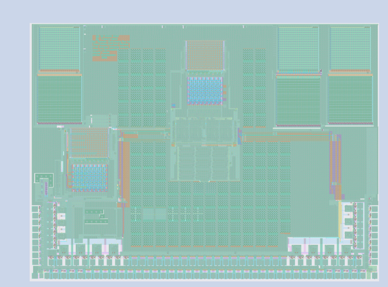


Tools available

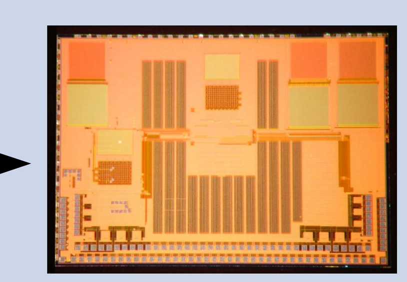
- Transistor sizing and logical effort
- Layout v/s schematics (LVS)
- Design rules checker (DRC)
- Electrical rules checker (ERC)
- Place and route flows
- Automatic gate and fill generators
- Electrical simulators
- Simple interfaces to many commercial tools

Using Electric in Sun Labs

- Fully supported in-house CAD tool
  - Facilitates research via building test chips
  - Augments commercial CAD platforms
- Platform for exploring CAD research



Electric layout



Actual chip

Examples of Electric-based CAD research

- Layout versus schematic: a critical design check prior to completing a chip design
  - Reduce layout and schematics each to graphs and perform a graph comparison
  - Commercial tools need > 1 hour to complete on a moderate chip ($25mm^2$)
  - Electric keeps the graph in memory already: does the check in 15s
- Connectivity checks through visualization
  - Sun's circuit designs use capacitive coupling, both on-chip and between-chips
  - Traditional validation flows fail, because the wires are not physically attached
  - Electric's visualization flow enables a rapid verification of the chip's correctness