
Sun
microsystems

Squaring the FIFO

in GasP

Jo Ebergen
Asynchronous Design Group
Sun Labs

Introduction

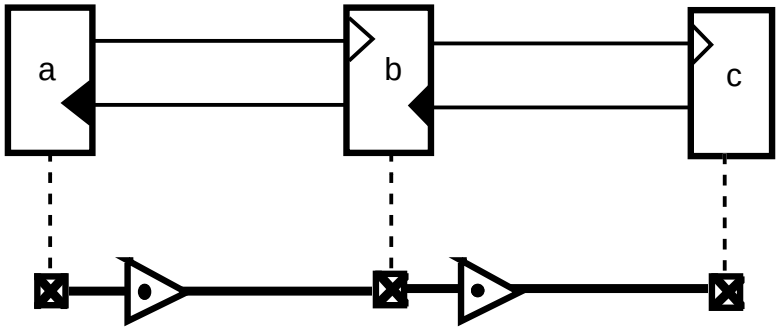
- A novel method for asynchronous design
  - GasP circuits
  - Notation for sequencing events
  - Logical Effort for uniform delays
- Example: Square FIFO
- Throughput of 1.56 GDI/s in 0.35u

Related Work

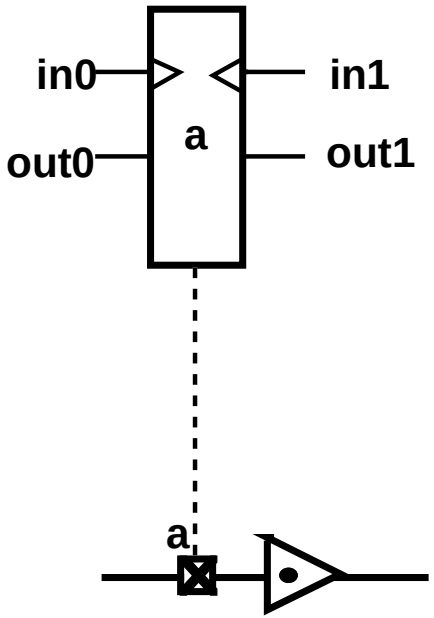
- asP* FIFO of Molnar et al.
- Self-resetting domino
- IBM's Interlocked Pipelined CMOS
- Erik Brunvand's Square FIFO

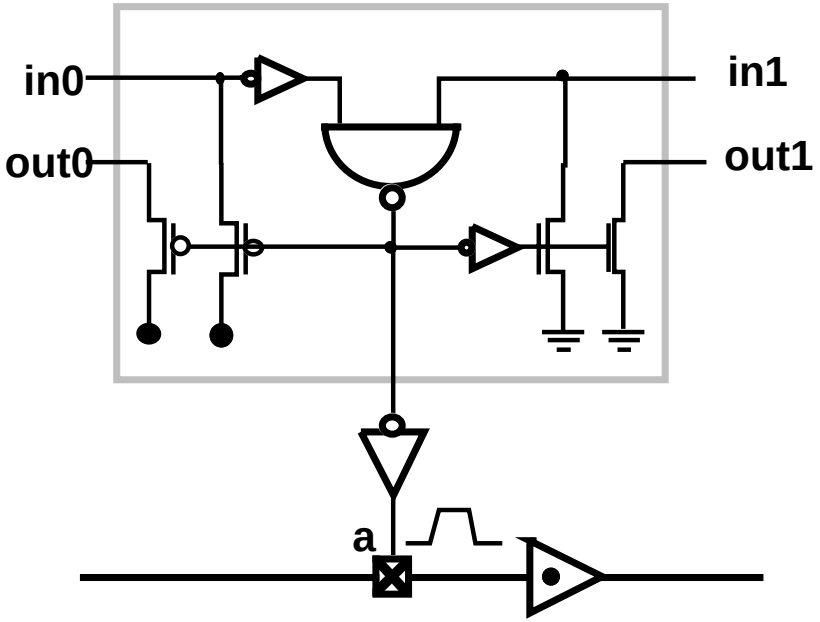
A GasP Module

- Control circuit = network of GasP modules
- GasP module realizes
  - Sequencing
  - Synchronization

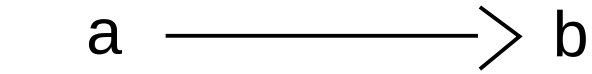


Inside a GasP Module

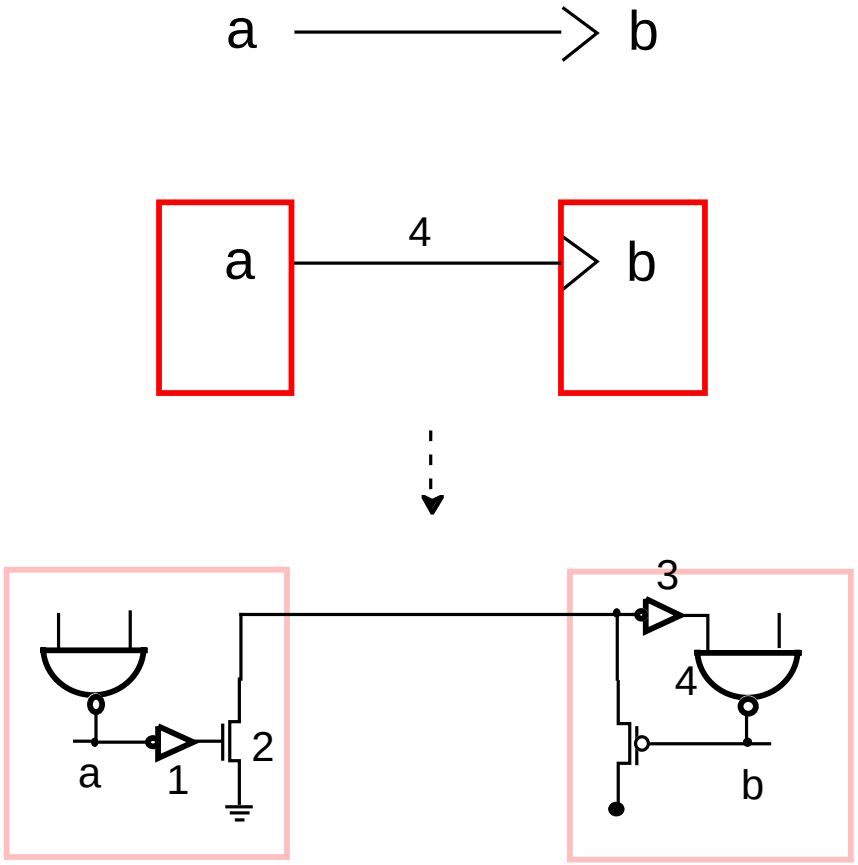




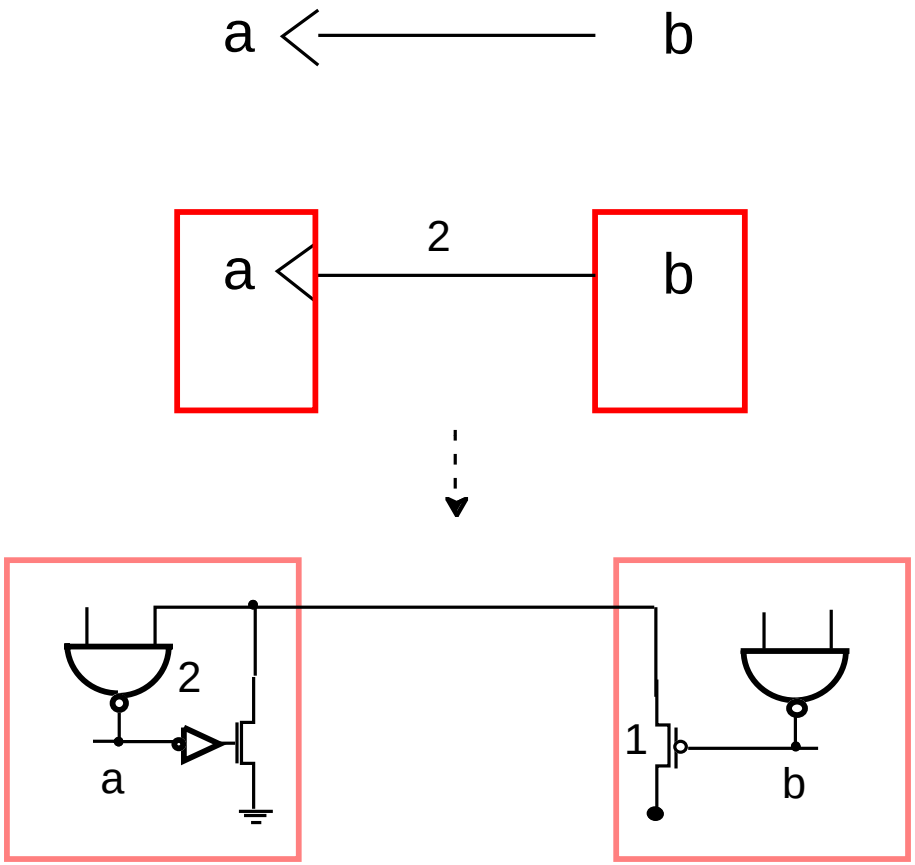
A Sequence of Events



Delay Assignment of 4



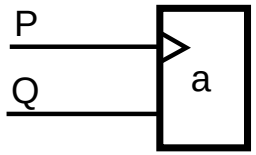
Delay Assignment of 2



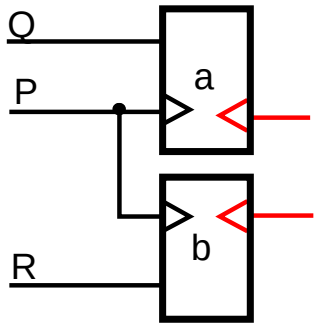
A Simple Translation

- **State: wire + keeper**
- **Event: GasP module**

```
P = (a -> Q)
```

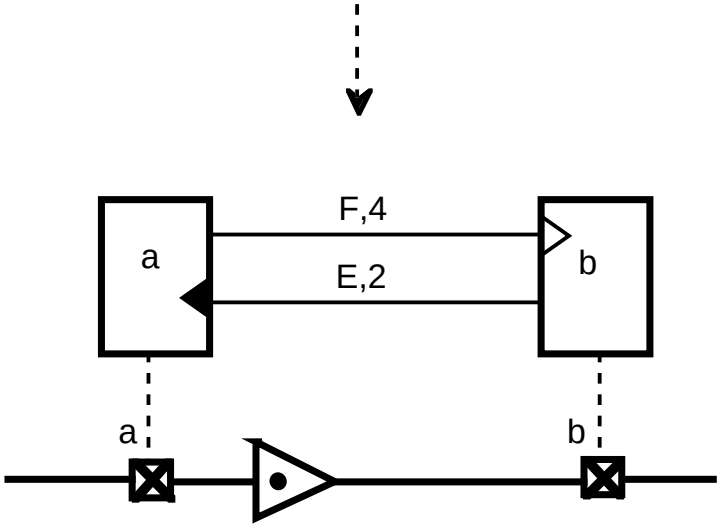



```
P = (a -> Q
    |b -> R)
```



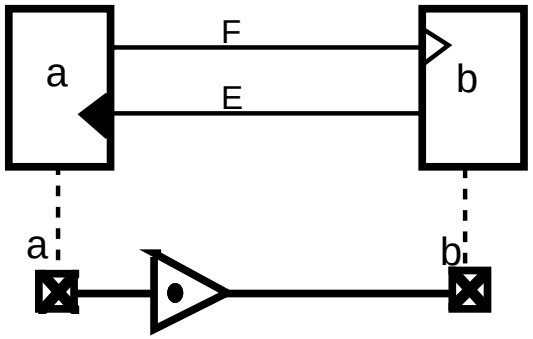
A One-Stage FIFO

```
Stage1 =
state E where
  E = (a -> F)
  F = (b -> E)
end
```

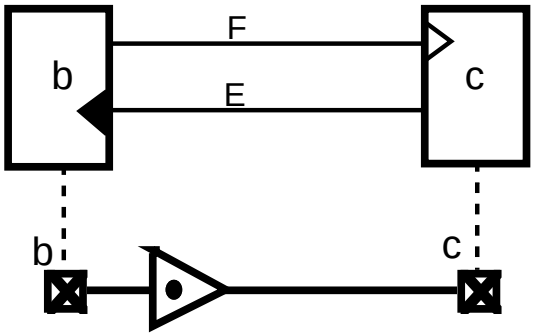


A Two-Stage FIFO (1)

```
Stage1 =
state E where
  E = (a -> F)
  F = (b -> E)
end
```

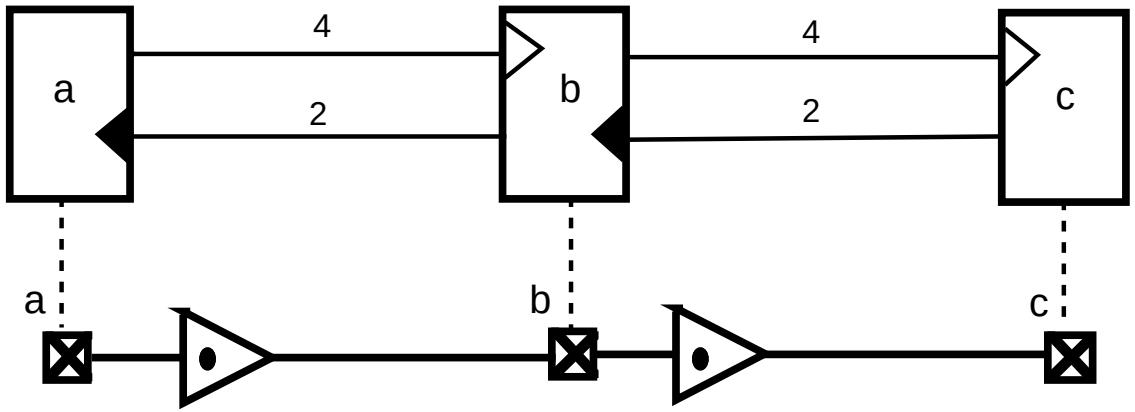



```
Stage2 =
state E where
  E = (b -> F)
  F = (c -> E)
end
```

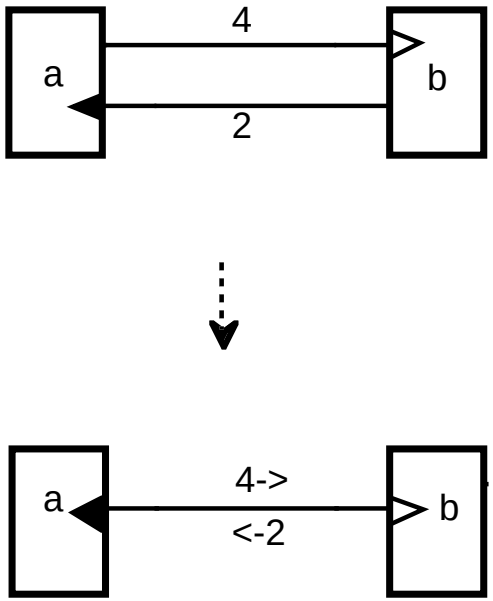


A Two-Stage FIFO (2)

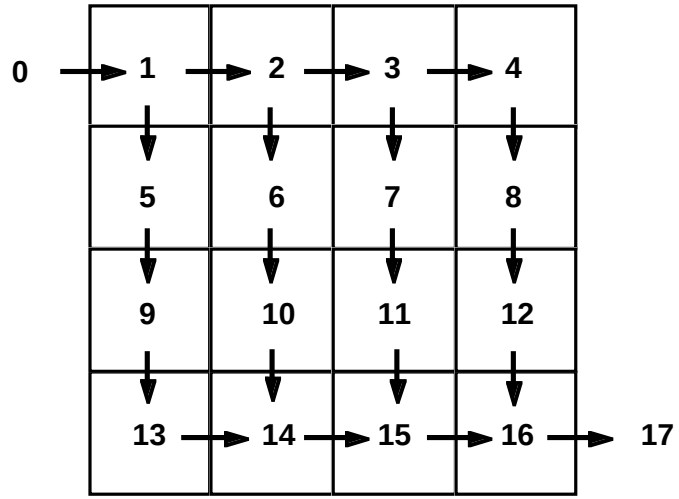
Stage1 & Stage2



A Peephole Optimization

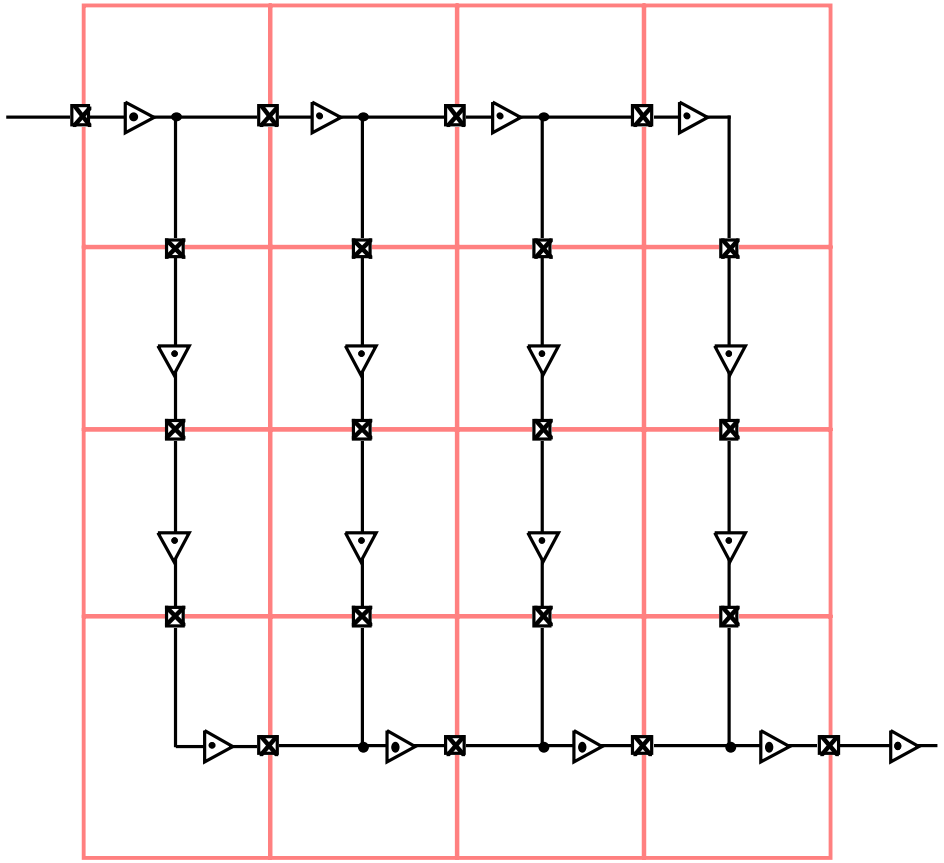


A Square FIFO



- Latency = 2*sqrt(N) for capacity=N
- Low Power
- Max throughput for large range of occupancies
- Simple layout

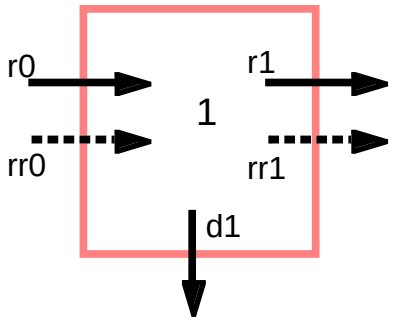
Data Path of Square FIFO



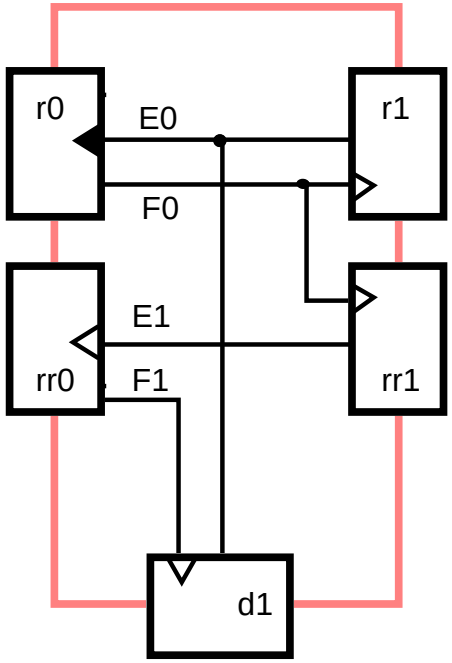
Implementation

- Each cell is a Finite State Machine
- Columns are linear FIFOs
- Top row and bottom row are special

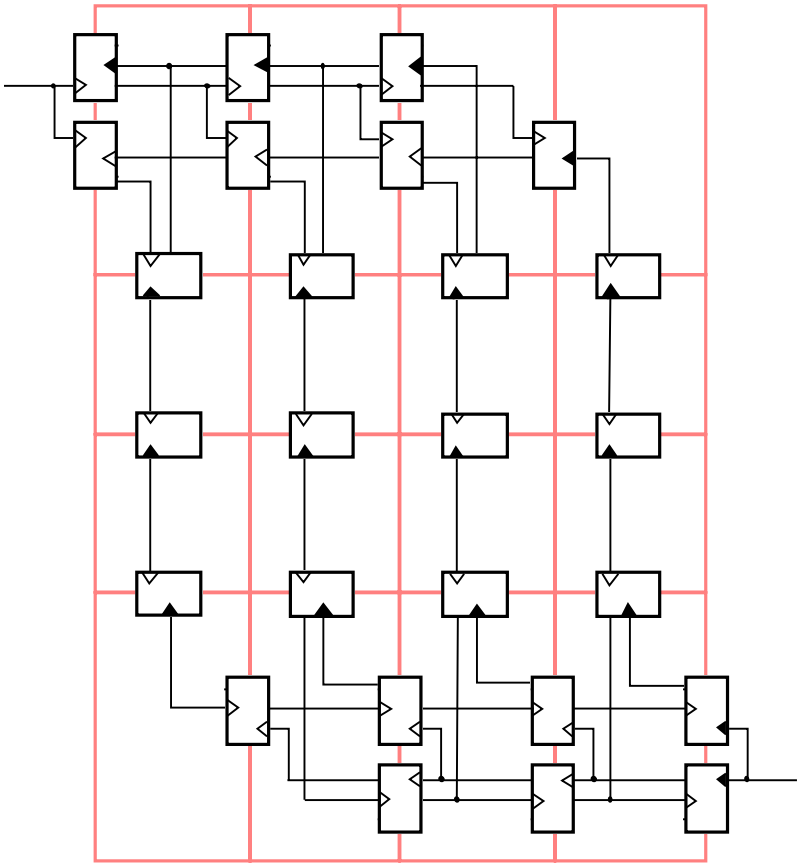
Implementation of Cell 1




```
Cell1 =
state E0 where
  E0 = (r0 -> F0)
  F0 = (r1 -> E0
       |rr1 -> E1)
  E1 = (rr0 -> F1)
  F1 = (d1 -> E0)
end
```



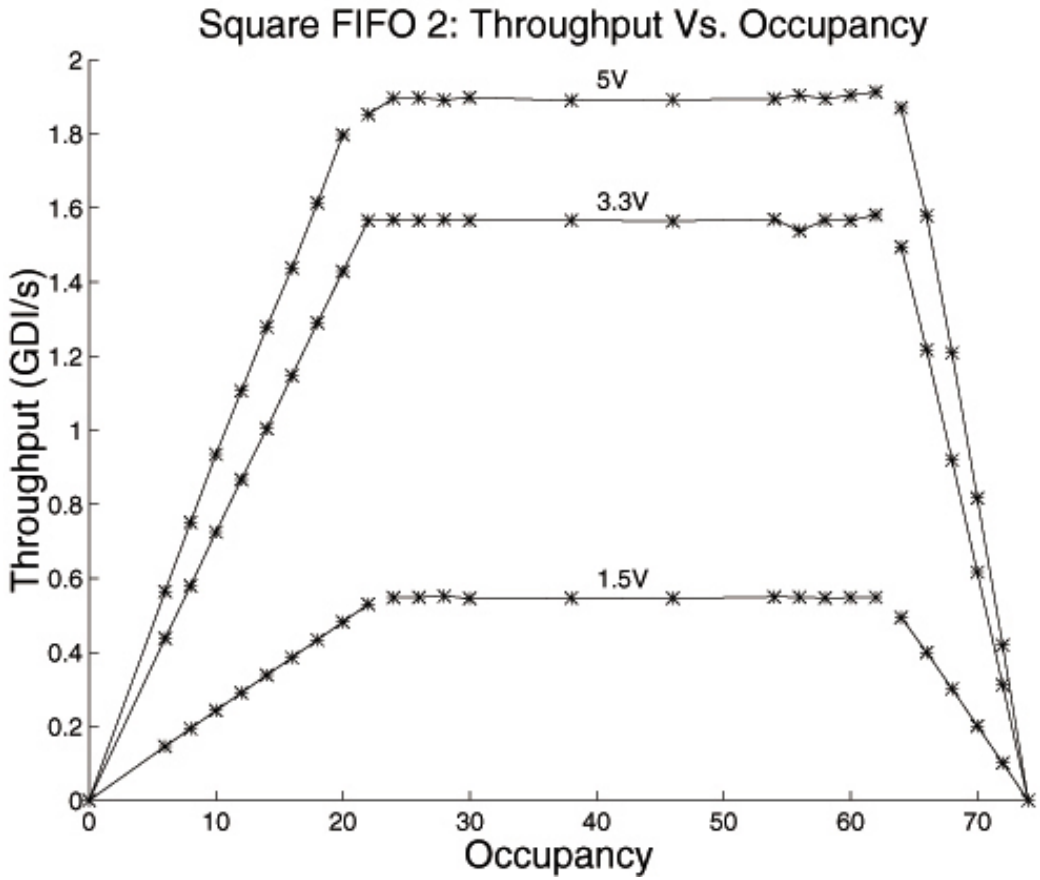
Complete Implementation for Control



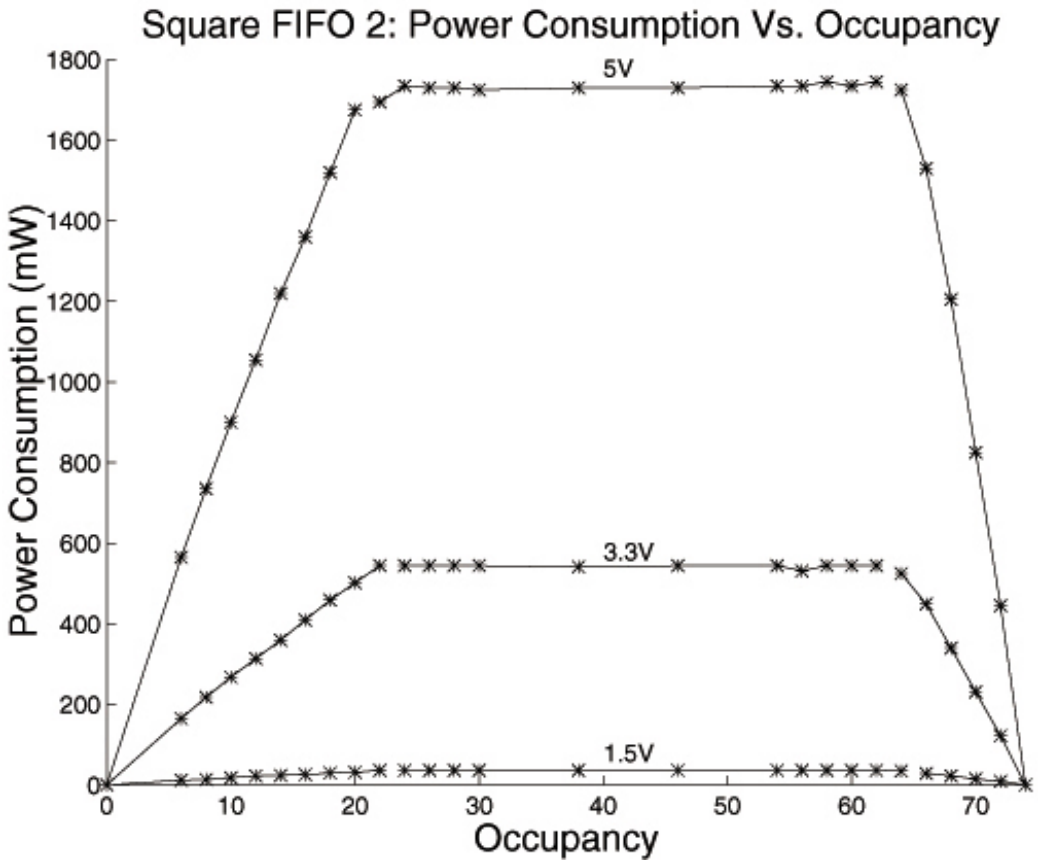
Experimental Results

- Fabricated in 0.35u CMOS through MOSIS
- Ring with two 5X5 and two 2X5 FIFOs
- Transistor sizing
- No bottlenecks
- First chip failed
  - Wire lengths grossly underestimated
- Second chip works fine

Throughput


Square FIFO 2: Throughput Vs. Occupancy
5V
3.3V
1.5V
Throughput (GDI/s)
Occupancy
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

Power Consumption



Concluding Remarks

- Speed, Speed, Speed
- Simple, Simple, Simple
- GasP, a minimal control primitive
- Control circuit = composition of FSMs
  - Event : GasP module
  - State : wire + keeper
- Careful sizing
  - Logical Effort
  - Wire estimates
- More testing needed


Sun
microsystems